Objectives of the Meeting

1) Make as sure as possible that NRAO and Innotech have the same understanding of the chip specification. This will probably require some review of the spec and some time to answer any questions Innotech will have.

2) Define to both NRAO's and Innotech's satisfaction the role NRAO is to take in monitoring and in aiding the chip development.

3) Come to a mutually acceptable understanding of the requirements and details of the test vector generation and chip simulation.

4) For NRAO to get as good an understanding of the entire design and development process as possible.

5) Come to a mutually acceptable understanding of how the chip pin assignments will be made.

6) Come to a mutually acceptable understanding of how the final chip package will be selected.

7) Resolve a possible change of spec that would do results read-out using a shift enable instead of a shift-out-clock. Note that the max shift-out rate was not specified but should be 125 MHz,

~ 7½ → 4K/16?

may be done clock

chematics that drive the
xors if that is better.

a output circuit may be

design to be used.

n technology for the
purchase request when

te as possible, without
ld like to know at what
and what design factors

equence as long as every
same number of pipeline
path. It would be best
ndary storage registers
to issue one or more
chip. This is acceptable
ere.

elays on data paths
ore than two delays would

ch suggests such as a PLL

power and ground pins
ect Innotech to provide
ation of such items.