Module; ALMA Test Correlator sampler
Responsible engineer; Ray Escoffier
Number required for test correlator; 4 (two per antenna)
Form factor; two-wide VLBA module with a rear 80-pin card edge connectorfor power, 100 MHz clock and the digital outputs and an SMA connectoraccessible from the module rear for the RF input.
RF input; 1.6 GHz to 2.4 GHz, 50 ohm, -14 dBm
Clock input; 100 MHz sinewave, about 2 VPP, terminated in 50 ohm to ground.
Control signal inputs; none
Digital output; sixteen 2-bit ECL output lines (outputs are single endedand require 50 ohm terminations to -2 VDC at the load).
Schematic; GBT/Tucson drawing 35208LO20 (LO20D01.SCH)
DC Power; + 5.0 VDC @ 0.03 Amp

- 5.2 VDC @ 1.9 Amp
+12.0 VDC @ 0.06 Amp
-12.0 VDC @ 0.01 Amp
+15.0 VDC @ 0.1 Amp
Cooling; ? CFM at ? C
Comment; The samplers can be housed two ways. At present, there is a VLBAbin with all 4 samplers mounted in the correlator rack. There are also twoextra VLBA bins, at present un-wired, to be used when the samplers aremoved to the antennas.
System; ALMA Test Correlator
Responsible engineer; Ray Escoffier
Form factor; one 24 inch EMI shielded rack
Clock input; 100 MHz sinewave, 50 ohm, 0 dBm (SMA connector)
Data input; sixteen single ended 2-bit ECL signals from each of 4 samplers(inputs have 50 ohm termination resistors to -2 VDC).
Sync input; 1 PPS (TTL logic leve1, 50 ohm input)
Computer communication; Ether net
AC Power; 30 Amp 240 VAC 3-phase circuit for digital logic117 VAC circuit for VME crateCooling; requires refrigerated air from computer floor (system dissipationis about 1 kW )
Comment; In the present configuration with the samplers in the correlatorrack, there are four 8-signal cables between each sampler and the samplerdistribution card. When the samplers are moved to the antennas, interface


## ALMA Test Correlator

| ALMA Test Correlator |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MODE | BANDWIDTH | PRODUCTS |  |  | LAGS |  | DELAY RESOLUTION | DELA | Y RANGE |
| 1 | 800 MHz | $\begin{array}{lll} O R & X & 1 R \\ O L & X & 1 L \\ O R & X & 1 L \\ O L & X & 1 R \end{array}$ | 512 | LEADS | $\begin{aligned} & \text { AND } 512 \\ & \\| \\ & \# \end{aligned}$ | LAGS | $8-S A M P L E S$ | 10 | uSEC |
| 2 | 800 MHz | $\begin{aligned} & 0 R \times 1 R \\ & 0 L \times 1 L \end{aligned}$ | 1024 | LEADS | $\text { AND } 1024$ | LAGS | 8-SAMPLES |  | uSEC |
| 3 | 800 MHz | OR X OR <br> OL X OL <br> 1 RX 1 R <br> 1L X 1L |  |  | $4 \text { LAGS }$ |  |  |  | - |
| 4 | 100 MHz | $\begin{array}{lll} O R & 1 R \\ O L & X & 1 L \\ O R & X & 1 L \\ O L & X & 1 R \end{array}$ | 4096 | LEADS | $\text { AND } 4096$ | LAGS | 4-SAMPLES | $80$ | uSEC |
| 5 | 100 MHz | $\begin{aligned} & 0 R \times 1 R \\ & 0 L \times 1 L \end{aligned}$ | 8192 | LEADS | $\text { AND } 8192$ | LAGS | 4-SAMPLES |  | uSEC |
| 6 | 100 MHz | $\begin{aligned} & O R \times O R \\ & O L X O L \end{aligned}$ |  | 8192 | , LAGS |  |  |  | - |
| 7 | 100 MHz | $\begin{aligned} & 1 R \times 1 R \\ & 1 L \times 1 L \end{aligned}$ |  | 8192 | $2 \text { LAGS }$ |  | - |  | - |

