ALMA Memo No. 532

The ALMA 3-bit 4 Gsample/s, 2-4 GHz Input Bandwidth, Flash Analog-to-Digital Converter

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Abstract: A high speed low power analog-to-digital converter (ADC) using the 0.25µm BiCMOS SiGe technology from ST Microelectronics has been developed to meet the specifications of the ALMA project. The main features of this ADC are: 3-bit resolution (8 quantization levels) in Gray code, an input bandwidth from 2 to 4 GHz, 4 GHz sampling rate (and possible operation up to 5 GHz), LVDS standard I/Os and low power dissipation (~ 1.4 W). We present in this paper some details of our ADC design and performance results obtained with the ALMA digitizer assembly including one ADC followed by three high speed 1:16 deserializers. ALMA production acceptance tests are briefly described.

1. Introduction

In the ALMA processing chain (Fig. 1) the Digitizer converts the analog signal delivered by the selected receiver and the intermediate frequency (IF) downconversion stage into a fully digital signal. The Digitizer includes a 3-bit Analog-to-Digital Converter (ADC) and three demultiplexers (DEMUX in Fig.1), one for each ADC output bit. The ADC sampling frequency is 4 GHz and the DEMUX stage decreases the data flow down to 250 MHz before the data are further processed, transported through an optic fiber line and finally correlated.

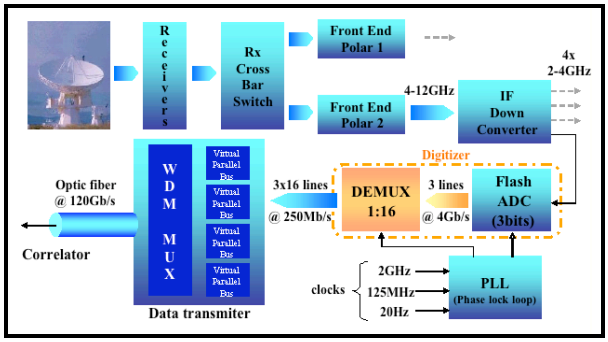

Fig. 1. Schematic of the data processing chain showing the ALMA Digitizer (flash ADC followed by three 1:16 deserializers)

The main specifications of the ALMA ADC are the following (see e.g. [1]): input bandwidth from 2 to 4 GHz; 4 Gsample/s sampling rate; 3-bit, 8-level resolution; LVDS I/Os; low power dissipation. The latter specification is most important in view of the long lifetime of the ALMA project (at least 30 years) and of the high elevation of the ALMA site (5000-m in a desertic area preventing any easy on-site maintenance). Because of ALMA interferometric system constraints related to the relative delays between the cosmic waves captured by the individual antennas, the 4 GHz clock will undergo a phase shift in order to implement the required time fine delays. Therefore, the ALMA ADC and deserializers must be synchronized with the outside 4 GHz and 250 MHz signals delivered by the special 4 GHz clock module (PLL in Fig. 1).
Some commercial high speed ADC products approaching the ALMA specifications exist. However, no one accepts an input signal up to 4 GHz and most of them offer more bits than actually required and thus exhibit high power consumption (several Watts) not well suited to the ALMA project. Therefore, a new ADC has been designed for the specific ALMA requirements. This effort was first described in general terms in [1] and first results obtained with the 2-bit and 3-bit versions of the ALMA sampler were given in [1], [2] and [9]. The design and performance results of the ALMA demultiplexer associated with the ALMA converter were given in [3].
In this paper, following general comments given in Section 2, we describe in Section 3 the ALMA 3-bit, 8-level ADC design, present in Section 4 test results and ADC performances in the complete ALMA digitizer assembly, briefly describe in Section 5 the production acceptance tests, outline in Section 6 new ideas on future works, and finally draw conclusions in Section 7.
An ALMA ADC Data Sheet has been prepared [4].

2. ADC structure and resolution

Specifying the main characteristics of an ADC (input bandwidth – speed – resolution – consumption – cost)

leads to the most appropriate topology for a dedicated application. There are several possible architectures for an ADC (e.g. [5]) and selecting a specific one becomes easier if no more than two ADC characteristics dominate. However, the ADC designer often has to realistically balance between several contradictory parameters.

The three main architectures which allow a high speed conversion are (e.g. [5]):

- SAR converter (Successive Approximation Register)
- Pipeline converter
- Flash converter

Currently, the commercial products with sampling clocks up to about 2 GHz adopt the flash structure. Nevertheless, this architecture doubles the ADC power dissipation for each additional bit. It is thus best suited to low resolution applications which is the general case in radio astronomy where the signal-to-noise ratios can be improved with long integration times.

The resolution of any converter must be sufficient in order to preserve the integrity of the analyzed signal. However, it is not mandatory to have a large number of bits to convert the signals radiated by cosmic radio sources because of the white noise nature of these signals (Gaussian statistics) and because they do not rapidly change with time (in contrast with current applications of ADCs). Therefore, in radio astronomy observations or in passive radio observations (e.g. atmospheric sounding) digitization can be carried out with a few bits resolution without causing information loss, provided that the input signal is integrated enough time to extract the useful scientific data it contains. (We note, however, that at low observing frequencies the level of radio frequency interferences may degrade the incoming signals whose integrity could be better preserved with high resolution ADCs.)

In this context, digitization implies a loss of sensitivity at the signal detection stage (auto- or cross-correlation) which can thus be recovered with long integration times. The sensitivity loss as a function of the ADC bit resolution has been derived in a number of works ([6], [7], [8]). It is rather large between 1 and 3 bits but becomes negligible above 3 bits (2-bit ADCs are common practice in radio astronomy). Because of this behavior and because of increasing power dissipation with the number of bits a 3-bit resolution ADC has been chosen for the ALMA project.

3. ALMA ADC description

Two ALMA prototype samplers have been designed, but only one meets the requirements for industrial mass production. The description and results presented in this paper refer to the design selected for mass production. This is a flash ADC design called VEGA 1. The chip integrates an input adapter amplifier, seven comparators (one per comparison level to provide 8 levels) with associated latches, an encoder matrix and three output buffers (Fig. 2).

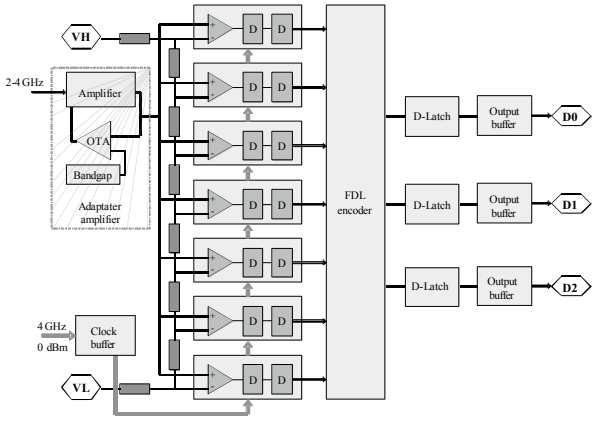

Fig. 2. ALMA converter block diagram

3.1. Input adapter amplifier

The input adapter amplifier (Fig. 3) is a low gain analog stage.

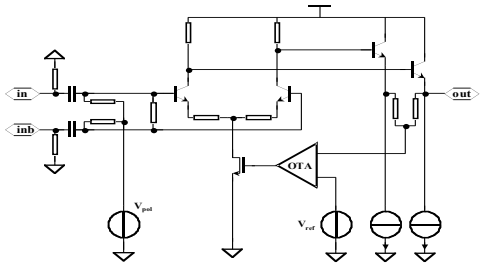

Fig. 3. Schematic of the input adapter amplifier

This critical stage performs 50 Ω matching over the overall input band (2 to 4 GHz), amplifies and converts the input asymmetrical signal into a differential one which is later sampled in the ASIC sampling cells. Simulations show that the response of this amplifier is linear up to 0 dBm at the ASIC input and that the ripple up to 4 GHz is negligible. (For the complete digitizer assembly the ripple should not exceed ±0.5 dB, see Section 4.2.2)

A common mode feedback loop (CMFB) is implemented in the chip to stabilize the mean voltage at the amplifier output in spite of possible temperature and fabrication process variations. The output common mode voltage is compared with a voltage reference generated on-chip by a 'Bandgap' cell. The operational transconductance amplifier (OTA) output is filtered with a low pass filter, and this voltage drives the current generator of the input differential pair.

3.2. Voltage thresholds

The comparator is made up of two amplification stages. This structure suppresses the metastability states by

providing more amplification of the input signal which decreases the indecision level and allows a better conversion speed to hold a state comparison result.

3.3. D-Latches

Two D-Latches perform the sampling function after the comparator in a master-slave configuration (Fig. 4).

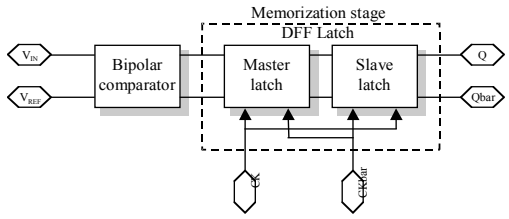

Fig. 4. Sampling cell block diagram

In order to decrease the number of stacked transistors and to be compatible with a low voltage supply technology, the clock is applied on the latches current sources (Fig. 5). In this pseudo-differential structure the NMOS transistor driven by the clock is a current source during one half-period and an open switch during the remaining half period.

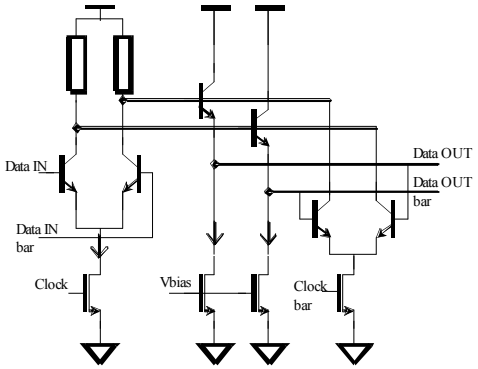

Fig. 5. Schematic of the D-latches

3.4. Clock amplifier

We have designed a dedicated clock amplifier block (Fig. 6) to drive the D-Latches. The first stages of this cell use voltage amplifiers while the last stages are current amplifiers in order to increase the fan-out required by the large number of latches.

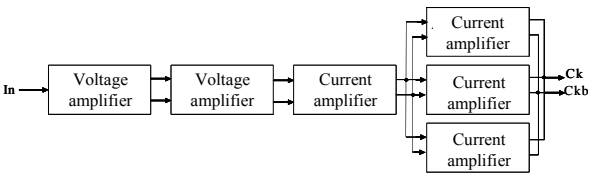

Fig. 6. Clock amplifier block diagram

All current amplifiers have the same structure (Fig. 7). The input signal drives the bipolar transistors in one conduction mode and the NMOS transistors in the opposite mode. Thanks to this structure, we cancel the static current in order to decrease the power consumption and generate an output voltage swing of 1.4 V.

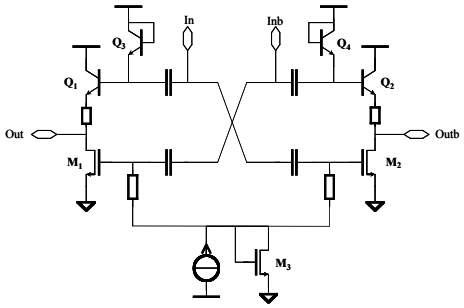

Fig. 7. Schematic of the current amplifier in the clock amplifier

3.5. Encoder

The FDL encoder (Fig. 8) converts the comparators results into a Gray code. This encoding process is implemented by using a current mode technique thanks to the association of several current generators.

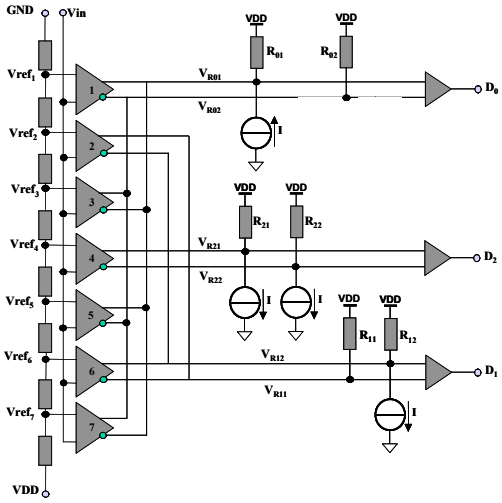

Fig. 8. Topology of the FDL encoder

3.6. Output buffer

The output buffer (Fig. 9) is implemented to convert the encoder output into a signal compatible with the LVDS standard (see Table 2). The output voltage swing is fixed by the two resistors in the differential pair and the current source.

Before the output PADs, an R-C filter has been integrated in order to decrease the transition time and the parasitic effects due to the bonding.

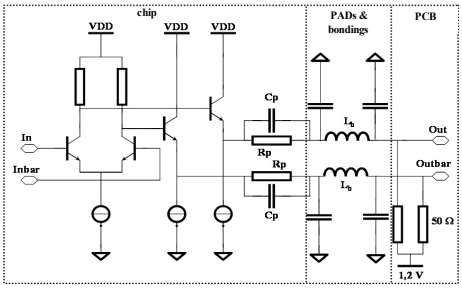

Fig. 9. Schematic of the output buffer

4. Test results

In order to verify the ADC functionality and to measure the ADC characteristics we have assembled the packaged VEGA 1 chip on a specific PCB for stand-alone tests. This PCB is also used together with the ALMA demultiplexing chips in the ALMA digitizer assembly (see Fig. 13). The VEGA 1 chip is available in a 44-pin ESD-protected VQFN package.
Details of the VQFN package together with some DC electrical and dynamic characteristics of the VEGA 1 chip are given in the ALMA 3-bit ADC Data Sheet [4].

4.1. Stand-alone ADC tests

The VEGA 1 chip, ALMA converter PCB and mechanical housing are shown in Fig 10. The ADC test procedure includes functionality tests and performance measurements. VEGA 1 functionality has been tested up to 5 GHz.

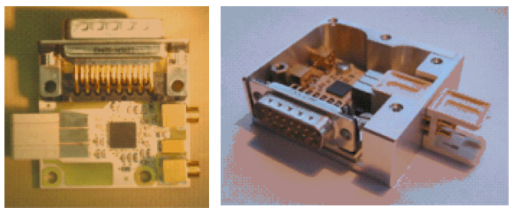

Fig. 10. Photograph of packaged VEGA 1 and converter subassembly

4.1.1. Currents check-out

The currents test purpose is to verify that there is good electrical connectivity between the chip and its package and the PCB and that all of the ADC internal blocks are functional. The converter has seven independent internal power supplies. A non-nominal current consumption measurement would demonstrate a potential problem such as a short-circuit, an open circuit or an internal cell failure. An example of such tests undertaken with 14 different converters assembled on the same type of PCB is given in Table 1. (Converter number SN011 was not included in the analysis.)

Table 1: Current test results obtained in fourteen VEGA 1 converters

	IDDA1	IDDA2	IDDCK	IDDBM	IDD0	IDD1	IDD2
SN001	130	95	101	156	25*	24*	24*
SN002	108	114	86	142	34	33	33
SN003	134	98	108	164	26*	25*	25*
SN004	129	96	104	158	25*	24*	24*
SN005	127	97	104	159	24*	25*	25*
SN006	132	97	107	154	31	32	31
SN007	138	99	105	168	25*	25*	25*
SN008	131	98	107	156	26*	25*	25*
SN009	135	97	106	160	34	33	33
SN010	130	95	106	163	32	30	31
SN012	103	104	83	138	36	33	33
SN013	118	109	81	140	35	33	35
SN014	113	106	85	137	37	34	35
SN015	107	109	88	143	35	33	35
VAL Min	103	95	81	137	24	24	24
VAL Max	138	114	108	168	37	34	35
VAL Moy	124	101	98	153	30	29	30

The currents are in mA and correspond to the input amplifier (IDDA1), comparators (IDDA2), clock (IDDCK), and D-latches (IDDBM) blocks. The output buffer currents are noted IDD0, IDD1 and IDD2. There is a relatively small dispersion of the measurements around the average currents given in the last row of Table 1. The random distribution of the measured currents is dominated by manufacturing process discrepancies which we have modeled with Monte Carlo simulations. Our measurements are consistent with the simulation results of our ADC design.

4.1.2. Eye diagrams

The eye diagrams of the VEGA 1 converter demonstrate that the output signals are in agreement with the LVDS standard voltage range (see Fig. 11 and Table 2).

Table 2: LVDS standard

	Min	Typ	Max	Unit
Differential input impedance	80	100	120	Ω
Common mode voltage signal	0.925		1.475	V
Differential voltage	250		400	mV
Input common mode current (LVDS input = 1.2V)		350		µA

They confirm that the following demultiplexing stages can be driven by the converter outputs, and they show good time coherence for the three output bits (maximum rising and falling edge times lie around 80 psec to be compared to the 250 psec period of the 4 GHz clock).

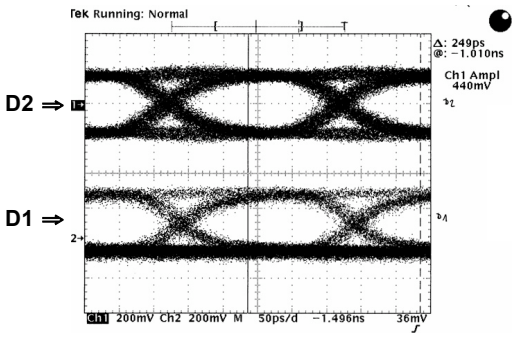

Fig. 11. Examples of eye diagrams for D2 (sign) and D1 output bits

4.1.3. Output code

We have also checked that for different input sinusoidal signals the output code is in agreement with the theoretical Gray code.

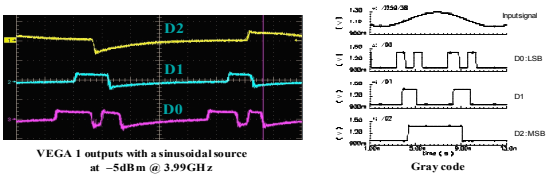

Fig. 12. Output code comparison with the theoretical Gray code

An example is shown in Fig. 12 where an input sinusoidal waveform at 3.99 GHz is sampled at 4 GHz. The observed output code is at 10 MHz (left hand side of figure) and can thus be recorded with a low frequency oscilloscope (the observed shape of the stable states is due to the capacitive link between the converter and the oscilloscope). D2 is the sign bit and D0 is the less significant bit. The expected standard Gray code is shown in the right hand side of Fig. 12.

4.2. ALMA digitizer

When the converter is associated with 3 deserializers (see description in [3]), they form one of the two polarization channels of the full ALMA digitizer assembly (Fig. 13). In this configuration, the ALMA ADC can be characterized either with a specific Digitizer Test Equipment (DTE) described in [10] or with the digital Test Fixture also used by the ALMA correlator team to qualify their digital filters. The DTE is our current tool for adjustments and performance check-outs of the VEGA 1 chip and ALMA digitizer. It performs an auto-correlation function of the 2-4 GHz input signal thanks to an FPGA bonded on a test card directly connected to one of the two output connectors of the DG assembly (see Test connector in Fig. 16); the digitizer frequency spectrum and other quantities are displayed using the LabView environment.

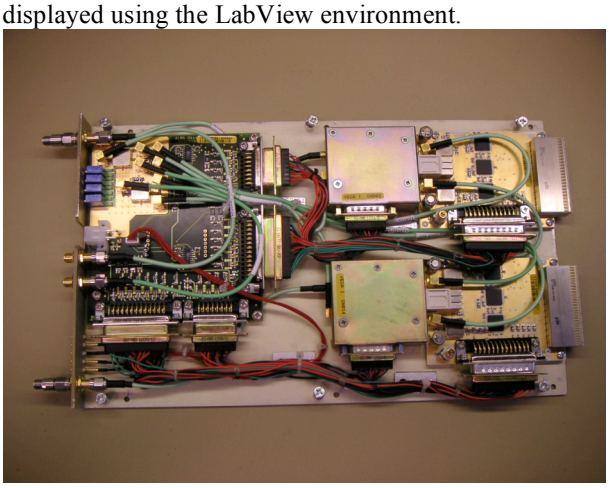

Fig. 13. Photograph of one uncovered DG assembly showing two polarization channels each one including one ADC (in mechanical housing) followed by three uncovered demultiplexing chips

When all functional tests concerning the power supplies and clock distribution of the digitizer assembly have been performed three main dynamic tests (see below) are performed to qualify the ALMA digitizer. All tests are described in the digitizer assembly test plan [11].

4.2.1. Threshold spacings

Using a broad band, temperature-controlled, noise source at the input of the ALMA digitizer allows us to measure and display the VEGA 1 state counts with the DTE. Assuming a Gaussian signal around 0 dBm ± 1dB at the digitizer assembly input -as expected during astronomical observations- one should observe a Gaussian probability distribution of the state counts measured in the equally distributed comparator thresholds of the ADC. Simulations show that a ± 1dB deviation from the expected 0 dBm input power results in an insignificant sensitivity loss (from an optimum 3.75% to 3.95% sensitivity loss). The measured statistical distribution may exhibit several types of distortion as illustrated in Fig. 14: static offset due to incorrect position of the thresholds or any dynamic offset due, for example, to an overdriving input or a clock feedback to the analog input. The ALMA converter is adjusted with our DTE and ready for operation when the counts are close to a Gaussian distribution.

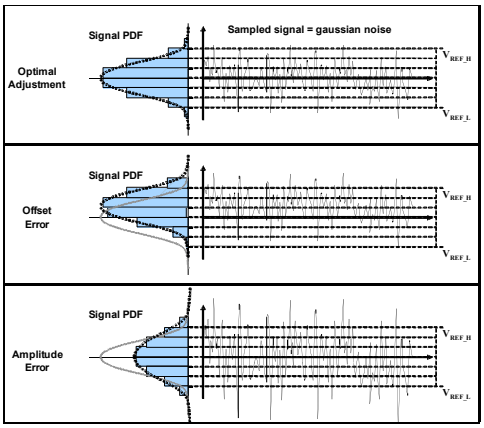

Fig. 14. Examples of optimum Gaussian distribution and of possible distortion of probability distribution function

In addition, we have verified that the Gaussian statistic distribution does not change with temperature when the common mode feedback (CMFB) loop mentioned in Section 3.1 is enabled; and we have observed changes with temperature when the CMFB is disabled. These tests performed in the range 0 to 50°C allow us to validate the CMFB loop and to confirm immunity of the ALMA converter to temperature drifts.

4.2.2. Frequency response

With the 2-4 GHz noise source added at the digitizer assembly input and using the DTE to analyze the assembly response we are able to reconstruct the power spectrum at the input of the assembly and compare it to the noise source spectrum (see [11]). The FFT of the auto-correlation function should mimic the noise source spectrum. However, there is a slope of a few dBs due to the converter subassembly which we must correct in our design. This initial slope is due to several factors such as transfer losses in the transmission cables, the subassembly PCB or the connectors, and to parasitic effects related to the metallic lines within the chip. This slope is corrected by adding passive components on the converter PCB to form a high pass filter. A reconstructed spectrum for the complete digitizer assembly, including the demultiplexing stage, is shown in Fig. 15.

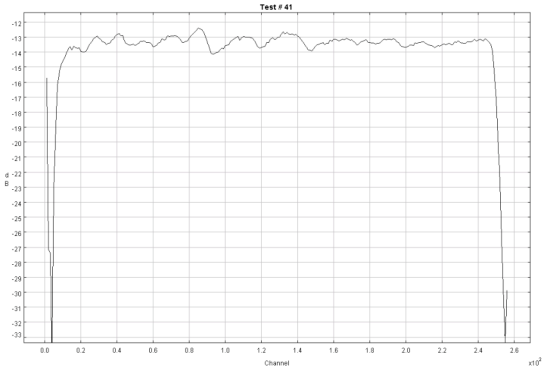

Fig. 15. Digitizer assembly response to 0 dBm broad band noise source across 2 GHz bandwidth (frequency axis is in channel number). The ripple is less than ± 0.5 dB

We have also used the DTE to measure the baseband ripple introduced by the digitizer assembly. With a weak (around -20 dBm) single tone signal added to the 0 dBm broad band noise source we have measured the level of this signal when it is shifted across the 2 to 4 GHz input bandwidth; the measured ripple including the remaining broad band slope is less than or around ± 0.5 dB from 2 to 4 GHz.

4.2.3. Digitizer assembly stability

In order to test the digitizer assembly stability we use a broad band, temperature-controlled, noise source and the DTE to estimate the Allan variance of the sampled data. Channel 'zero' of the DTE auto-correlation function represents the input signal total power and we estimate the time stability of the digitizer assembly by measuring the Allan variance of this channel as defined in [10]. The digitizer input data set is split into several slices of τ duration. For each time segment one derives the mean value and the variance of this statistical value over the whole set of time slices; the same derivation is later performed with an increased τ duration. Our measurements are performed in a controlled frequency, voltage and temperature environment so that any bias or gain drifts are minimized.

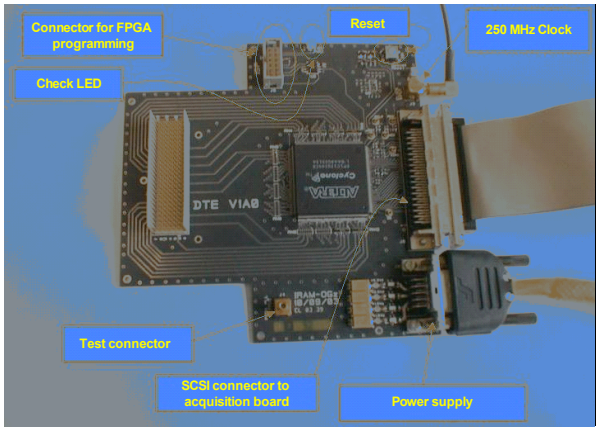

Fig. 16. Digitizer Test Equipment (DTE) showing various connectors and the FPGA (picture center) used for ALMA digitizer assembly signal processing

Time stability for the ALMA project is driven by two main basic integration times: 16 ms min for fast interferometric mapping; and up to around 1 minute for coherent long time integrations. Fig. 17 shows a typical Allan variance profile versus integration time for an ALMA digitizer assembly. The variance profile exhibits the improvement expected with integration time.

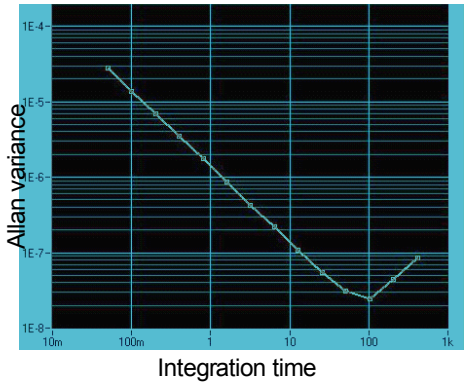

Fig. 17. Typical Allan variance of ALMA digitizers. The variance reaches a few 10^{-8} in 100 seconds

5. Power dissipation and ALMA production acceptance tests

One of the most important requirements of the ALMA ADC design is to achieve low power dissipation under normal operation in order to maximize the lifetime. The ALMA converter requirement is less than 2 W and the actual measured dissipation is in the range 1.35 to 1.45 W (see Table 1). This dissipation does not change for sampling clocks above the nominal 4 GHz setting (our converter can be operated up to 5 GHz clock). Most of the dissipation comes from the comparators, clock amplifier and DFFs.

A comparison of the VEGA 1 design with existing commercial devices around 1 Gsps show that our ADC

exhibits good performances in the Power/Frequency domain (see red dot in Fig. 18). Some converters are working up to 10 Gsps (pink dot in the upper right of Fig. 18 and ref. [12]) but still exhibit relatively high dissipation while the ALMA ADC works up to 5 GHz but with significantly lower dissipation.

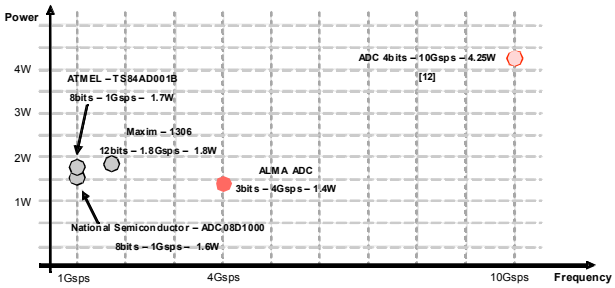

Fig. 18. VEGA 1 chip (red dot at 4 GHz) and high speed commercial ADCs. The VEGA 1 converter can be operated up to 5 GHz

Production acceptance tests of the ALMA ADC have been performed with the industrial equipment also used for the ALMA demultiplexer chips (see [3]). The first step in the validation procedure consists in checking the currents in all blocks of the ALMA chip with the ST Microelectronics tester. In a second step, the toggling rate of all converter LVDS outputs is checked using the low frequency clock stage (around 800 MHz) built in the chip. Finally, both static tests and dynamic tests (for long DTE integrations) are performed in our laboratory as described in Section 4 with chips assembled on the ALMA PCBs.

6. Ongoing work on fast ADCs

In addition to the designing, prototyping and testing tasks presented here for the ALMA production, our team has designed and prototyped with the same SiGe technology another chip very similar to VEGA 1. This chip has been tested in an ALMA digitizer assembly with existing ALMA demultiplexer chips to demonstrate that the power dissipation in the DFF and clock amplifier blocks could be lowered to reach a total chip dissipation of about 1W. Only a few of these chips have been produced.

Our team is also working on a System On Chip (SOC) approach which consists in porting our converter and demultiplexing chip designs to a single circuit. By merging our 3-bit ADC and the 3 demultiplexing chips (one for each bit) into a single circuit our goal is to offer a less than 5mmx5mm circuit in a 256-pin BGA package. If the demultiplexing stage would be 1:8 instead of 1:16 we would need a 196-pin package. The SOC design would then further reduce the total power dissipation of samplers and integrated demultiplexers to around 3 W or less because, in particular, the converter output buffers would not be required anymore.

We are also preparing a multichip approach (System In Package or SIP) for the existing and individually packaged converter and demultiplexing chips in order to improve the ALMA digitizer assembly in terms of cost and maintenance and for other applications.

7. Conclusions

We have briefly described the design of the ADC custom chip which has been selected for the ALMA production (VEGA 1 chip) and we have presented some of the assembly tests and performances of this new chip. Three major goals have been achieved for the VEGA 1 design, low power dissipation (~ 1.4 W), high speed conversion (up to 5 GHz clock) and signal input adaptation up to 4 GHz. To diminish the development time required for the ALMA ADC production, and because of technology compatibility reasons, we have used the SiGe technology which was successful in our previous high speed demultiplexers and first 2-bit ADC designs. After extensive simulations, design validation tests have been undertaken with several pre-production chips assembled on ALMA test boards. During these tests we have used a specially designed auto-correlator/FFT system and/or a digital test fixture including an ALMA correlator chip.

The industrial production of the packaged ADCs required for the ALMA project includes static and low frequency qualification tests based on simulations and laboratory qualification tests. Industrial testing is performed for all chips produced at the ST Microelectronics site before shipment to the assembler site.

Research work based on the ALMA converter and demultiplexer design and packaging continue and aim at integrating all chips in a single BGA packaged ASIC.

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