Development Upgrades of the Atacama Large Millimeter/submillimeter Array (ALMA)

Study Report

NRC TALON Frequency Slice Architecture Correlator / Beamformer (AT.CBF) for ALMA

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LIST OF ACRONYMS AND TERMS

ACA – Atacama Compact Array, a separate adjunct array of smaller antennas next to ALMA-B.

AFSP – ALMA Frequency Slice Processor.

AFSP-Part (or just FSP-Part) – The portion/partition of AT.CBF containing AFSPs.

AFSP-UNIT – The collection of TALON LRUs that form an AFSP, for AT.CBF this is notionally 4 TALON LRUs.

ALMA-B – The main ALMA array consisting of 50 x 12 m antennas, processed by the BLC.

ARTTA-4 – Advanced Radio Telescope Test Array-4 antenna.

AT.CBF – ALMA TALON Correlator/Beamformer.

AT.CDP – CDP for the AT.CBF.

ATD – Astronomy Technology Directorate of HAA.

BBC – Baseband Converter.

Beam-Channel – A particular VDIF-formatted stream/spigot VLBI beam out of AT.CBF.

BITE – Built-In Test Environment.

BLC – Baseline Correlator—the original/existing installed ALMA-B correlator.

CASA – Common Astronomy Software Applications.

CDP – Correlator Data Processor, of the BLC.

CDR – Critical Design Review.

COTS – Commercial Off-The-Shelf.

CRD – ALMA Central Reference Distributor.

CRG – ALMA Central Reference Generator.

CSPPFB – Critically Sampled Poly-Phase Filter Bank.

CSP_Mid.LMC – The M&C software layer between TM and Mid.CBF in the SKA1 Mid telescope.

CTR – Central Timing Reference.

DCLC – Direct Contact Liquid Cooling wherein liquid coolant flows through a plate that is thermally coupled to a device to be cooled.

DDC – Direct Digital down Conversion.

EMC – Electro-Magnetic Compatibility.

EMI – Electro-Magnetic Interference.

ESD – Electro-Static Discharge.

EVLA – Expanded Very Large Array; after commissioning re-named the Jansky VLA (JVLA.)

FFX – Generally refers to a correlator architecture wherein there is a 2-stage Fourier Transform followed by multiply/accumulate.

FIR – Finite Impulse Response (filter.)

FinFET – 3D Field Effect Transistor technology.

FPGA – Field Programmable Gate Array.

Frequency Slice – The name given to a ~200 MHz coarse channel in the FSA.

FSA – Frequency Slice Architecture.

FTE – Full-Time Equivalent.

Function Mode – The configured operating mode of an AFSP, either "Imaging Correlation" or "VLBI Beamforming".

HAA – Herzberg Astronomy and Astrophysics. The NRC Research Center whose purpose is astronomy and astrophysical science and development of technology and instrumentation for observatories that Canada has an interest in.

HIL – Hardware In the Loop.

HPBW – Half-Power Beam Width.

HPS – Hard Processor System, the multi-core embedded ARM processor in the Intel Stratix-10 FPGA on the TALON-DX board.

IP – Intellectual Property.

JSON – JavaScript Object Notation.

LRU – Line Replaceable Unit.

LSB – Least Significant Bit.

LSTV – Long Sequence Test Vectors.

LVDS – Low Voltage Differential Signaling.

MBO – Mid Board Optical.

Mid.CBF – SKA1 Mid Telescope Array Correlator/Beamformer.

M&C – Monitor and Control.

MM – Multi-Mode (fiber.)

MTP-x – A trademark of US Conec for a version of the MPO (Multi-Fiber Pull Off) connector with improved specifications. "x" indicates the number of fibers in the connector (if present), normally a multiple of 12.

NFS – Network File System.

ngVLA – Next Generation VLA.

NRC – National Research Council of Canada.

NRE – Non-Recurring Engineering (costs.)

NRZ – Non-Return to Zero wherein one symbol contains 2 levels or 1 bit of information.

NTP – Network Time Protocol.

OSF – Observation Support Facility (for ALMA.)

(VCC-) OSPPFB – Over Sampling Poly-Phase Filter Bank.

OTB – Observation Time Block. For the purposes of this report, and contiguous swatch of time during which the AT.CBF configuration, for a particular sub-array, doesn't change.

PAM4 – 4-level Pulse Amplitude Modulation, wherein one symbol contains 4 levels or 2 bits of information.

PDU – Power Distribution Unit.

PPS – Pulse Per Second.

Processed Bandwidth – The bandwidth that AT.CBF processes and outputs to the ALMA Archive for science use.

RFI – Radio Frequency Interference, referring to signals in the data streaming from antennas that AT.CBF must process.

SERDES – Serializer/Deserializer. Implied with this is a CDR—Clock Data Recovery Phase-Locked Loop wherein the receive clock is derived from the serial data.

SFDR – Spurious Free Dynamic Range.

SFP+ -- Small Form Factor Pluggable; "+" means 10 Gbps.

SKA(1) – Square Kilometre Array (phase 1.)

SM – Single Mode (fiber.)

SSR – Super Sample Rate.

SSTV – Short Sequence Test Vectors.

TALON – The name, not an acronym, given to Mid.CBF and/or its technology.

TALON-DX – The circuit board assembly containing the Intel Stratix-10 FPGA; 2 of these are contained in a TALON LRU.

TALON/FSA – Loosely refers to the technology, physical architecture, and signal processing architecture of Mid.CBF.

TBC – To Be Confirmed.

TBD – To Be Defined.

TCD – Timecode Distribution.

TDC – TALON Demonstration Correlator.

TOR – Top Of Rack.

UDP/IP – User Datagram Protocol (over) Internet Protocol.

UTC – Universal Coordinated Time.

VCC – Very Coarse Channelizer, although this generally refers to the first stage coarse filterbank and associated circuitry of AT.CBF.

VCC-Part – The portion/partition of AT.CBF containing VCCs.

VCC-UNIT – A convenient collection of TALON LRUs in the VCC-Part; for AT.CBF this is notionally 5 TALON LRUs.

VDIF – VLBI Data Interchange Format.

VLA – Very Large Array.

VLBI – Very Long Baseline Interferometry.

VTP – Verification Test Plan.

VTR – Verification Test Report.

WIDAR – Name of the JVLA (EVLA) correlator.

Zoom Window – a tunable width and placement portion of bandwidth (within a Frequency Slice) in AT.CBF.

ACKNOWLEDGEMENTS

We would like to thank Alejandro Saez of the ALMA program office for visiting us at NRC-Penticton in February 2020 to provide us with insight into ALMA systems and operations, as well as being kind enough to review and provide feedback on this report.

1 Executive Summary

This report contains the results of an investigation into the feasibility, cost, and impact on existing ALMA systems of utilizing NRC's Frequency Slice Architecture (FSA) and TALON technology ("TALON/FSA") for a new ALMA correlator and VLBI beamformer.

The NRC TALON/FSA is designed for the SKA1 Mid telescope Correlator/Beamformer ("Mid.CBF") but has the flexibility to be used for wideband medium-N (N: number of antennas) radio telescopes and ALMA falls into this category. As such, the design and costing is very mature, supported by ~60 person-years of Mid.CBF development effort including detailed signal processing modeling and development, prototype design, fabrication, and testing, and multi-layer software design and specification—all within the framework of a formal systems engineering approach.

Thus, a TALON/FSA correlator and VLBI beamformer for the ALMA telescope can be available and deployed within a ~5 year horizon[1] to replace the BLC, meet ALMA 2030 goals of at least 2X bandwidth, and, we believe, is future-proof in its physical/electrical architecture and signal processing approach to provide ALMA with a foundation to build on for years to come. By upgrading the ALMA correlator to AT.CBF now, not only will it provide much-improved science capability in the near term, but it will position ALMA to provide uninterrupted science operations whilst transitioning to upgraded ALMA 2030 antennas, a process that will take several years[2].

A new ALMA TALON Correlator/Beamformer ("AT.CBF"), described in considerable detail in this report, will vastly improve ALMA likely well before ALMA 2030 bandwidth upgrades come into effect. The key capabilities of an AT.CBF are as follows:

- No sensitivity losses of any significance (i.e. << 1.5%) with ≥ 8-bit data paths and 6-bit correlation.
- ~14 kHz correlated[3] spectral channel bandwidth, with contiguous linearly-spaced channels across the full digitized bandwidth, with ~60 dB channel-to-channel isolation and > ~80 dB of spurious-free dynamic range (SFDR) provided by a modern poly-phase filterbank design and NRC signal processing innovations [1].
- Correlated spectral channel bandwidth, down to ~200 Hz, on at least 48 tunable (width & center frequency) Zoom Windows.
- Sideband separating correlation.
- At least 80 antennas. Thus, the AT.CBF is capable of correlating all ALMA-site antennas.
- Virtually perfect delay and phase tracking requiring no post-correlation corrections.

[1] From start of funding.
[2] As noted by Brogan at the ALMA correlator workshop, February 2020, in Charlottesville. Also, see Brogan's talk entitled "A Straw ALMA2030 Deployment Plan", presented at the conference (https://osf.io/6wc8f/).
[3] Throughout this document, unless otherwise stated, bandwidths are always "per-polarization", all 4 Stokes visibilities are always produced from the correlator, and both polarizations are always beamformed.

- For each sub-array independently, each ~200 MHz of correlated bandwidth (or Zoom Window) can optionally be on a different delay-center on the sky; as well, the same bandwidth can be on multiple delay centers.
- Concurrent 1600 MHz of VLBI beamforming bandwidth; up to the full ALMA bandwidth by trading-off correlated bandwidth, or by adding more hardware than costed here. Many independent beamforming delay centers on the sky, independent of correlated delay-centers, are possible.
- Any number of sub-arrays, with a practical limit being ~16 (same as SKA1 Mid.CBF.)
- No practical limitation in baseline extent (i.e. up to 10,000 km.)
- "FFX" architecture easily expandable in bandwidth.

Key deliverables defined in the Proposal (section 5.1, clause 2.) require study of AT.CBF interfaces with, and impacts on, existing ALMA systems. These are summarized below:

- The existing ALMA observer/observation preparation tool is intimately integrated and tuned to the existing ALMA Baseline Correlator's (BLC) capabilities and is therefore incompatible and not capable of being used to set up or utilize the AT.CBF in any fashion. Thus, this front-end software and any associated ALMA online observing control and set up software that is tuned to the BLC, must be entirely replaced. Observer/observation preparation software for AT.CBF is not examined or costed in this report. However, its implementation should be reasonably straightforward; it produces observation block JSON scripts offline, subsequently fed by the existing or modified ALMA online controller/executor, at scheduled times, to AT.CBF for execution.
- As will be described in detail, the AT.CBF will directly integrate into the existing real-time hardware interfaces, including:
    - Digitized data on fiber from antennas (12 fibers for each antenna), optimally fusion-spliced to MTP-12 single-mode fiber connectors at the AT.CBF-to-antenna interface boundary.
    - The 125 MHz reference.
    - The 48 msec reference.
    - Streaming VLBI beam outputs in VDIF format, via one or more Ethernet connections.
- The existing BLC Correlator Data Processor (CDP) compute cluster back-end will be replaced with a new AT.CBF "AT.CDP" compute cluster and software. AT.CDP converts native AT.CBF-produced visibilities, already in the frequency domain, as well as meta-data, to ALMA CASA data sets transmitted to the ALMA Archive on one or more Ethernet interfaces. CASA data set formats are flexible enough to handle the full capabilities of AT.CBF and thus there are no essential modifications to CASA or its input data format required.

- The Monitor and Control (M&C) interface to AT.CBF is via Ethernet, with the existing or modified ALMA online controller/executor providing AT.CBF with observation block JSON scripts for execution.
- Whilst not essential, it is likely prudent that the AT.CBF be located at the OSF rather than the high-site since doing so will not interrupt existing ALMA operations. There, cooling systems design, on-going maintenance, and operations are simpler and cost less.
- An AT.CBF that correlates the existing ALMA bandwidth plus 1600 MHz of VLBI beamforming is implemented in an estimated total of 10, 19" standard COTS racks and ~100 kW of power; a 2X bandwidth correlator, plus 3200 MHz of VLBI beamforming, requires an estimated total of 19 racks and ~200 kW[4] of power. These can be air-cooled; however, to minimize total system power consumption (AT.CBF power and cooling power), Direct Contact Liquid Cooling (DCLC) is recommended although details of such is not contained in this report. The TALON 2U air-cooled enclosure design is easily migrated to a DCLC design, requiring only a new rear panel and customized liquid cooling plates (complete with dry connect/disconnect hoses) obtained from the DCLC solution supplier. Other COTS items such as Ethernet switches and rack-mount computers could be migrated to DCLC, although for simplicity it is likely most prudent to keep them air-cooled since their total power dissipation is relatively small.

The AT.CBF design and costing contained in this report takes advantage of the existing advanced development and synergy of SKA1 Mid.CBF design, construction, and deployment to reduce its cost to the ALMA observatory.

Using this synergy, an existing bandwidth replacement correlator/beamformer is estimated to cost $13.5M USD[5] (including a ~$1.6M contingency); a 2X bandwidth ALMA 2030 AT.CBF is estimated to cost $19.5M USD (including a ~$2M contingency.)

These numbers include additional AT.CBF FTE effort over and above that for SKA1 Mid.CBF of ~19 person-years and assume that the TALON technology of today (planned for deployment for SKA1 Mid.CBF) is used for both. Likely an ALMA 2030 AT.CBF upgrade will use newer-generation hardware, in whole or in part, requiring additional NRE at that later date to develop/port FPGA designs to the new technology.

If the synergy with SKA1 Mid.CBF development doesn't occur (i.e. if SKA1 Mid.CBF construction funding is not obtained) another ~$4.4M USD in NRE is required.

[4] Assuming that the current Mid.CBF Intel Stratix-10 FPGA technology is used; likely newer technology will be used for ALMA 2030 bandwidth, with some reduction in power dissipation. See section 11.2 for further discussion.
[5] For 0.84624 USD c/w the Euro.

2 Introduction

The NRC SKA1 Mid telescope correlator & beamformer ("SKA1 Mid.CBF") has been under development for the past several years as one of many projects in the SKA1 pre-construction phase. Mid.CBF passed a CDR in March 2018 and since then further work on development in the so-called "bridging" phase has, and continues to, occur. Significant work has gone into the effort up to the CDR, estimated at ~60 person-years, and such work included system engineering (requirements & interfaces definition, test and verification planning), hardware/software/firmware prototyping, system design, non-functional design and analysis (e.g. reliability), as well as detailed development and cost estimation. In short, the effort up to the CDR was a design and de-risking exercise so that the costs of construction and deployment have a high confidence level, needed to ensure that the "ask" for SKA1 construction is well-supported.

The implementation of the Mid.CBF design is not complete; much work is required in the formal construction phase for development, testing, and deployment. This work includes development of a TALON Demonstration Correlator (TDC) for early AA0.5 SKA1 Mid deployment, scheduled to be on-site in mid-2023. An instance of a 4-antenna, 800 MHz TDC will also be used for the NRC-funded Advanced Radio Telescope Test Array-4 ("ARTTA-4") on the same timeframe, wherein 4 antennas of the NRC-Penticton synthesis telescope will be outfitted with a new 400-800 MHz and 900-1800 MHz dual-band feed, receivers, Direct Digital Conversion (DDC) digitizers, and the TDC to on-sky test a new all-digital method of clock & timing, something being considered for the ngVLA (see Carlson and Shillue's talk at: https://ngvla.nrao.edu/page/tech-talks.) Thus, significant and on-going development and de-risking of the TALON/FSA design is in progress.

The Mid.CBF design is for the Mid telescope, consisting of ~200, 12 m[6] and 15 m antennas, with an aperture extent of ~160 km, located in South Africa. Mid.CBF must correlate up to 5 GHz/pol, handle multiple different Bands and bandwidths, as well as produce beams for pulsar searching, pulsar timing, and VLBI, all within a hostile RFI environment. Thus, Mid.CBF signal processing and electrical/physical architecture is designed for a low-to-medium "N" (i.e. number of antennas) telescope array with a significant bandwidth to be correlated and a significant number of beams to be produced. ALMA is in this category. In 2018 the Mid.CBF design was also used by NRC, at NRAO's request, as a basis to develop a reference correlator/beamformer design for the ngVLA [2].

The Mid.CBF design makes use of modern electronics, namely Intel's Stratix-10 14 nm FinFET transistor technology, high-speed 25G/100G serial and fiber optics technology, and modern signal processing techniques to produce high-quality visibility channels and beamformed output data products. As such, Mid.CBF is capable of processing significant bandwidth at a reasonable cost and power, compared to previous technology nodes.

What follows is a design study into a new ALMA correlator/beamformer, which we call the "ALMA TALON Correlator/Beamformer" (AT.CBF), highly leveraging the funding and work that has gone into the SKA1 Mid.CBF design. Thus this study, although a "paper exercise", yields results that are very well investigated and supported on a number of fronts, much more so than the funding for an ALMA development study on its own would yield. As such this AT.CBF design, with references to key SKA1

[6] MeerKAT antennas, which will become part of the Mid telescope array and will be processed by Mid.CBF.

Mid.CBF documents that took an enormous effort to produce, is very mature and close to the CDR stage[7].

[7] As defined by the SKA Organization, for systems like Mid.CBF where a mixture of prototyping, design, and analysis of critical and cost-driving aspects is appropriate.

3 Study Approach

In the first phase of the study we investigated existing ALMA systems, the Baseline Correlator (BLC), and interfaces to it to determine the appropriateness of the fit of the TALON/FSA technology to the problem. Some of this was known a priori; NRC has a long-standing involvement in ALMA and the primary author of this report (Carlson) was the chair of the NRAO ALMA correlator CDR in the fall of 2003 and so had some knowledge of the BLC design and interfaces to it.

Further research was undertaken (with the kind assistance of ALMA and NRAO personnel) to gather and examine pertinent ALMA documentation, namely ALMA memos 070, 287, 385, 537, 556, and 565, as well as the "ALMA Cycle 6 Technical Handbook" [3], the ALMA System Block Diagram [4], and the document "Scientific Specifications and Requirements for the Next Generation ALMA Correlator", Draft version, June 30, 2016 authored by Rupen, Baudry, and Lacasse (it is from this memo that we settled on costing an 80-antenna AT.CBF in this report.)

Next, rather than visit the ALMA site to "see for ourselves" (our original plan), we took advantage of the coincidence of "The ALMA2030 Vision: Design Considerations for the Next ALMA Correlator" workshop, held in Charlottesville February 11-13, 2020, to invite Alejandro Saez—ALMA BLC support/maintenance engineer—to our NRC facility in Penticton for a few days before the workshop to gather further first-hand understanding of the ALMA BLC, interfaces, and surrounding infrastructure. Alejandro was kind enough to accept our invitation and over the period of 3 days of meetings and discussions we were able to obtain further detailed understanding of appropriate systems, gain an appreciation of his depth of knowledge of ALMA, and convey to him what a new AT.CBF correlator might look like and how it works.

Finally, leading up to, and at the workshop, we had discussions with several NRAO staff to obtain further understanding of the BLC and ALMA, primarily with Dr. Crystal Brogan, the North American ALMA Program Scientist. Dr. Brogan provided us with further insight into the development and political structure of the ALMA organization and assurance that the observer/observation preparation front-end—which we understand is a European ALMA responsibility—would have to be replaced along with a correlator replacement, something we had largely concluded by examining ALMA memo 556.

In the next phase, we developed an AT.CBF signal processing and technology/implementation architecture that, as closely as possible, aligned with the SKA1 Mid.CBF design, bearing in mind the hardware interfaces to ALMA that the AT.CBF would need. The impact of doing such was enormous since by doing so we could minimize the design and testing delta for an ALMA correlator/beamformer and we could confidently rely on the ~60 person-years of engineering that went into Mid.CBF to inform the AT.CBF design and costing presented here. This phase entailed some re-jigging of the physical connectivity of the TALON/FSA design for the AT.CBF as well as modeling and testing of a key AT.CBF ingest signal processing block to convert ALMA sampled data to Mid.CBF sample rates. The utility of doing this meant we could use Mid.CBF processing for the rest of the processing pipeline primarily with the exception of the cross-correlation component, requiring a sideband separating design and a smaller (i.e. 80 vs 200) antenna correlation matrix, although it is still based on the Mid.CBF correlator design.

The final phase, of course, is this report, we believe containing enough detail to fully understand the capability, design, technology, and cost of the AT.CBF as well as the enormous boost in science capability that it could bring to the ALMA observatory.

4 Overview

4.1 Context diagram, interfaces, and infrastructure overview

A context block diagram of the AT.CBF and interfaces, including the AT.CDP, is shown in Figure 4-1 below. Some discussion of the details of the interfaces to the AT.CBF is provided here, with further details contained in section 5.3.

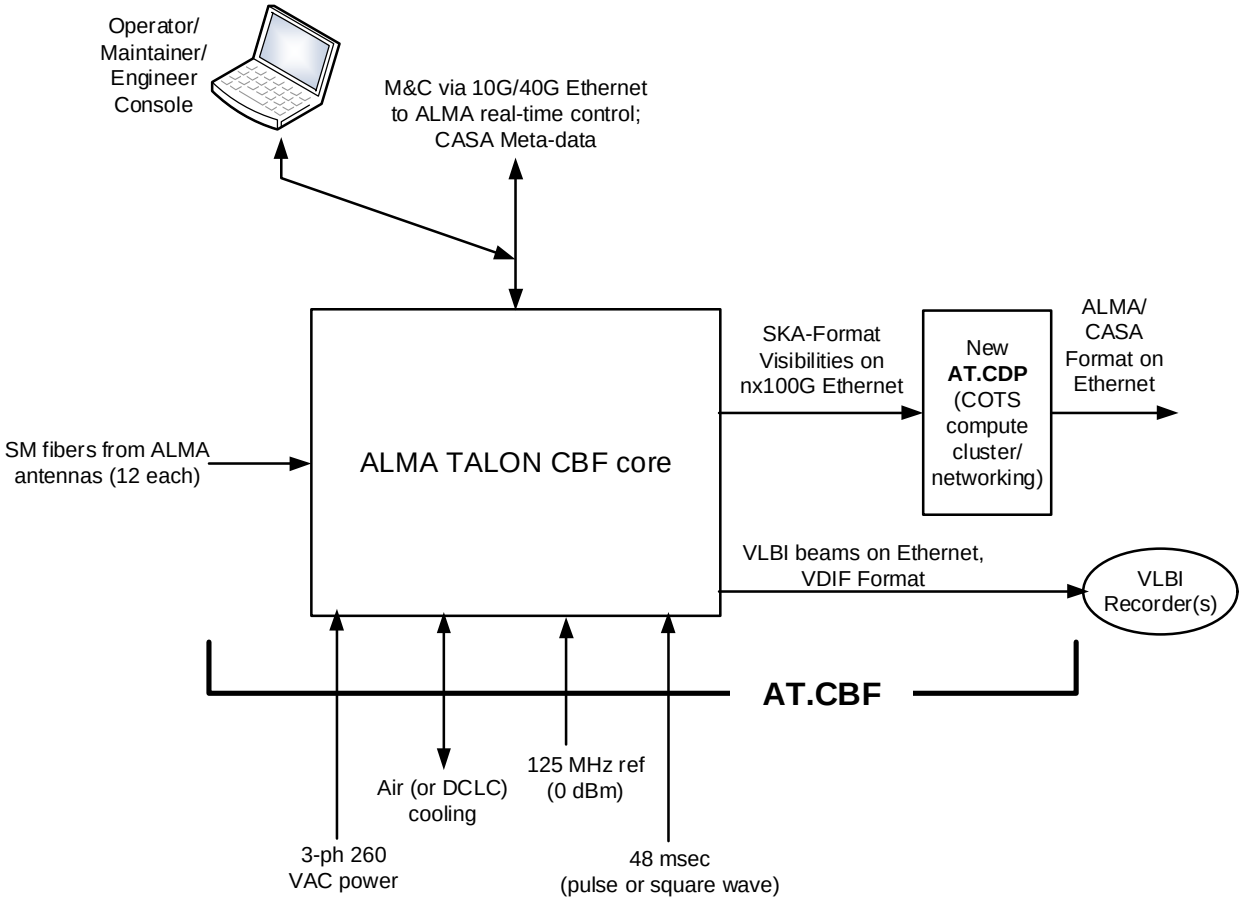

Figure 4-1 ALMA AT.CBF context diagram showing all crucial interfaces.

The 125 MHz reference sources from the ALMA Central Reference Generator (CRG 55.03 [4], sheet 4) and its input to the AT.CBF is via a single-ended coaxial connector. The 48 msec sourcing from the Central Reference Distributor (CRD 55.02 [4], sheet 4) also is input to the AT.CBF via a single-ended coaxial connector and so the native 48 msec LVDS signal on a twin-ax connector will need an LVDS-to-single-ended converter (not shown.) If desired, a redundant 125 MHz and 48 msec can be fed into the AT.CBF and distributed internally for 1+1 fault-tolerant operation. Internally, AT.CBF forms a "Timecode" signal that is native 1PPS-based—this internal 1PPS will be formed by capture of the 48 msec[8] and associated time-tagging via an ALMA NTP server (existing or added), knowing that the 48 msec and 1PPS are coincident every 6 seconds (surmised from CRD 55.02 [4].) Internal AT.CBF logic will

[8] And subsequent flywheel/checking. i.e. we assume that the 48 msec pulse has some jitter compared to the 125 MHz reference and include logic to avoid timing hiccups/jumps.

then develop the 48 msec where needed for 48 msec-aligned operations, but generally AT.CBF operates on 1PPS and internally-generated 10 msec boundaries for all delay and phase model application and data product timestamping[9].

There are 12 single mode (SM) fibers from each ALMA antenna, 3 for each BBC polarization pair, at ([3], Chapter 5) (4 Gs/s x 3b/sample x 2)/3 = 8.0 Gbps each[10] operating at a 1.5 µm optical wavelength[11]. The protocol on the fiber contains a Meta-Frame bit that is 1 on each 48 msec epoch [5], thus 48 msec time ticks flow with the data from the antennas to the correlator. Each of these sets of 3 fibers for a particular antenna route to a Quadrant in the BLC, but for AT.CBF, all 12 fibers route to a single place, namely an MTP-12 fiber input to the TALON LRU (Line Replaceable Unit) (see section 7.2, Figure 7-17.) Thus, fibers will be routed to AT.CBF from the FOAD 54.05 modules AMB14, AMB23, and AMB29 (for ACA antennas [4] sheet 4.) It is not clear whether fiber cables to these modules will simply be replaced or cut and fusion-spliced to an MTP-12 fiber connector for input to the TALON LRU. Internally, in the TALON LRU the 12 single-mode, λ=1.5 µm fibers go through an Optical (media) Converter (see Figure 7-6) to convert, via COTS 10GBASE-ER SFP+ modules (such as the Cisco SFP-10GER-55, λ_rx=1260-1600 nm) to multi-mode for ingestion into the TALON-DX FPGA board's Mid Board Optical modules (MBOs.) If the AT.CBF is located at the OSF, then a different antenna digitized data access method may be developed to stay within the site-to-OSF fiber capability.

For Monitor and Control (M&C), there is a 10G or 40G Ethernet connection from the ALMA online real-time controller(s) to an AT.CBF internal network switch. This switch connects to the AT.CBF Master control computer, a Top of Rack (TOR) network switch in each AT.CBF Signal Processing Rack, and the AT.CDP (not shown.) AT.CBF observation block execution JSON scripts, delay models, CASA meta-data (not required in the correlator core, but needed by the AT.CDP to form complete CASA data sets), and monitor data flow across this connection. Also, maintenance/engineering console GUI access to TALON-DX FPGA embedded processors occurs via this connection, communicating to AT.CBF TANGO [6] devices via TANGO messages.

Visibilities produced by the AT.CBF are output on multiple TBD 100G Ethernet ports in native SKA1 visibility format. These, along with meta-data, are converted in real time to ALMA CASA data sets by the AT.CDP cluster and transmitted to the ALMA Archive on TBD Ethernet data links.

The AT.CBF, when configured, forms VLBI beams at sample rates from 2 Msps, 4 Msps, ..., to 256 Msps, and then for the widest single contiguous bandwidth, 448 Msps [7], in VDIF format available on one or more 40G or 100G Ethernet output data links. The 2-256 Msps outputs provide up to 128 MHz of contiguous bandwidth, tunable within a TALON/FSA 200 MHz "Frequency Slice" (see section 6.1.3), the center ~90% of which is science-quality data, containing no aliased spectral content of any significance. The latter 448 Msps provides the entire 224 MHz over-sampled Frequency Slice, with the center 200 MHz containing un-aliased science-quality bandwidth. The 448 Ms/s sample rate is not "VLBI standard" per se, but a capable poly-phase filterbank in the VLBI correlator can process this sample rate to produce channels that can be correlated with channelized VLBI-standard data rates from other VLBI

[9] For sideband separating correlator dumps, alignment to the 48 msec Walsh switching cycle is performed.
[10] Of sampled data; exactly 10.0 Gbps total bit rate per fiber Error! Reference source not found..
[11] The digital fiber optic transponders for ALMA and the EVLA are the same, both operating at λ=1.5 µm (verified by Alejandro Saez, email communication to B. Carlson, July 16, 2020 and data sheet for the RX192DL PIN receiver module from Kerry Shores, NRAO-Socorro, May 2019).

antennas. Internally, all-digital re-sampling operations provide these output data rates so there is no temporally-varying signal degradation as would happen if analog conversion methods were used.

AT.CBF TALON hardware is contained in COTS "Signal Processing Racks" and powered by 3-phase 230VAC power. Each Signal Processing Rack contains dual Ethernet-controllable COTS Power Distribution Units (PDUs), which distribute redundant AC power to each TALON LRU's 1+1 redundant AC-to-DC power supply. M&C and AT.CDP racks are similar, with AC power provided to all COTS compute server and network switch units. If needed, TALON LRUs' mains AC power supplies are plug-in COTS units (see Figure 7-15) and have a 48VDC compatible plug-in unit. Thus, 48VDC mains power for Signal Processing Racks' equipment is possible, but not studied in any detail here.

The AT.CBF TALON LRUs are natively air-cooled (as in SKA1 Mid.CBF), however Direct Contact Liquid Cooling (DCLC) may be better and provide lower total system power operation, although engineering and study of this option is not contained in this report. Technology similar to that used in CHIME [17] might be used. The AT.CDP, M&C servers, and Ethernet switches are natively air-cooled—since their power dissipation is relatively minor, likely air cooling is the most prudent cooling option for them.

Signal Processing Racks are standard COTS 19" server racks[12] with a foot-print of 600 mm W x 1070 mm D x 1991 mm high. AT.CDP and M&C server/network switch "Control Processing Racks", estimated to be quantity=2 of them, are the same size. Mains (AC) power is supplied to all racks via under-floor 3-ph AC plugs, with 1+1 redundant rails if desired, with all fiber and network cabling provided to them via overhead cable trays. Cold air delivery/hot air removal is via cold (front) aisle and hot (rear) aisle airflow, where airflow to all racks is front-to-back via TALON LRU and COTS server & switch built-in fans.

The existing bandwidth correlator replacement AT.CBF, AT.CDP, and M&C requires a total of 10 server racks[13]. Double-bandwidth requires 19 server racks.

4.2 Data flow and signal processing overview

The AT.CBF signal processing architecture, as mentioned, is largely the same as SKA1 Mid.CBF for the reasons previously stated. This is the NRC "Frequency Slice Architecture" (FSA), developed to minimize the cost of dealing with the variety of sample rates, bandwidths, and science processing requirements of the SKA1 Mid telescope.

At its core, though, the FSA is really a 2-stage oversampled poly-phase filterbank "FFX" correlator. For ALMA, with all Bands being digitized at the same sample rate, the utility of the FSA is not as evident, although it is a nice fit for ALMA and provides some key additional capabilities that may find utility, namely the ability to trade-off bandwidth for independent delay centers on the sky, correlated vs VLBI beam-formed bandwidth trade-offs, and the inherent ability to transition to upgraded bandwidths and technologies. This latter capability is important for a living instrument such as ALMA.

A simplified data flow and signal processing block diagram of the AT.CBF, including the AT.CDP back-end, is shown in Figure 4-2.

[12] Further investigation is needed to determine if these "standard" server racks, with possible modifications to them, can meet ALMA seismic zone 4 requirements or if other racks are required.
[13] Depending on AT.CDP computing performance requirements; assume here that the AT.CDP occupies 1 rack in the replacement bandwidth AT.CBF and 2 racks in the 2X bandwidth AT.CBF.

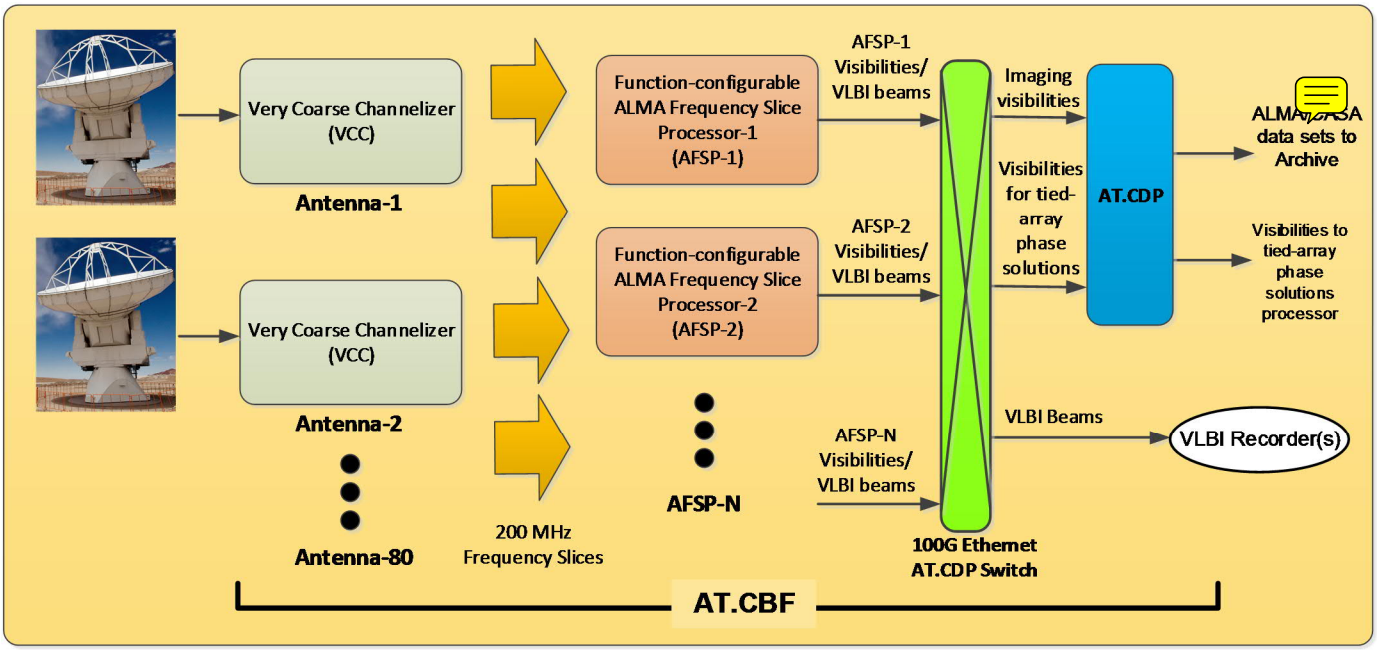

Figure 4-2 Simplified AT.CBF data flow and signal processing block diagram.

Digitized data flows from ALMA antennas to Very Coarse Channelizers (VCCs) where bulk integer delay in units of integer samples is applied to the wideband (4 Gs/s) data before it is channelized into 10/9 x 200 MHz ~= 220 MHz over-sampled frequency channels referred to as "Frequency Slices" (FS.)

Frequency Slices are then fed, via a passive optical cross-connect, to ALMA Frequency Slice Processors (AFSPs) (qty=24[14]—existing bandwidth; qty=48—2X bandwidth, costed here)[15] where for imaging correlation, final fractional delay (+/-0.001 sample—see section 6.1.2) and phase compensation occurs followed by optional Zoom Window selection, fine channelization, and cross-correlation. Each AFSP processes two Frequency Slices, each of which is any select Frequency Slice (i.e. there is no requirement that they are adjacent slices.)

For VLBI beamforming, final delay and phase compensation, re-sampling to VLBI data rates, and beamforming summing occurs. Also for VLBI, to allow for independence of VLBI beamforming delay centers on-the-sky, further (medium-fine) channelization and cross-correlation occurs to produce visibilities needed for calculating tied-array solutions for VLBI beam coherence, done so that imaging AFSPs don't need to be used for determining VLBI tied-array solutions. See section 6.1.3 for further details.

All visibility and beamformed data products go through an output Ethernet AT.CDP Switch, directed either to the AT.CDP for format conversion and merging with meta-data, or output to a VLBI recorder. Finally, the AT.CDP produces ALMA/CASA data sets for the Archive and with a similar or trimmed format,

[14] Up to 44 by adding 20 more AFSPs and using all available TALON-DX optical interconnects.
[15] These quantities are chosen to allow for 1600 MHz (3200 MHz; 2X bandwidth system) of concurrent VLBI beamforming bandwidth or with up to 8 (16; 2X bandwidth system) Zoom Windows concurrent with full digitized bandwidth correlation.

to external equipment (not part of AT.CBF) that calculates tied-array phase solutions for feedback into AT.CBF to achieve VLBI beam coherence.

Each AFSP may be configured for a different "Function Mode" (FM.) For SKA1 Mid.CBF there are many Function Modes, but for ALMA only 2 are envisioned, namely "Imaging Correlation" and "VLBI Beamforming".

Within each AFSP there can be multiple independent sub-arrays[16] (up to 16 as previously mentioned), with the caveat that within each AFSP independently, all sub-arrays must be in one Function Mode of either:

- Imaging Correlation or,
- VLBI Beamforming, concurrent with medium-fine channel cross-correlation.

Furthermore, for Imaging Correlation Function Mode within each AFSP independently, for each Frequency Slice independently, each sub-array can be correlating standard-resolution channels OR zoom-window resolution channels, but not both.

Any Frequency Slice may be directed to any AFSP as illustrated in Figure 4-3. Since final delay and phase compensation (tracking) occurs in each AFSP independently[17], it allows for trading off Processed Bandwidth[18] (correlation, beamforming) for delay centers on the sky, as previously mentioned.

[16] Where a sub-array is defined here as an exclusive sub-set of ALMA antennas, where the subset is any number from 1 to all ALMA antennas.
[17] With the restriction that all delay centers must be within the primary beam of the antenna, because of the bulk delay in the VCC
[18] "Processed Bandwidth" is defined as the bandwidth delivered to external equipment for science use.

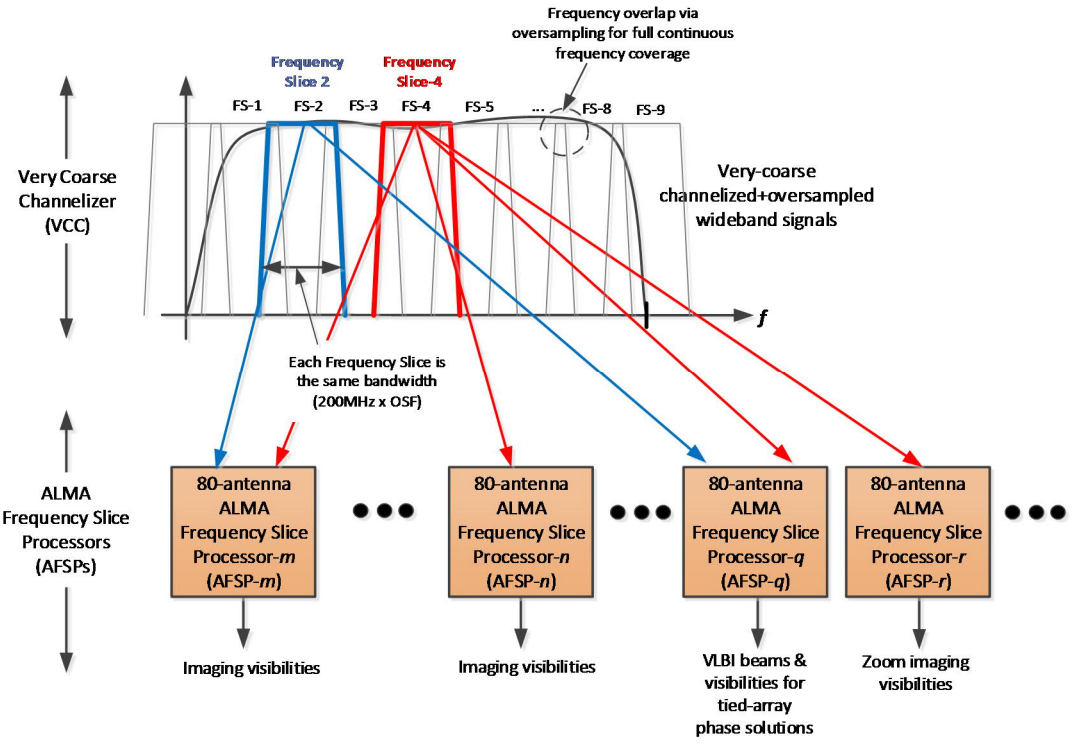

Figure 4-3 Frequency Slice distribution from the VCCs to the AFSPs—any 2 Frequency Slices, for all antennas, may be directed to any AFSP using internal circuit cross-connect switching built into the VCCs.

For Function Mode "VLBI Beamforming", TALON/FSA terminology defines a "VLBI Beam" as being a beam formed on a particular delay center on the sky, of whatever bandwidth desired from 1 MHz to the full digitized ALMA bandwidth available. A "VLBI Beam-Channel" is a particular beamformed sampled data streaming VDIF spigot derived from a VLBI Beam. Any particular VLBI Beam-Channel spigot has a sample rate of 2 Ms/s, 4 Ms/s, ..., 256 Ms/s, or 448 Ms/s, as previously mentioned.

To illustrate the flexibility and limitations of a TALON/FSA AT.CBF, an "FSP Explorer" Excel spreadsheet developed for Mid.CBF, has been modified/adapted for an existing bandwidth replacement AT.CBF, with two concurrent multi-subarray use cases for 24 AFSPs, shown in Figure 4-4 and Figure 4-5 below:

Subarray	Band	Continuum Imag BW (MHz)	# Zoom Windows	VLBI BW (MHz)	# VLBI Beams	Subarray N_imag_AFSPs	Subarray N_VLBI_AFSPs
1	3	8000.0	0	1600.0	4	20	4.000
2	4	0.0	40	1600.0	4	20	4.000
3	4	4000.0	20	1600.0	4	20	4.000
4	5	2000.0	30			20	0.000
5	9	0.0	40			20	0.000

Figure 4-4 Existing bandwidth replacement AT.CBF example use case 1.

Subarray	Band	Continuum Imag BW (MHz)	# Zoom Windows	VLBI BW (MHz)	# VLBI Beams	Subarray N_imag_AFSPs	Subarray N_VLBI_AFSPs
1	3	0.0	0	8000.0	4	0	20.000
2	5	0.0	8			4	0.000
3	9	1600.0	0			4	0.000
4	10	800.0	4	4000.0	2	4	10.000

Figure 4-5 Existing bandwidth replacement AT.CBF example use case 2.

There are 2 key driving factors in the design of SKA1 Mid.CBF signal processing blocks—amplitude dynamic range for RFI and spectral channel response characteristics, largely to restrict aliasing of strong narrowband RFI into other channels but also, of course, for spectral channel purity for spectral-line science. These determine how many bits/sample must be carried through the entire signal processing chain and the filterbank processing load. In short, these factors determine the fidelity of output data products and, indeed, of the telescope itself.

For AT.CBF, the RFI environment is likely less extreme than SKA1 Mid and some bit trimming affecting amplitude dynamic range—to save cost and power—has been done in the AT.CBF design compared to SKA1 Mid.CBF. This includes carrying 8+8b (rather than 16+16b) per sample from the VCC to the AFSPs; this, and the much smaller correlator size compared to Mid.CBF, leads to an AFSP processing two Frequency Slices, rather than one per FSP as in SKA1 Mid.CBF[19]. Similarly some trimming could be done for spectral channel response (e.g. less reject band attenuation), however doing so entails additional design effort than costed here. Thus, SKA1 Mid.CBF spectral channel responses essentially come with no additional NRE in the AT.CBF, but at some (low) cost in hardware and power.

The normal (i.e. not VLBI) Imaging Correlation standard and zoom spectral channel response extracted from [8] is shown in Figure 4-6, providing excellent reject-band attenuation and, with -3 dB channel-edge amplitude, seamless amplitude and phase coverage across the channelized bandwidth (i.e. the bandwidth into the filterbank.) This channel response, of course, is because a poly-phase FFT filterbank is used in the second "F" portion of the TALON/FSA "FFX" architecture. See section 6 for further details including other channel responses and the total end-to-end spectral response.

[19] Thus, throughout this document the term "ALMA FSP" (AFSP)—processing two Frequency Slices—is used to differentiate it from the SKA1 Mid.CBF FSP, which processes one.

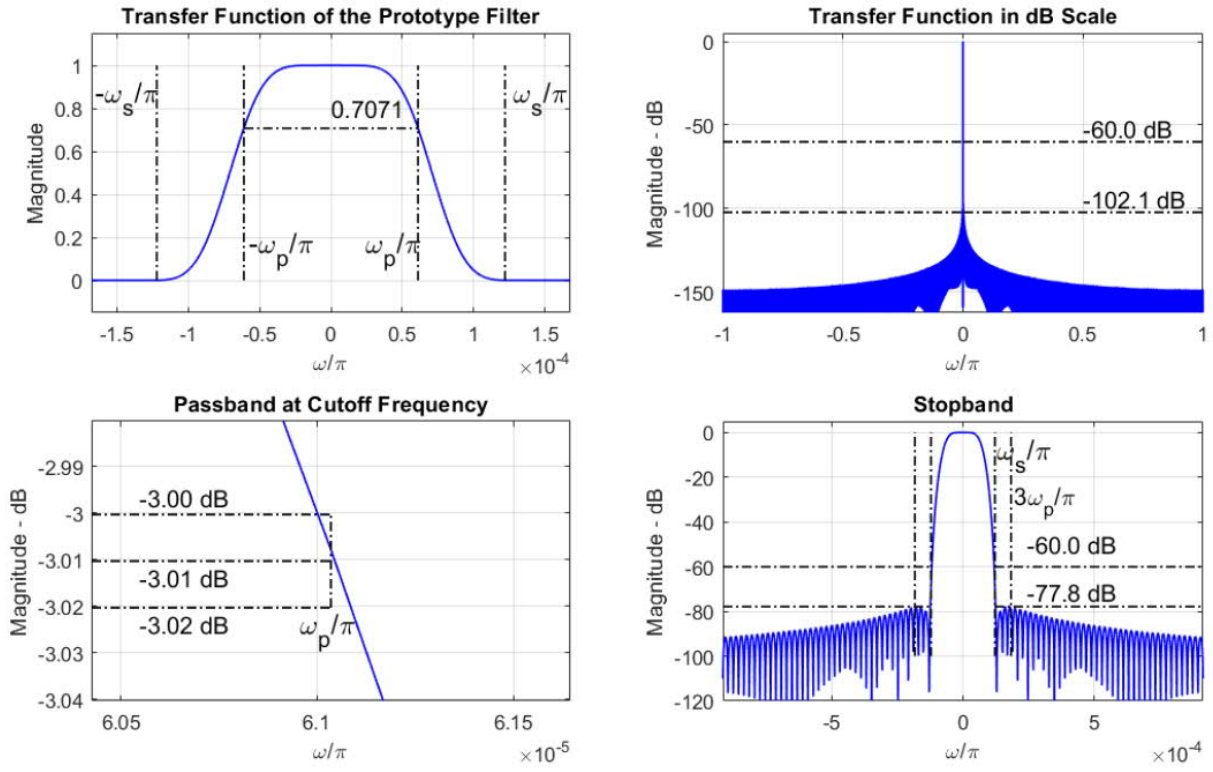

Figure 4-6 Normal (~14 kHz) imaging and zoom imaging spectral channel response. The channel passband is between $\boldsymbol{\omega/\pi}$=+/-0.5 x 10^{-4} (seen most clearly in the upper left panel.)

Another point worth briefly noting here is that in the AT.CBF, final delay and phase tracking—including fractional delay—occurs in the time domain on the 200 MHz Frequency Slice before the fine filterbank. Thus, there are no delay "clunks" (integer delay steps) propagating through the fine poly-phase filterbank(s)[20], which means there is no detectable delay-rate-dependent modulation artefacts in output visibilities. This also means that virtually any delay rate can be handled, such as that required for fast-slewing wide-field on-the-fly mapping, with no restriction on baseline extent.

4.3 Monitor and Control (M&C) overview

As with other aspects of AT.CBF, M&C[21] is largely copied from the SKA1 Mid.CBF design, with capabilities not required by AT.CBF pruned out. The entire AT.CBF M&C infrastructure is built on TANGO [6] messaging and devices, copying as much as possible from SKA1 Mid.CBF, with details in [7].

The "Primary Presentation" [9] of the "Command and Control" view for SKA1 Mid.CBF, extracted from [7], is shown in Figure 4-7. The view for AT.CBF is similar, with non-applicable pieces pruned out or pieces added that are specific to AT.CBF. (The number annotations next to the connecting lines in the diagram indicate the number of instances of each path, for SKA1 Mid.CBF.)

[20] As would occur if fractional delay was implemented with phase-delay after the fine filterbank.
[21] Throughout this document "M&C" generally refers to all aspects of "monitoring and controlling software". Specific facets of M&C are explicitly identified and defined where needed.

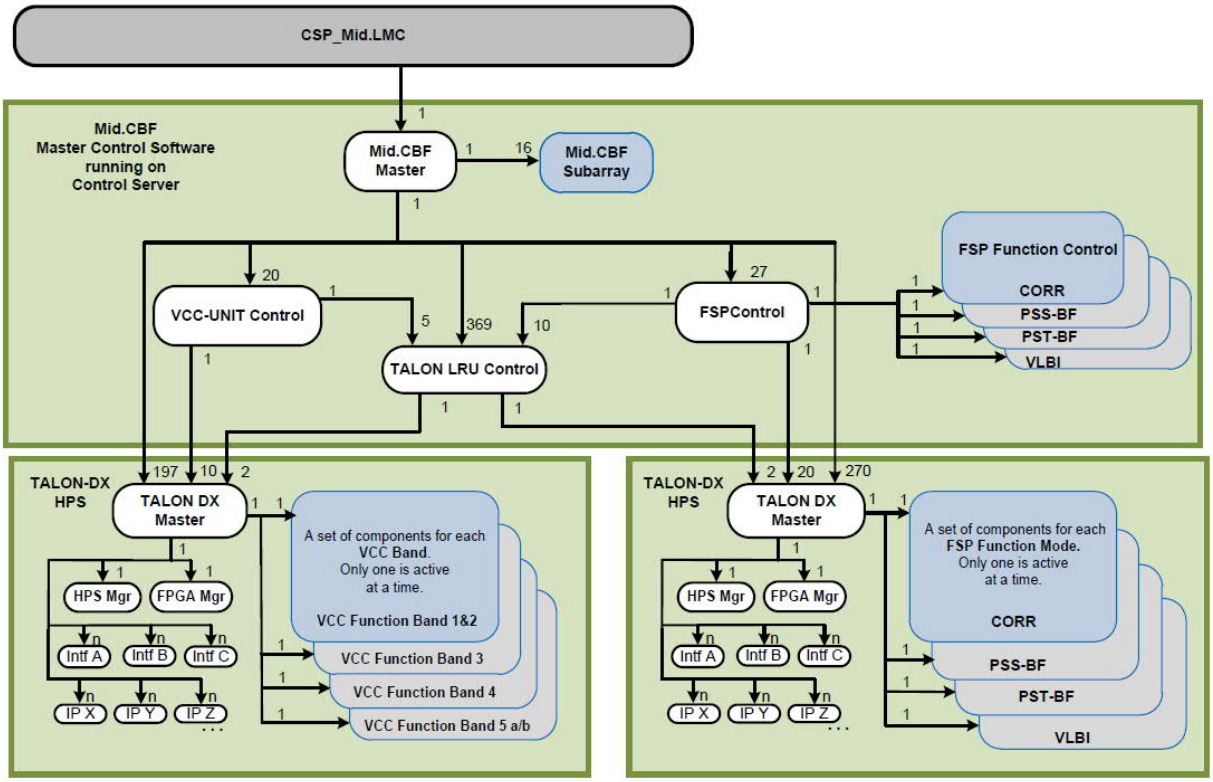

Figure 4-7 Command and Control Primary Presentation view of the SKA1 Mid.CBF M&C system; the AT.CBF view is similar, adapted appropriately.

The "CSP_Mid.LMC" block of Figure 4-7 for AT.CBF is equivalent to the existing or modified ALMA online executor/scheduler. It is provided JSON configuration/execution scripts, one script for each observation block, which it sends to AT.CBF for execution at the appropriate times. As is current ALMA practise[22], these scripts are built off-line and in advance by the previously-mentioned observer/observation preparation tool built for AT.CBF and containing configuration information needed by AT.CBF Master to configure all TALON-DX compute nodes.

The "TALON-DX HPS" (Hard Processor System) of Figure 4-7 is an embedded multi-core ARM processor residing in each TALON-DX FPGA and it is in these FPGAs—one on each TALON-DX circuit board and two such boards in each TALON LRU (see section 7.2)—that all VCC and AFSP signal processing occurs. These HPS compute nodes perform final mapping of configuration requests from AT.CBF Master to FPGA control register configurations, as well as performing real-time functions such as delay & phase tracking and some data product acquisition and timestamping.

In this manner it is believed the AT.CBF can be more or less seamlessly integrated into the existing ALMA online executor/scheduler infrastructure and use, to the greatest extent possible, most SKA1 Mid.CBF developments.

[22] At least as we understand ALMA's real-time operation from our investigation.

Other SKA1 Mid.CBF views and "Presentations", including monitoring and archiving, sub-array configuration and control, and an example AT.CBF configuration script are presented and discussed in further detail in section 8.

5 Key requirements

Up until now the processing capabilities of the TALON/FSA-based AT.CBF have been described as "capabilities" and somewhat loosely. In this section, we develop key requirements for AT.CBF, largely based on SKA1 Mid.CBF (Level-3) requirements, but augmented with requirements specific to ALMA and AT.CBF processing. Key requirements are those that are judged to be major design and cost drivers or science performance indicators and define the key capabilities of any system that meets them. Development of a full requirements set is beyond the scope of this report but will, of course, be needed in the engineering of an actual system.

In order to clearly specify requirements for a near-term AT.CBF that replaces the BLC at the existing bandwidth and an ALMA 2030 AT.CBF that processes at least 2X bandwidth, the following naming convention is used in the requirements below:

- "AT.CBF" – the requirement applies to both the replacement and ALMA 2030 correlator/ beamformer.
- "AT.CBF-2030" – the requirement applies only to the ALMA 2030 correlator/beamformer.
- "AT.CBF(only)" – the requirement applies only to the replacement correlator/beamformer.

In the following tables the "Req ID" is just a logical requirement identification number local to this document to facilitate referencing within this document (and by external documents if desired.)

5.1 Functional requirements

Table 5-1 AT.CBF functional requirements

Req ID	Requirement	Traceability	Compliance/Comments
General			
AT.CBF-0000	When commanded, AT.CBF(only) shall ingest and process at least 8 GHz/pol of double-sideband digitized data from each of up to 80 antennas.	[10] [11] AT.CBF design	Compliant.
AT.CBF-0001	When commanded, AT.CBF-2030 shall ingest and process at least 16 GHz/pol of double-sideband digitized data from each of up to 80 antennas.	[12] [10] [11]	Compliant. AT.CBF(only) can be seamlessly upgraded to AT.CBF-2030 bandwidths (TBC[23])
AT.CBF-0002	When commanded, AT.CBF shall configure its processing resources such that: • Data from each antenna digitizer is divided into multiple identical Frequency Slices whose collective contiguous	SKA1 Mid.CBF design [7]	Compliant.

[23] With input as to the selection of ALMA 2030 digitizer frequencies to be compatible with AT.CBF VCC processing.

	Processed Bandwidth covers the entire digitized bandwidth and, • The Processed Bandwidth of each Frequency Slice is 200 MHz +/-2 MHz.		
AT.CBF-0003	AT.CBF(only) shall contain at least 24 AFSPs, each AFSP processes any two select Frequency Slices and each AFSP is independently configurable under software control to any one of the following Function Modes: • Imaging Correlation or, • VLBI Beamforming.	AT.CBF design proposal derived from SKA1 Mid.CBF design [7] [3]	Compliant.
AT.CBF-0004	AT.CBF-2030 shall contain at least 48 AFSPs, each AFSP processes any two select Frequency Slices and each AFSP is independently configurable under software control to any single one of the following Function Modes: • Imaging Correlation or, • VLBI Beamforming.	AT.CBF design proposal derived from SKA1 Mid.CBF design [7] [11]	Compliant.
AT.CBF-0005	AT.CBF shall provide full processing capability with no performance degradation for a maximum ALMA array diameter of at least 500 km.	"100s of km stretch goal" [11]	Compliant.
AT.CBF-0006	The phase-center, for any AT.CBF sub-array, shall be within the smallest circle encompassing the sub-array.	SKA1 Mid.CBF req't [7]	Compliant.
AT.CBF-0007	AT.CBF shall provide sub-arraying capability, for up to 16 independent simultaneous sub-arrays in each AFSP, for its configured Function Mode.	6 minimum [11] SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-0008	When commanded, for all output correlation and beamforming data products, as appropriate, AT.CBF shall calculate and provide all internally-determined and calculated gain correction factors to be applied in post-processing.	(Brogan: ALMA can't do on-sky bandpass cal) [13] SKA1 Mid.CBF design [7]	Compliant.
AFSP Function Mode: Imaging Correlation			
AT.CBF-0100	When commanded, AT.CBF normal (non-zoom) Imaging Correlation AFSP Function Mode shall provide, for each	SKA1 Mid.CBF req't [7]	Compliant.

	Frequency Slice independently, for each of up to 16 sub-arrays independently: • 14,000 to 15,000 critically-sampled channels across the Frequency Slice Processed Bandwidth. • Post-correlation channel averaging factors of at least 2, 3, 4, 5, 6, and 10. • Linearly-spaced channels, with or without channel averaging, across the Processed Bandwidth of the Frequency Slice and any number of adjacent Frequency Slices sourcing from the same digitizer. • For each sub-array independently, selectable sideband suppression or sideband separation correlation. Note: when sideband separation, the total net correlated output bandwidth is 2X the Frequency Slice Processed bandwidth comprised of 2X the number of channels (i.e. 28,000 to 30,000.) • Cross-correlation visibility integration times, settable for each sub-array independently in integer multiples of 16 msec, up to 10 sec, synchronized to the 16 msec Walsh time epoch, and such that integration times across all AFSPs that are part of the same sub-array are synchronized in time. • Auto-correlation visibility integration times down to at least 1 msec. • Delay and phase tracking for a phase-reference position on the sky (a.k.a the boresight delay center), which is within	[11] [3]	

	the antenna primary beam HPBW and independent of any other Frequency Slice, and which may be different and variable by up to +/-10 nsec for each polarization.		
AT.CBF-0101	When commanded, AT.CBF Imaging Correlation AFSP Function Mode, when correlating Zoom Windows, shall provide for each Frequency Slice independently: • At least 1 tunable Zoom Window per antenna, with a tuning resolution of at least 10 kHz anywhere in the Frequency Slice Sampled Bandwidth. • Zoom Window sampled bandwidths of /2, /4, /8, /16, /32, or /64 of a Frequency Slice sampled bandwidth. • Sideband suppression only. • Auto and cross-correlation visibility integration times, settable for each sub-array independently in integer multiples of 16 msec, up to 10 sec and such that integration times across all AFSPs that are part of the same sub-array are synchronized in time. • Number of channels and channel averaging identical to non-zoom visibilities. • Linear channel spacing within each Zoom Window independently. • Delay and phase tracking for a phase-reference position on the sky (a.k.a the boresight delay center), which is within the antenna primary beam HPBW and independent of any other Frequency Slice, and which may be different and variable by up to +/-10 nsec for each polarization.	SKA1 Mid.CBF req't [7] min req'd spectral resolution: 1.17 kHz [11] Assumption: sideband suppression only sufficient	Partially compliant for integration time: The narrowest zoom channel width of ~211 Hz requires 24 x 16 msec = 384 msec to ensure that each integration is the same number of unique samples. For integration times less than this down to 16 msec, the number of unique samples per integration is not identical; this means that there is some "leakage" of a sample across integration boundaries resulting in some integration time smearing. See section 6.1.2. Sideband suppression is performed by the Frequency Slice phase rotator in the AFSP. See section 6.1.2.

AT.CBF-0102	When commanded, in AT.CBF Imaging Correlation AFSP Function Mode, each sub-array in any AFSP, and for each Frequency Slice independently, shall be independently configured to correlate zoom or non-zoom visibilities, but not both.	SKA1 Mid.CBF design [7] flexibility [11]	Compliant.
AT.CBF-0103	When commanded, in AT.CBF Imaging Correlation AFSP Function Mode, each zoom sub-array in any AFSP, and for each Frequency Slice independently, shall be configured for a Zoom Window bandwidth and tuning independently from any other sub-array's or Frequency Slice's configuration.	SKA1 Mid.CBF design [7] flexibility: spectral tuning independence and resolution req'd to achieve req'd spectral resolution [11]	Compliant.
AFSP Function Mode: VLBI Beamforming			
AT.CBF-0200	AT.CBF VLBI Beamforming AFSP Function Mode shall be capable of forming a total of at least 4 independent VLBI Beams per Frequency Slice, across all sub-arrays, where each independent Beam may be on a different delay center on the sky within the antenna HPBW, and independent of any other AFSP's Beam steering.	SKA1 Mid.CBF design [7] 1 minimum [11]	Compliant. This means that a total of 8 Beams can be formed in each AFSP, across all sub-arrays and Frequency Slices.
AT.CBF-0201	When commanded, the AT.CBF VLBI Beamforming AFSP, for each Frequency Slice independently, and for each sub-array independently, shall form at least 2 VLBI Beams per-sub-array and each Beam: • Has a contiguous, non-channelized, Processed Bandwidth of a Frequency Slice. • Can be formed from a select sideband. • Is independently steerable to a delay center on the sky anywhere within the HPBW of	SKA1 Mid.CBF design [7] AT.CBF design 1 minimum [11]	Compliant.

	the antenna primary beam, and which may be different and variable by up to +/-10 nsec for each polarization. • Can be formed from any select ALMA-B or ACA antennas up to all antennas.		
AT.CBF-0202	When commanded, in VLBI Beamforming Function Mode and simultaneous with beamforming in each VLBI sub-array, each AT.CBF AFSP shall: • Produce 900 to 1000 supporting visibility channels for a select sideband, for at least 1 Beam (i.e. delay center), across the Frequency Slice Processed Bandwidth. • Have an integration time in the range of 16 msec to 10 sec, synchronized in time within each sub-array across all AFSPs.	SKA1 Mid.CBF design [7] Assume sideband suppression correlation only.	Compliant. Sideband separation is possible if required: 224.0 MHz / 1024 channels = 218.750 kHz, having 3500 samples every 16 msec.
AT.CBF-0203	In AT.CBF VLBI Beamforming Function Mode, within each AFSP independently and for each Frequency Slice within it independently, at least 16+1 Beam-Channels shall be produced, distributed arbitrarily across sub-arrays with: • 16 Beam-Channels having at least 2 kHz tuning resolution anywhere within the Frequency Slice Sampled Bandwidth (of 224 MHz), with bandwidths of 1 MHz x 2^n (n=0, 1, ..., 7.) • 1 Beam-Channel fixed at the Frequency Slice sampled bandwidth of 224 MHz. • Real output. • Nyquist-sampled output sample rates. • Independently settable 2-bit, 4-bit, or 8-bit word size per Beam-Channel. • VDIF formatted output.	SKA1 Mid.CBF req't and design [7] AT.CBF design	Compliant.

5.2 Performance Requirements

Table 5-2 AT.CBF performance requirements

Req ID	Requirement	Traceability	Compliance/Comments
AT.CBF-0300	In AFSP Imaging Correlation Function Mode, AT.CBF normal and zoom visibilities shall: • Have a -3 dB +/-0.01 dB channel edge amplitude, • Be monotonically decreasing in any region above -60 dB from the channel edge to the next adjacent channel center frequency, • Have an amplitude of -80 dB or better thereafter (i.e. reject band), • Have a post-gain factor correction amplitude that varies at most by +/-0.01 dB across the processed bandwidth across all Frequency Slice of a digitized bandwidth and, • Provide at least 99% correlation efficiency when there is no more than 10% RFI power present in any particular channel.	SKA1 Mid.CBF req't [7]	Compliant as per the SKA1 Mid.CBF design, except with 6+6b samples correlated rather than 9+9b as the RFI environment for ALMA is less extreme.
AT.CBF-0301	Zoom Window visibilities produced by AT.CBF, when averaged to the same frequency channel resolution as non-zoom visibilities, and for spectrally flat signals with half-power bandwidths greater than 3 non-zoom visibility widths, shall agree with normal visibilities to within +/-0.01% in amplitude and +/-1e-4 radians in phase, for the same frequency range, integration time, and stationary input data.	SKA1 Mid.CBF req't [7]	Compliant.
AT.CBF-0302	When commanded, AT.CBF shall provide digital bandpass correction factors, per-antenna and per-spectral channel that, once applied and for spectrally-flat signals with half-power	Brogan: "ALMA can't do on-sky bandpass cal [11]	Compliant.

	bandwidths greater than 3 channel widths, correct any digital spectral gain variations introduced by AT.CBF to within 0.01% in amplitude and 0.001 radians of phase.	SKA1 Mid.CBF design [7]	
AT.CBF-0303	Unless commanded to do so, AT.CBF shall maintain the complex response of all visibility and beamforming data products at a level within 0.01% in amplitude and within 1e-4 radians of phase, through any AT.CBF delay center on the sky changes, resets, or power cycles.	SKA1 Mid.CBF req't [7]	Compliant.
AT.CBF-0304	Imaging visibilities produced by AT.CBF shall have an amplitude response, after application of AT.CBF per-channel gain factors, which varies by at most +/-0.01 dB across the Processed Bandwidth. Applies to both zoom and normal visibilities.	SKA1 Mid.CBF req't [7]	Compliant. This is a swept-tone response with allowed variation due to uncorrectable effects of imaging channel ripple and coarse-channel-ripple gain slope within an imaging channel.
AT.CBF-0305	In AFSP VLBI Beamforming Function Mode, AT.CBF visibilities produced in support of VLBI simultaneously in the same AFSP shall: • Have visibility channel response: maximum +/-0.1 dB amplitude and +/-0.01 radian phase passband (channel edge-to-edge) ripple; -3 dB +/-0.2 dB channel edge amplitude; monotonically decreasing amplitude from the channel edge to the adjacent channel far edge; at least -60 dB reject-band amplitude anywhere greater than the 1 channel width away from the channel edge and, • Provide at least 99% correlation efficiency when there is no more than 10% RFI power present in any particular channel.	SKA1 Mid.CBF req't [7] Efficiency [11] Assumption not to use imaging channels for VLBI tied-array solutions.	Compliant.
AT.CBF-0306	When commanded, AT.CBF shall apply wavefront delay model corrections such that the coherence loss (visibilities and	SKA1 Mid.CBF req't [7]	Compliant.

	beams) resulting from such corrections, not including errors in the provided delay model, is <0.1%.	Efficiency [11]	
AT.CBF-0307	When commanded, AT.CBF shall apply delay and phase model corrections such that there is no discernable correlated phase or amplitude closure anomalies, on any integration time scale, above the expected noise.	Simplified derivation from SKA1 Mid.CBF req'ts [7]	Compliant.
AT.CBF-0308	When commanded, AT.CBF shall apply delay and phase model corrections when forming VLBI Beams such that there is no discernible phase or amplitude variation due to such application above the expected noise.	Simplified derivation from SKA1 Mid.CBF req'ts [7]	Compliant.
AT.CBF-0309	When commanded, AT.CBF shall apply phase rotation (frequency shift) corrections on Frequency Slices up to at least +/-10 MHz (TBC), with no discernible impact on output data quality compared to no shift, over the expected noise and bandpass characteristics.	SKA1 Mid.CBF design [7] Frequency offset removal [3]	Compliant.
AT.CBF-0310	When commanded, AT.CBF shall apply Walsh +/-90 and/or +/-180 degree phase switching for sideband suppression or separation in-sync with the reference 48 msec with a minimum period of 16 msec with maximum time skew of +/-1 sample of a channel stream in any integration (TBC.)	[3] Assume that some time skew is allowed	Compliant

5.3 Interface Requirements

Table 5-3 AT.CBF interface requirements

Req ID	Requirement	Traceability	Compliance/Comments
Interface to ALMA-B and ACA antenna digitized sampled data streams			
AT.CBF-0400	AT.CBF(only) shall be compliant with the existing ALMA-B and ACA antennas' digitized sequences, with format, optical characteristics, and number of fibers per antenna as defined in [5].	A necessary capability of a replacement correlator/ beamformer	Compliant.

AT.CBF-0401	AT.CBF(only) shall ingest digitized data from existing ALMA-B and ACA antennas' digitized sequences as: • 4 x 2 GHz/polarization Digitized Bandwidth, real, • The center 90% (TBC) of the Digitized Bandwidth is the Processed Bandwidth (for science), • Sample rate of 4.0 Gs/s for each of the 8, 2 GHz Digitized Bandwidth signals and, • 3 bits per real sample.	[5][4]	Compliant. ACA antenna digitized samples streams appear, from available documentation, to be identical to ALMA-B antennas.
AT.CBF-0402	AT.CBF shall automatically recover and require no on-sky calibration in the event of a temporary loss of link on any or all antenna data ingest pipelines (fibers.)	Assume this is a valuable capability to help maximize ALMA observing time.	Compliant. From [5] the 48 msec TE pulse, embedded with the data, comes from each antenna to the AT.CBF. AT.CBF uses the 48 msec reference, and the embedded antenna 48 msec, to re-establish timing after a link loss, of whatever duration similar to SKA1 Mid.CBF's use of a 1PPS ([7] section 5.2.6.) Assume ALMA-2030 antennas will have a similar embedded time tick.
AT.CBF-0403	AT.CBF-2030 shall be compliant with ALMA 2030 antennas' (ALMA-2030-B and ACA-2030) digitized sequences, with format and optical characteristics TBD.	Placeholder for 2030 interface	Compliant, subject to input on choice of digitizer frequencies.
Interface to ALMA reference clock and timing			
AT.CBF-0500	AT.CBF(only) shall accept a 0 dBm +/-6 dBm, single-ended, 125 MHz reference clock, frequency-locked to the digitized data streams from all ALMA antennas including ALMA-B and ACA. This clock: • May be square-wave or continuous sinusoidal wave, • Has pk-pk cycle-to-cycle jitter not exceeding 200 psec (TBC), • Is present on an N-type female/jack coaxial connector	Discern from [4]	Compliant. Max phase wander spec is required to size internal AT.CBF buffers.

	at the AT.CBF interface boundary, • Has no phase wander on any timescale compared with digitized data samples exceeding 50 nsec (TBC.)		
AT.CBF-0501	AT.CBF(only) shall accept an LVDS 48 msec period square-wave clock as its timing epoch. This clock: • Is phase-stable with the 125 MHz reference with a minimum 1 nsec set up and 1 nsec hold time (TBC), • Is AC-coupled with a differential pk-pk voltage swing in the range of 200 mV to 1.5 V (TBC), • Is present on a Twin-ax coaxial connector (TBD) at the AT.CBF interface boundary, • Is coincident with the reference UTC 1-second epoch every 6 seconds, • Has the same timing epoch as the 48 msec TE pulse in the digitized data stream flowing from ALMA-B and ACA antennas, with uncertainty due to the antenna-to-AT.CBF delay.	Discern from [4]	Compliant. If the phase wander of the 48 msec is such that it can't be reliably captured consistently on a 125 MHz clock edge then single-shot capture (on command) and internal flywheel can be used instead.
AT.CBF-0502	When commanded, AT.CBF shall obtain its absolute UTC time from a Network Time Protocol (NTP) server via the AT.CBF-to-ALMA Ethernet network connection.	SKA1 Mid.CBF design [7]	Compliant. Fundamentally AT.CBF doesn't know the time (e.g. it could know the time from packets from antennas, but not with the existing protocol) so must get it from such a server.
AT.CBF-0503	The latency of NTP UTC time messages to AT.CBF shall be less than ~10 msec (TBC) from the UTC epoch.	Require there is no ambiguity in tagging a 48 msec epoch with UTC	Compliance TBD.
AT.CBF-0504	AT.CBF-2030 reference clock and epoch shall have similar functionality as the existing ALMA clock and timing, but possibly with different values TBD.	AT.CBF design	Compliant. AT.CBF clock and timing ingest can build/create compatible

			internal clock and timing if needed.
Interface to ALMA online controller/executor or other ALMA computers			
AT.CBF-0600	When commanded, AT.CBF shall accept a JSON script file for its configuration for a sub-array and Observation Time Block (OTB) (defined here as a contiguous period of time where the sub-array configuration does not change, although source pointing, i.e. delay and phase models, may), and be producing valid output science data starting at the stated execution epoch.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-0601	When commanded, the ALMA online controller/executor shall provide AT.CBF with an OTB JSON script file at least 10 seconds (TBC) in advance of the time epoch of when it is to take effect, wherein AT.CBF is producing valid science output data.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-0602	When commanded, AT.CBF shall make a new JSON file take effect such that a maximum of 10 seconds (TBC) of dead time (i.e. where no or flagged science data is produced) occurs before the OTB execution epoch.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-0603	AT.CBF shall perform internal consistency/resource checking to ensure that a JSON configuration file, if executed, does not over-write an existing configuration that has not completed execution.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-0604	The minimum period of new JSON OTB configuration file application requests to AT.CBF, for a particular sub-array and without requiring AFSP Function Mode changes, shall be 30 seconds (TBC.)	SKA1 Mid.CBF design [7] Assume fast switching required	Compliant.
AT.CBF-0605	Each AT.CBF sub-array's configuration, including start and stop times, shall be independent of any other sub-array, except as imposed by AFSP Function Mode configuration restrictions.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-0606	When commanded, AT.CBF shall provide the ALMA online	SKA1 Mid.CBF design [7]	Compliant.

	controller/executor with monitor data for any time period up to 7 days (TBC) previous to the current time.	Assumption	
AT.CBF-0607	AT.CBF shall maintain monitor data in its internal data base for a period of at least 7 days (TBC) previous to the current time.	SKA1 Mid.CBF design [7] Assumption	Compliant.
AT.CBF-0608	AT.CBF shall make its internal monitor data base available to external ALMA networked computers via its Ethernet network connection using an appropriate industry-standard protocol such as NFS.	Assumption	Compliant.
AT.CBF-0609	When commanded, AT.CBF shall provide network access to its internal servers and databases without authentication.	SKA1 Mid.CBF design [7]	Compliant. Rely on ALMA networking/firewalls to provide authentication.
Delay models			
AT.CBF-0700	When commanded, AT.CBF shall accept streaming delay models, one (set) for each antenna, from an ALMA network server in a publish-subscribe fashion with protocol TBD.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-0701	One or more ALMA network servers shall supply AT.CBF with delay models, each of which is a polynomial of order TBD valid from a defined start epoch, for at least 10 seconds.	SKA1 Mid.CBF design [7]	Compliant. Polys for ~10 sec each is preferred. Faster cadence and lower order models could be handled if absolutely necessary.
AT.CBF-0702	Any VLBI tied-array delay/phase closure solutions provided to AT.CBF shall be incorporated with streaming delay models, except that phase corrections that are to be applied independently of delay may be a different stream.	SKA1 Mid.CBF design [7]	Compliant. If needed, the tied-array (residual) delay models can be separate from geometric delay models and AT.CBF can merge them.
Visibility outputs to the ALMA Archive			
AT.CBF-0800	When commanded, AT.CBF shall write ALMA/CASA-format imaging visibility data sets to one or more ALMA Archive servers. Note: AT.CBF (internally AT.CDP) needs to be provided (mechanism TBD) with required meta-data to form complete data sets ready for CASA ingest.	[3]	Compliant.

AT.CBF-0801	When commanded, AT.CBF shall send or write TBD-format visibility data sets in support of VLBI to one or more ALMA servers that calculate tied-array solutions. Note: AT.CBF (internally AT.CDP) needs to be provided (mechanism TBD) with required meta-data to form complete data sets ready for the ALMA online tied-array solutions calculator.	Assumption	Compliant. AT.CBF does not calculate tied-array solutions.
AT.CBF-0802	When commanded, AT.CBF shall sustain a continuous total visibility output data rate of at least 280 MB/sec, spread across TBD 100 Gbit Ethernet links, each with 10 km, 1500 nm, single-mode fiber optics (TBC.)	[11]	Compliant.
VLBI Beam (Beam-Channel) outputs			
AT.CBF-0900	VLBI Beam-Channel streaming outputs shall be Ethernet UDP/IP packet format, with a VDIF (VLBI Data Interface Format) user data payload.	SKA1 Mid.CBF design [7] Assumption	Compliant.
AT.CBF-0901	When commanded, Each VLBI Beam-Channel streaming output, constituting a dual-polarization sampled stream, shall be independently configurable for 2-bits, 4-bits, or 8-bits per sample.	SKA1 Mid.CBF design [7] (except 16 bits not expected to be useful for ALMA)	Compliant.
AT.CBF-0902	When commanded, for each VLBI Beam-Channel streaming output and polarization independently, AT.CBF shall determine appropriate weights such that quantization efficiency within at least 10% of the optimal is obtained, and thereafter maintain that weighting until next commanded to change.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-0903	VLBI Beam-Channel streaming outputs shall be real sampled data, with the same frequency sense as the RF signal from whence it came.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-0904	AT.CBF Beam-Channel output data rate capacity shall be such that the full ALMA bandwidth, for one beam, can be output at 2 bits per sample.	Assumption	Compliant.

AT.CBF-0905	AT.CBF Beam-Channel outputs shall be delay and phase-corrected to the ALMA (sub-) array phase center, a.k.a. array "topo-center".	Believed to be standard VLBI tied-array practise	Compliant.
Mains power			
AT.CBF-1000	The mains power supply to AT.CBF shall be 3-phase 230VAC (Wye.)	SKA1 Mid.CBF design [7]	Compliant. Alternatively, 48VDC mains is possible.
AT.CBF-1001	AT.CBF shall automatically balance its 3-phase loading to be within 5% of each other.	SKA1 Mid.CBF req't [7]	Compliant.
AT.CBF-1002	The total steady-state operational power requirement of AT.CBF(only) shall be less than 100 kW (TBC.)	SKA1 Mid.CBF design [7] translated to AT.CBF	Compliant. Calculated for 24 AFSPs.
AT.CBF-1003	The total steady-state operational power requirement of AT.CBF-2030 shall be less than 150 kW (TBC.)	Assume TALON technology refresh to keep within BLC power limit	Compliant. Calculated for 48 AFSPs.
AT.CBF-1004	The steady-state operational power requirement of each AT.CBF Signal Processing Rack shall be less than 12 kW.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-1005	For 1+1 fault-tolerant redundancy, AT.CBF shall be equipped to accept, and if ALMA infrastructure is so enabled accept, dual redundant mains AC power such that AT.CBF remains fully operational (at its current operational state) if either source blacks out for any period of time.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-1006	AT.CBF power draw delta shall be less than 20% of the maximum steady-state power draw, averaged over a one second interval, at all times.	SKA1 Mid.CBF req't [7]	Compliant.
AT.CBF-1007	AT.CBF shall, at all times, ensure that its instantaneous peak power load is within 125% of its maximum steady-state load.	Assumption	Compliant.
AT.CBF-1008	The power quality of mains AC power provided to AT.CBF shall meet or exceed TBD specifications.	SKA1 Mid.CBF req't [7] (needed to determine internal	Compliant. Costing in this report assumes that AT.CBF is supplied "office quality" mains AC power.

		AT.CBF mains power conditioning requirements, if any)	
AT.CBF-1009	When commanded, AT.CBF shall automatically power-up and come to an operationally-ready state within 5 minutes (TBC.)	SKA1 Mid.CBF design [7] Assumption	Compliant.
AT.CBF-1010	When commanded, AT.CBF shall automatically and safely power down to a power-off state within 1 minute (TBC.)	SKA1 Mid.CBF design [7] Assumption	Compliant.
AT.CBF-1011	AT.CBF equipment shall have dead-man thermal overload protection that independently detects and powers-down affected equipment when the equipment's safe operating temperature range is exceeded.	SKA1 Mid.CBF req't [7]	Compliant.
Cooling & environment (air cooling; DCLC not included in this report)			
AT.CBF-1100	AT.CBF shall operate in a "cold aisle/hot aisle" air-cooling environment where the cold aisle is provided at the front of each AT.CBF rack and the hot aisle is at the back.	SKA1 Mid.CBF design/req't [7]	Compliant.
AT.CBF-1101	AT.CBF shall maintain its fully-operational steady-state condition: • For ambient temperature, available at rack front (cold-aisle), between 18 C and 27 C, • With maximum cold-aisle ambient temperature slew rate, at any time, of 5 C/hour and, • At an equivalent air-density altitude not exceeding 2900 m (9900 ft.)	SKA1 Mid.CBF design/req't [7]	Compliance assumes the AT.CBF is located at the OSF. Location of it at the high-site would require further cooling study and design beyond the scope of this report.
AT.CBF-1102	The air environment particulate contamination within which AT.CBF operates shall meet or exceed ISO Class 14644-1 class 8, with additional MERV 13 filtering (TBC: contamination of MTP fiber-optic connections is the main concern here and the correct standard needs to be chosen.)	EVLA correlator spec	Compliant. The air quality requirement is driven by fiber-optic connections.

AT.CBF-1103	The AT.CBF shall operate in a benign office environment with no imposed continuous vibration and/or shaking present (TBD: exact industry-standard specification of "benign office environment" required here.)	SKA1 Mid.CBF design/req't [7] Assumption	Compliant.
AT.CBF-1104	The AT.CBF shall survive an earthquake of magnitude X for a period of Y seconds. (Exact definition of X, Y, and "survive" is TBD.)	Assumption: ALMA is in a severe earthquake zone	Compliant. Further requirement refinement to an industry-standard applicable to the ALMA OSF is required.
AT.CBF-1105	The radiated EMI emissions of each AT.CBF equipment unit or LRU shall meet or exceed FCC Part 15, Subpart J, Class-A (TBC)	SKA1 Mid.CBF design/req't [7] FCC equivalent; a reasonable spec to meet to ensure EMC.	Compliant.
AT.CBF-1106	AT.CBF conducted EMI emissions onto ALMA AC mains power of each AT.CBF equipment unit or LRU shall meet or exceed FCC Part 15, Subpart J, Class A (TBC.)	SKA1 Mid.CBF design/req't [7] FCC equivalent; a reasonable spec to meet to ensure EMC.	Compliant.
AT.CBF-1107	AT.CBF shall operate without fault (caused by external EMI) at radiated and conducted emissions levels from its own or other equipment units or LRUs not exceeding FCC Part 15, Subpart J, Class A.	Assumption	Compliant.
AT.CBF-1108	AT.CBF equipment units or LRUs, during operation and handling shall meet at least ESD 15 kV tolerance (TBC, TBD.)	SKA1 Mid.CBF design [7] Assumption	Compliant. This means that AT.CBF can be located in an office environment, and AT.CBF LRUs can be handled with no purposeful ESD human handling measures in place.
AT.CBF-1109	The AT.CBF operating environment shall have a humidity maintained between 20% and 40% RH (TBC).	Assumption	Puts requirements on the room design, important for cooling and controlling ESD.

AT.CBF physical infrastructure			
AT.CBF-1200	The total number of AT.CBF(only) racks shall be maximum 12 (TBC.)	AT.CBF(only) design	Compliant for the 24 AFSPs. Assume max 2 AT.CDP racks.
AT.CBF-1201	The total number of AT.CBF-2030 racks shall be maximum 20 (TBC.)	AT.CBF(only) design	Compliant for 48 AFSPs. Assume max 3 AT.CDP racks.
AT.CBF-1202	Each AT.CBF physical rack shall: • Have maximum outside dimensions within a 600 mm (W) x 1070 mm (D) x 2000 mm (H) and, • Have a mass less than 600 kg.	SKA1 Mid.CBF req't [7]	Compliant.
AT.CBF-1203	ALMA infrastructure shall provide mains AC power for each AT.CBF rack via 1 (or 2, if redundant supplies) appropriate (TBD) power connector(s), located within 2 m (TBC) of under the floor.	SKA1 Mid.CBF design [7]	Compliant.
AT.CBF-1204	AT.CBF signal interconnect cabling, including intra-fiber cabling and fiber cabling from ALMA-B and ACA antennas shall be delivered to each rack via rack-overhead cable trays, provided by ALMA infrastructure.	SKA1 Mid.CBF design [7]	Compliant.
Reliability, availability, and maintainability			
AT.CBF-1300	AT.CBF shall be available at least 96% (TBC) of the time, assuming an MTTR of a TALON LRU of less than 24 hrs (TBC.)		Compliance TBC. Allows for an average of ~1 day per month of downtime for repair/maintenance.
AT.CBF-1301	AT.CBF shall be considered available if there is any failure of a single TALON-LRU in either the VCC-Part, AFSP-Part, or both simultaneously.		Compliant. Not well stated but this ensures that no explicit hardware redundancy or dynamic fail-over switching needs to be built into AT.CBF, something that can be very costly.
AT.CBF-1302	It shall be possible to hot-swap replace any TALON LRU in AT.CBF, affecting only the power of the affected unit.		Compliant.
AT.CBF-1303	TALON LRUs shall have hot-swap replaceable mains power supplies and fans.		Compliant.

			These are the 2 most likely to fail items.
AT.CBF-1304	TALON LRUs shall continue to operate if either or both of an LRU's mains power supply or fan fails.		Compliant.
AT.CBF-1305	All AT.CBF equipment, with the exception of TALON LRUs, shall be 1+1 redundant.		Compliant. Needed because such a failure of other equipment than TALONs requires rack power down.

6 Signal Processing Chain

This section presents and discusses, in considerable detail, the proposed signal processing chain which is closely aligned with the SKA1 Mid.CBF signal processing chain and for which costing in this report is developed.

It also briefly discusses and contrasts an alternative somewhat "standard" approach signal processing chain that could be implemented but that has some clear disadvantages and complications.

6.1 Proposed signal processing chain

6.1.1 Overview

As mentioned, the proposed AT.CBF signal processing design is derived from, and closely aligned to, the SKA1 Mid.CBF TALON Frequency Slice Architecture (FSA) [7]; doing so allows for considerable cost sharing with SKA1 Mid.CBF construction design and hardware procurement[24].

For imaging correlation, AT.CBF is fundamentally an "FFX" design, with the first "F" being an oversampling poly-phase coarse filterbank, the second "F" a critically-sampled fine 16k channel filterbank, and the "X" being the complex-conjugate multiply-accumulate correlation function of fine channels only within the center ~200 MHz of the Frequency Slice that contain no aliasing because of oversampling in the first "F". Coarse channels from the first "F" filterbank are referred to as "Frequency Slices" distributed to, and processed by, ALMA Frequency Slice Processors (AFSPs.)

For VLBI beamforming, the first "F" stage is the same as for correlation, with beamforming occurring on oversampled Frequency Slices in AFSPs, followed by optional tunable DDC (Direct Digital down Conversion) Beam-Channel filters to target spectral regions of interest within the Frequency Slice, before re-quantization and VDIF formatting for streaming output to VLBI recorder(s). Also, concurrently in the VLBI Beamforming AFSP, a second "F" critically-sampled medium-fine 1k channel filterbank, followed by the "X" complex correlation operation occurs. Calculating visibilities here allows for calculation of tied-array phase-closure solutions on the same delay-center as one of the two independently steerable VLBI beams, without compromising concurrent imaging correlation needs.

A simplified signal processing chain diagram from streaming input data from antennas to output data products for both Imaging Correlation and VLBI Beamforming is shown in Figure 6-1 below. The boxes highlighted in bold red are blocks that must be designed (or modified from Mid.CBF designs) and tested specifically for AT.CBF due to N=80 antennas (instead of SKA1 Mid's nearly 200), sideband separating correlation, and conversion of the (existing) ALMA 4.0 Gs/s sample rate to SKA1 Mid 3.96 Gs/s + kΔf s/s sample rates to allow use of as many downstream SKA1 Mid.CBF signal processing blocks as possible to realize AT.CBF implementation cost savings.

[24] Hardware procurement savings are contingent on alignment of SKA1 Mid.CBF and AT.CBF TALON LRU production timelines.

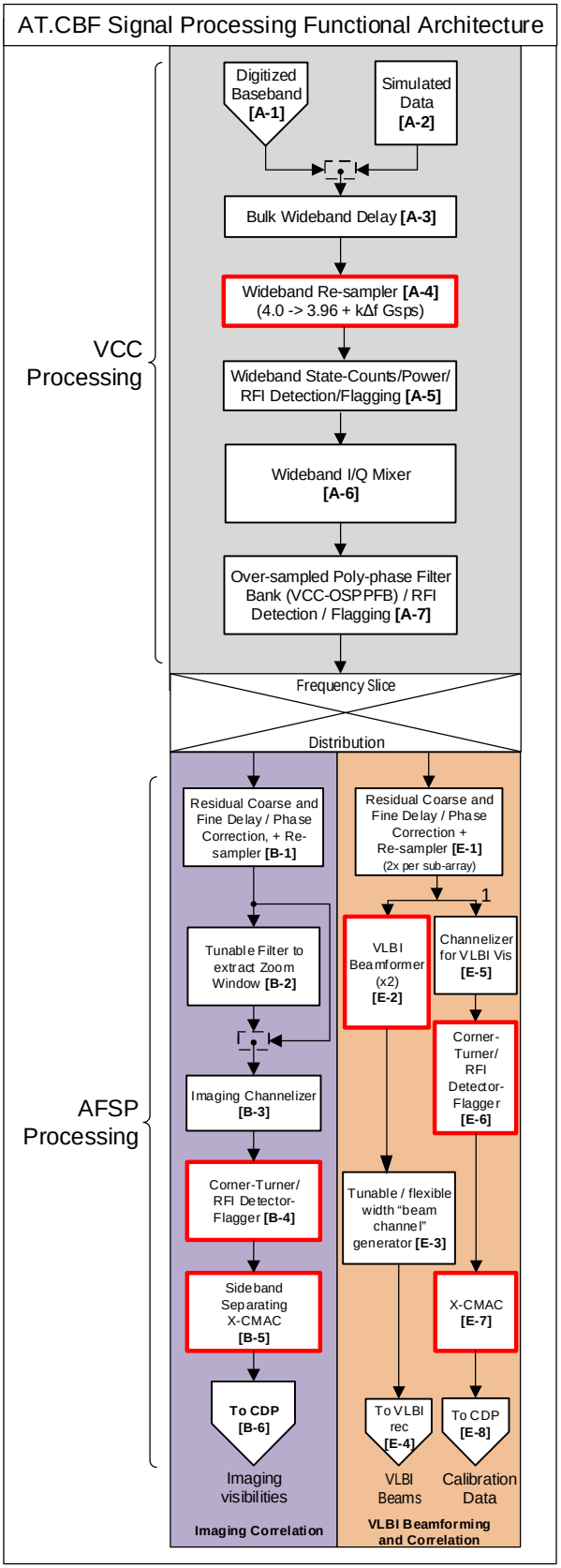

Figure 6-1 Simplified AT.CBF signal processing chain.

All signal processing occurs in (TALON LRU) Intel Stratix-10 FPGAs, with all VCC-to-AFSP Frequency Slice signal transport and distribution via passive optical fiber cross-connects operating at 25 Gbps per fiber (see section 7.1.)

6.1.2 Imaging Correlation signal chain

A more detailed signal chain diagram for Imaging Correlation is shown in Figure 6-2. This diagram indicates (without regard for how many antennas are being processed, data formats/data management, or how signals paths are implemented or cross-connected) each processing step, sample rate, number of bits per sample for each step, and amplitude and frequency responses extracted from [8] to illustrate what is happening to the signal at each step. Boxes and annotations in bold red are those that are designed specifically for (or are modified Mid.CBF blocks specifically for) AT.CBF (i.e. design deltas over SKA1 Mid.CBF.)

A brief description of each signal processing step in Figure 6-2 is as follows:

- Streaming digitized data, after frame decoding etc., is fed through a Bulk wideband delay [A-3]. This is updated every 10s to 100s of seconds[25] to compensate for most of the delay the signal must undergo and is the same for all streams. Once this delay is set, the residual (coarse and fine) delay is removed in the ReSampler in the AFSP. Thus, each Frequency Slice in each AFSP can have a different delay center on the sky, but not too different (i.e. within the antenna HPBW) since they all share this bulk delay component.

- Next, the streams are converted to SKA1-Mid standard sample rates in the [A-4] Wideband ReSampler block. There, each 4.0 Gs/s digitized stream is re-sampled down to 3.96 Gs/s + kΔf s/s, where k is a select integer, different for each antenna between 1 and 2222, and Δf=1800 Hz. This re-sampler, for select values of k, is an exact, rather than approximate, operation, i.e. the re-sampled interpolation points (in delay) are precisely determined. It is an 80-tap filter and, because data is only 3 bits wide, the data x tap coefficient multiply is performed using memory LUTs (lookup tables.)

  It is possible that this step could be eliminated and the 4.0 Gs/s stream be processed directly. In this case, the 10/9 VCC-OSPPFB output is 222.222⋯ MHz, which has an integer number of samples (i.e. repeat interval) every 18.0 sec. Re-sampling to f_c=221.1840 Ms/s still occurs and there are no baseline delay-rate dependent gain or phase artefacts in the correlator output (see below.) Further investigation is required to see if there is a design impact/delta on the downstream IP blocks compared to SKA1 Mid.CBF.

- Block [A-5] calculates reduced-sensitivity auto-correlations, cross-polarization correlations, and state counts to provide wideband signal diagnostic capability, with results periodically captured and saved to the monitor data base.

- Then, block [A-6]—a wideband I/Q mixer—allows the entire wideband signal (each of 8 streams independently) to be shifted around by at least +/-50 MHz with at least 10 kHz tuning resolution so that following Zoom Windows, selected from within Frequency Slices can be optimally placed on spectral regions of interest. Zoom windows and fine channelization in adjacent Frequency

[25] Depending on whether sidereal or X-times faster than sidereal delay tracking occurs.

Slices can be set such that contiguous linear channels across Frequency Slice boundaries are obtained, but this mixer allows for flexibility and optimization in the placement of Zoom Windows.

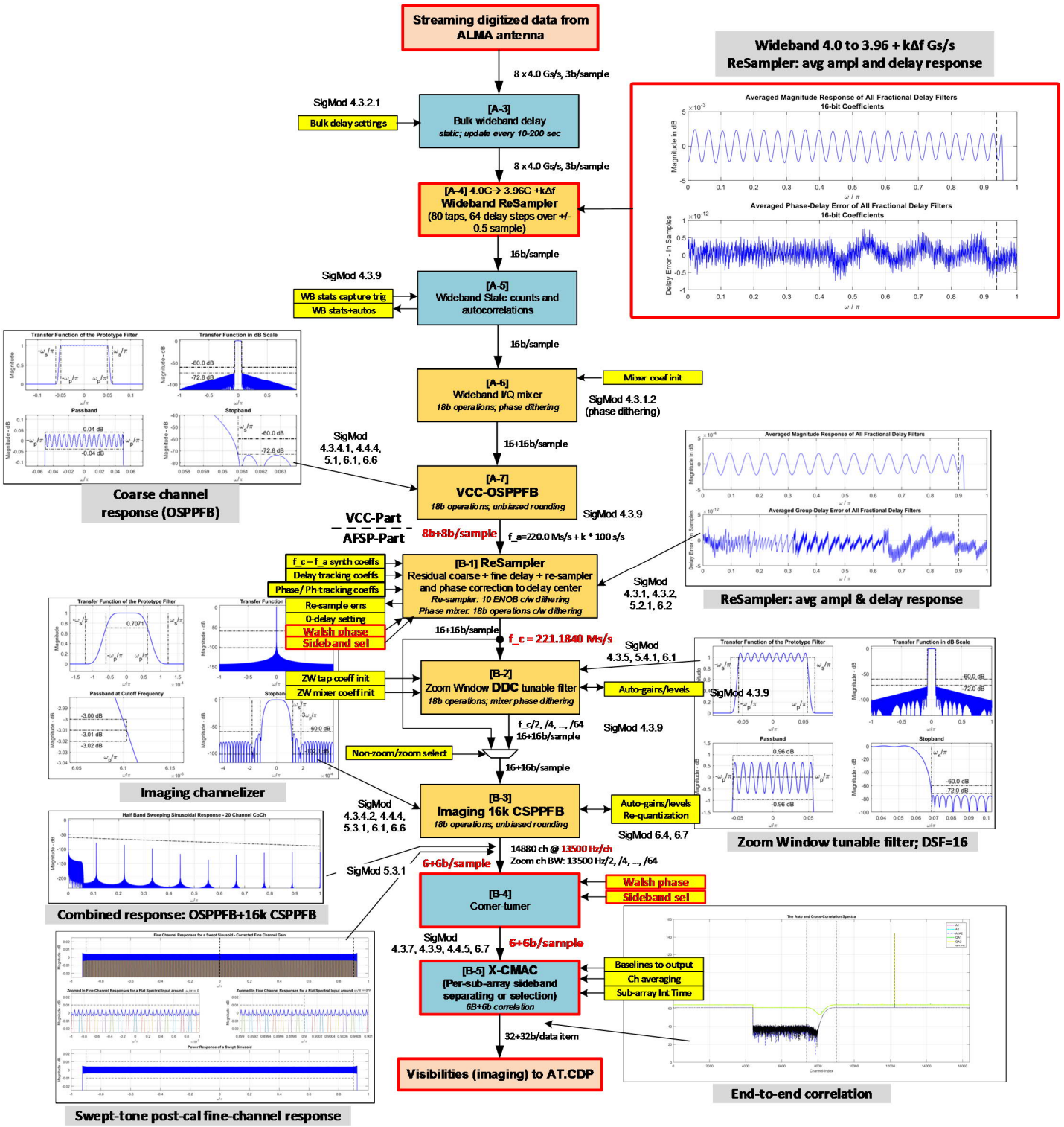

Figure 6-2 AT.CBF Imaging Correlation end-to-end signal chain diagram.

- Next, in block [A-7] (VCC-OSPPFB), the wideband signals are coarsely channelized with a 10/9 Over-Sampling Poly-Phase FilterBank. Each output coarse channel (i.e. Frequency Slice) is complex, at a complex oversampled sample rate (and bandwidth) of 220.0 Ms/s + k * 100.0 s/s, a rate that is nicely matched to FPGA direct processing. This last point is important since it means there is no corner-turner required before going to the next stage (something this is exceedingly complicated since the next stage is a poly-phase filterbank.) Frequency Slices out of block [A-7] are then routed to select 25G fiber output ports (2 Frequency Slices per fiber) at a quantization of 8+8b, via an internal FPGA circuit switch (not shown.) Each fiber operates at less than full capacity of ~14 Gbps (i.e. 220 Ms/s x 16b x 2 pol x 2 FS.)
- Next, in the AFSP, is the Frequency Slice ReSampler, block [B-1]. This block performs the following processing:
    - Coarse (residual from bulk) delay at the f_a=220.0 Ms/s + k * 100.0 s/s sample rate using an on-FPGA memory buffer.
    - Re-sampling to f_c=221.1840 Ms/s (a common sample rate) and fine (fractional) delay at the same time. Re-sampling is an interpolation operation and fractional delay is just a slowly changing offset to this interpolation. The fractional delay is 1024 steps between 0 and 1 samples, calculated at f_a.

      Re-sampling (provided the difference between the input sample rate and the re-sampled rate is sufficiently large) involves rapidly sweeping through all 1024 interpolation coefficients at a different rate for each antenna. This ensures that there are no baseline fractional-delay-dependent amplitude or phase anomalies on the output (i.e. the average amplitude and delay response of all 1024 tap coefficients is obtained as the annotation in Figure 6-2 shows[26]), and this means there are no delay rate-dependent anomalies or signatures in visibility and beam outputs.
    - Complex phase rotation including: earth-rotation fringe phase correction, frequency offset removal, shifting the Frequency Slice for fine channel alignment across adjacent Frequency Slices (see Figure 6-3), and Walsh sideband (suppression) selection via 90/180 phase switching if not doing sideband separation in the correlator.

  Since each ReSampler in each AFSP for each Frequency Slice is independent (including a separate one for each polarization), each one can implement a different delay & phase correction, hence each one is able to correct for a different delay center on the sky. Also in this ReSampler and in the phase rotator, the LSBit is scrambled to wipe out spectral spurs that are produced by saw-tooth fractional delay error and phase error functions [8] [1].

  The ReSampler also allows re-sampling to a common frequency, specifically chosen (see discussion below) to have features that allow synchronization to the 16 msec Walsh cycle, the correlator integration cycle, post-correlation channel averaging, linearly-spaced channels across Frequency Slices, and periodic re-synchronizing to a known epoch (48 msec.) The ReSampler de-

[26] Noting that the magnitude full-scale is 0.001 dB and the group delay full scale is 1e-11 samples.

couples sample rates chosen in the final "FX" from the original digitizer sample frequency, a feature with significant utility.

- Next, the signal undergoes selectable Zoom Window selection with a Direct Digital Conversion (DDC) filter [B-2] and decimation, followed by a 16k Critically Sampled Poly-Phase FilterBank (CSPPFB) [B-3]. Oversampling is not needed here because fine channels do not undergo further spectral decomposition before correlation. After the CSPPFB, data is re-quantized to 6+6b for efficiency of correlator implementation, allowed since the ALMA RFI environment is relatively benign.

- Finally, corner-turning [B-4] and complex correlation [B-5], sized for 80 antennas, with selectable sideband selection or separation occurs. The corner-turner arranges columns of samples out of the 16k CSPPFB into rows of samples, each being a burst of time-contiguous samples for each channel, an essential data arrangement for any practical channel-based (FX) correlator implementation. Visibilities, in native SKA1 Mid.CBF format, are transmitted to the AT.CDP for further long-term integration, channel averaging, and formatting for output to the ALMA Archive.

ReSampler output frequency and Walsh switching discussion

The primary additional design-driving feature of the AT.CBF compared to SKA1 Mid.CBF is the need for de-Walshing for selectable sideband suppression or separation, on a 16 msec cadence and synchronized with the reference 48 msec epochs. To accomplish this, of course, for normal-resolution (~14 kHz) imaging channels, a sideband separating correlator is required and in order to ensure precise separation, the number of samples per 16 msec period must be an integer.

The ReSampler [B-1] block in the AFSP easily facilitates this by allowing for precise digital re-sampling of the input Frequency Slice at complex sample frequency f_a=220.0 Ms/s + k * 100 s/s (out of the VCC-OSPPFB) to any arbitrary sample frequency. The "k * 100 s/s" is the frequency offset of the Frequency Slice, k (in the range 1…2222) chosen differently for each antenna, part of the SKA1 Mid telescope design of "frequency offset sampling" wherein each antenna is sampled at a different frequency to ensure that self-interference, including that from digital filtering reject-band aliasing before re-sampling to a common frequency, de-correlates.

A re-sampled common complex sample frequency that works well is f_c=221.1840 Ms/s, explained here in some detail for normal-resolution imaging correlation:

- When channelized with a 16k (i.e. 16,384) channel filterbank, each channel's complex sample rate (and bandwidth) is exactly 13.50 kHz. Thus, within a 16 msec Walsh period, there are exactly 0.016 x 13500 = 216 samples, allowing for integration of an integer number of samples in the sideband separating correlator that follows[27]. For auto-correlations, this doesn't work out

[27] AIthough it must be noted that due to the combined impulse response of the VCC-OSPPFB, the ReSampler, and the 16k CSPPFB, there is a time-smearing effect (dominated by the 16k CSPPFB) of about 7 samples across Walsh phases. These could and likely should be flagged/blanked so that such smearing does not show up in the correlator output.

for an integration time of exactly 1.0 msec, but rather 0.888… msec, or 12 samples per integration, with exactly 18 such integrations within a 16 msec Walsh period.

- Exactly 14880 of the center channels are correlated, providing for a total correlated bandwidth for the Frequency Slice of 14880 channels x 13.50 kHz/channel = 200.8800 MHz, easily covering the center 200 MHz with some overlap (i.e. redundantly correlated channels) with adjacent Frequency Slices. As with Mid.CBF, these 14880 channels allow for post-correlation channel averaging[28] factors of 2, 3, 4, 5, 6, and 10, each factor evenly divisible into 14880 channels.
- If 8 TALON FPGAs (see section 7.1) are used to correlate 14880 channels, it works out to exactly 1860 channels per FPGA. 1860 is also evenly divisible by 2, 3, 4, 5, 6, and 10, which means that each FPGA can perform required channel averaging independently, without having to transport/share channels with other FPGAs in the AFSP.

If AFSP FPGA resource and/or performance becomes an issue, an AFSP can use 10 TALON FPGAs for processing, wherein 1488 channels per FPGA are correlated. This allows for all previously mentioned channel averaging factors except 5, forming a nice risk-mitigation fallback position.

For Zoom Window selection with a /2, /4, …, /64 decimating DDC, followed by a 16k filterbank, the situation isn't quite so perfect but in this case (it is assumed-- see requirement AT.CBF-0101) that sideband separating correlation is not required, just sideband selection.

For zoom/64, the DDC has an output sample rate of 221.184 MHz / 64 = 3.4560 MHz; divided by 16,384 = 210.9375 Hz/channel. If a 16 msec minimum integration time is chosen, it is 3.375 samples per integration, which means there will be some time smearing. If a minimum integration time with zoom/64 of 384 msec (24 x 16 msec) is acceptable, then there are exactly 81 samples correlated per integration. If this isn't acceptable, a zoom DDC for AT.CBF could be developed (TBC) with, say, /3, /6, /9, /18, /36, and /72 zoom factors to provide a (/72) channel bandwidth down to 221.184 MHz / 72 / 16384 = 187.5 Hz, with exactly 3 samples integrated per 16 msec dump[29].

Linearly-spaced channels across Frequency Slices discussion

As mentioned above, a phase-rotator in the [B-1] ReSampler block allows for frequency shifting of the Frequency Slice before the zoom DDC and the 16k imaging channelizer. This, along with re-sampling to f_c=221.1840 MHz, allows for fine-channel center-frequency alignments across Frequency Slices to be the same as fine-channel center-frequency alignment within the Frequency Slice, which means contiguous linearly-spaced channels across all Frequency Slices that source from the same 2 GHz I/F signal. This is explained in further detail in [14] but the key figure illustrating this feature, extracted from the same, is in Figure 6-3 below:

[28] Performed in the FPGA; further channel averaging is possible in the AT.CDP.

[29] Noting that the issue of time smearing across sideband separating Walsh phases does not apply since sideband separation is assumed to not be required in zoom mode (see requirement AT.CBF-0101.)

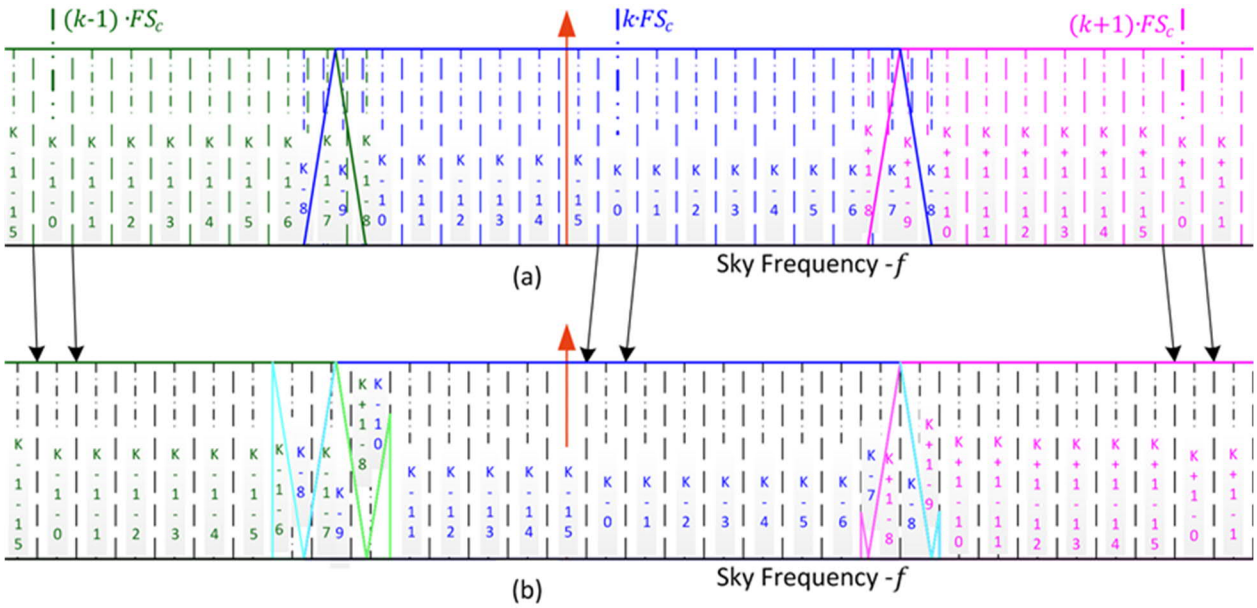

Figure 6-3 Illustrating the generation of linearly-space fine frequency channels across adjacent Frequency Slices (FS.) (a) Non-aligned center frequencies before shifting; (b) center frequencies are aligned after shifting.

Linearly-spaced channels across the adjacent Frequency Slices, and therefore across the entire digitized bandwidth, is an important science capability feature, enabled to some extent by choice of a "convenient" fine channel bandwidth due to the re-sampling function in the ReSampler block, but primarily due to its phase rotator.

6.1.3 VLBI Beamforming signal chain

The complete VLBI Beamforming signal chain—the same as imaging in the "VCC-Part" but different than imaging in the "AFSP-Part"—is shown in Figure 6-4 below annotated, as done for the imaging signal chain diagram, with number of bits per sample, frequencies, and filter response diagrams.

A brief description of each signal processing step in the "AFSP-Part" in Figure 6-4 is as follows:

- The [B-1] ReSampler block is the same as for imaging, except that now the re-sampled output frequency f_c=224.0 Ms/s, and there are two ReSamplers (for each polarization) for each Frequency Slice. This allows for 2 VLBI beams to be independently formed on a delay center within the antenna HPBW for each Frequency Slice. 224.0 Ms/s facilitates Beam-Channel tunable DDCs' output at VLBI standard data rates from 2.0 to 256.0 Ms/s each and, a full Frequency Slice bandwidth output at 448.0 Ms/s. Here is where 90/180 Walsh de-switching for sideband suppression/selection occurs, i.e. each dual-pol beam is only formed on one select sideband. As well, the ReSampler phase rotator can be used to perform frequency shift operations etc. as described for the Imaging Correlation signal chain.
- Thereafter, for each of the 2 beams:
    - The VLBI Beamformer block [E-2] performs a (dual-polarization) complex vector sum of all select antennas forming the beam.

- Block [E-3] performs a complex-to-real conversion using a Hilbert transform on the 224.0 Ms/s Frequency Slice, described in detail in [8] with response shown in the figure.
- Block [E-4] contains 4 (dual-pol) tunable DDCs for real VLBI Beam-Channel outputs from 2.0 to 256.0 Ms/s (1 MHz to 128 MHz bandwidth), described in detail in [8].
- Finally, each Beam-Channel spigot is re-quantized to a selectable 2, 4, or 8 bits/sample with on-command automatic level setting for optimal sensitivity.

- Thereafter, for one select ReSampler output (i.e. one VLBI delay center on the sky):
  - Block [E-5] is a 1k CSPPFB, producing channels that are 224.0 MHz / 1024 = 218,750 Hz wide each, re-quantized to 6+6b. This filterbank has a channel response as indicated, one that is not as flat-topped as the 16k imaging filterbank, to save FPGA resources for its implementation.
  - The center 920 channels are corner-turned in block [E-6] and correlated, without sideband suppression or separation (done in the ReSampler phase rotator above) in the correlator block [E-7]. There is also no post-correlation channel averaging in this correlator.

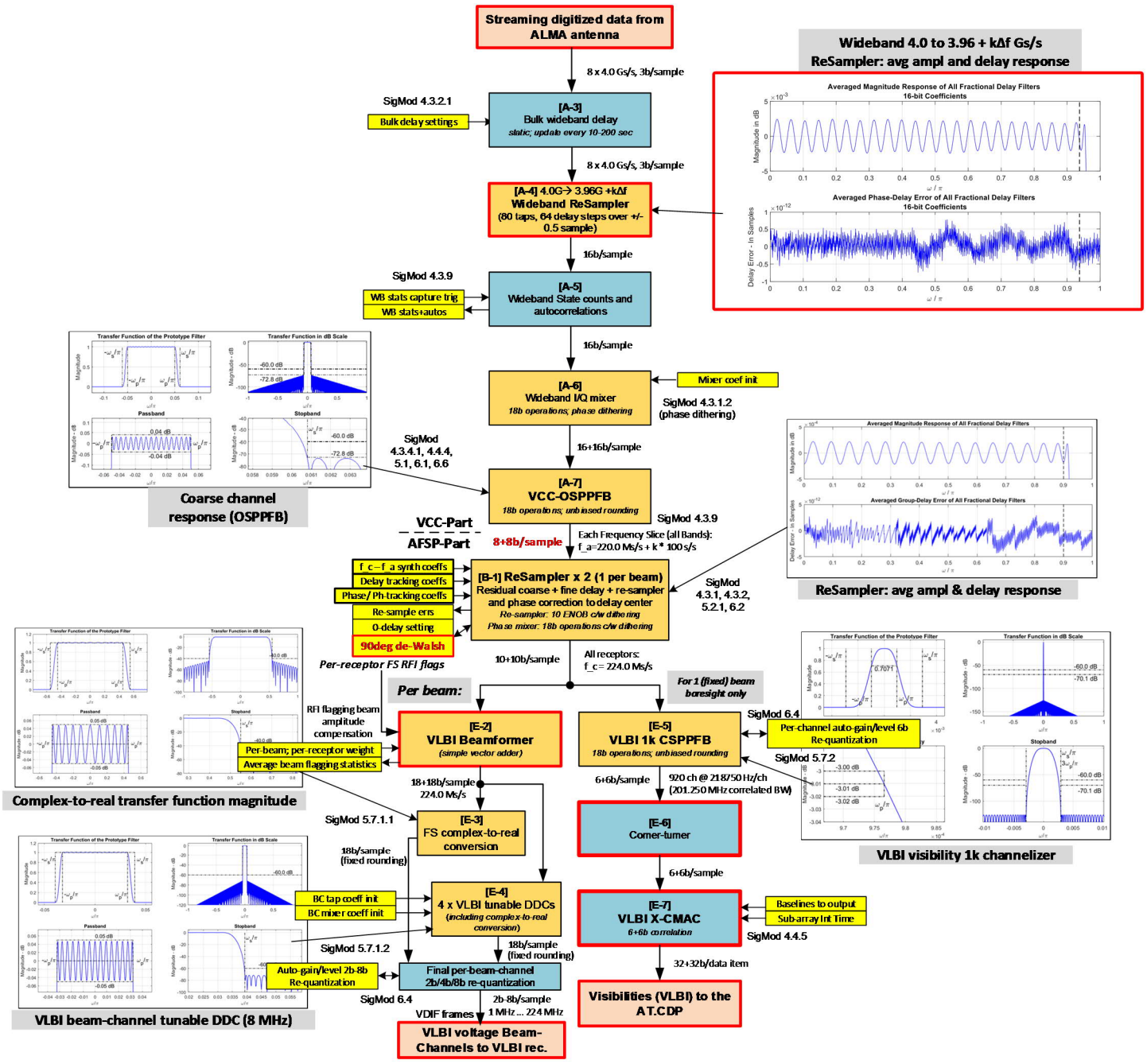

Figure 6-4 VLBI Beamforming signal chain.

6.2 Alternative signal processing chain

The preceding sub-section discussed the signal chain developed for SKA1 Mid.CBF, but with a block added and some blocks changed to facilitate processing for ALMA.

Some of the flexibility in the signal chain that is essential for SKA1 Mid.CBF, may not be as essential for ALMA and so, one might ask, is there a more efficient and/or simpler alternative? This section briefly discusses one alternative and perhaps more conventional approach that could be implemented, but

which has some drawbacks in an over-sampling "FFX" architecture. As well, it would not easily[30] allow for multiple delay centers on the sky within a sub-array for the same digitized data stream.

A key part of this discussion involves definition of the over-sampling factor in the first "F" stage filterbank, of the form A/B, where both A and B are integers. "A" is the number of unique complex channels ("Frequency Slices") that come out of the filterbank. "B" should divide into the digitizer sample rate evenly every T_{rep} seconds (or 48 msec epochs) so that the ingest pipeline, that feeds "super-sample rate[31]" (SSR) streams to the filterbank (i.e. a "commutator" operation), has its SSR phase deterministic every T_{rep} seconds. As the A/B ratio gets smaller, the steepness of the filterbank channel response must increase to ensure aliasing doesn't spill into the passband, requiring more filterbank FIR taps. Also, ideally A is a power of 2 to allow for a radix-2 implementation, the simplest for an FFT, although such is not essential.

For imaging, this alternative signal processing chain includes the following basic steps:

- Wideband +/-0.5 sample coarse delay tracking on the 4.0 Gs/s data streams. This could be implemented in the VCC FPGA, using external DDR4 memory, with appropriate input and output FIFOs and logic. Each stream could undergo a different delay (with the use of separate output FIFOs) to a certain extent to make up for differential RF data paths or to place each stream pair (i.e. pol'n pair) on a different delay center on the sky within the HPBW of the antenna.
- An A/B oversampling coarse filterbank (VCC-OSPPFB) to produce Frequency Slices as in the proposed approach. With an input sample rate of 4.0 Gs/s, and A/B=10/9, the output sample rate of each Frequency Slice is 222.222⋯ Ms/s complex, a decidedly inconvenient sample rate since, within any reasonable epoch (16 msec, 48 msec, 1 second) there aren't an integer number of samples at the Frequency Slice sample rate, nor at the fine channel sample rate. Another common oversampling factor is 8/7, producing a 2.0 GHz/8 x 8/7 = 285.7142857⋯ MHz Frequency Slices, decomposing into 17438.61607⋯ Hz after the 16k filterbank; these numbers are also not only inconvenient for reasons stated, but push FPGA processing clock frequencies into the ~600 MHz range introducing risk in achieving FPGA timing closure, at least in the 14 nm Stratix-10 FPGA on the TALON board. Finally, 11/10 is possible, producing 11 x 200.0 MHz Frequency Slices with the center 10/11 (~182 MHz) un-aliased, decomposing into 12207.03125 Hz channels with similar problems synchronizing with the 16 msec Walsh sequence. 16/15 oversampling is possibly another one to consider.
- Phase-correcting (to the center frequency of) each Frequency Slice, for phase-delay fractional-delay correction. This leaves a residual phase—different for each fine channel—that should be corrected before visibility output (such as a phase correction after the 16k imaging filterbank), or possibly corrected in post-processing. This phase corrector can also do sideband suppression, frequency offset removal, and frequency shifting for fine-channel alignment across adjacent Frequency Slices. Alternatively, phase-delay could be entirely performed on fine channels, but this means that coarse 1-sample delay jumps ("clunks") propagate through the very long 16k

[30] Some off-boresight steering is possible with just phase delay, but the offset is limited and depends on array extent.

[31] A term used in industry to refer to parallel processing of time-de-multiplexed data streams rather than the at-sample-rate stream, to allow processing to occur at clock frequencies possible in digital logic.

imaging poly-phase filterbank, which should be blanked to avoid imprinting a delay-rate-dependent coherence loss and phase anomaly on imaging visibilities (for ALMA, with little to no narrowband RFI, it is possible that the number of taps in the 16k poly-phase filterbank could be reduced to reduce the propagation time through the filterbank, which also relaxes channel-to-channel isolation and bandpass ripple.) This option also entails significant data management overhead in the correlator to ensure the right phase is applied to the right fine channel at the right time.

As well as all of the above, these inconvenient Frequency Slice and fine channel sample rates:

- Make the state of the entire signal chain after the VCC-OSPPFB, depend on the previous state, without the reasonable possibility of synchronizing it to a known state every 48 msec, 1 second, or reasonable multiple thereof (TBC.) This makes synchronizing integration times across AFSPs so that they are aligned for the same sub-array difficult if not practically impossible.
- Couple AFSP processing sample rates to the original digitizer sample rates, something that could become limiting and problematic when transitioning/upgrading to ALMA 2030 digitizers.

For VLBI, the visibility signal chain has similar issues to the above. For the beamformer, all beamforming operations could occur at the Frequency Slice sample rate with re-sampling after beamforming to produce sample rates that are VLBI-standard, but again synchronizing to a known epoch every so often is difficult if not impossible.

Notwithstanding everything stated above, this alternative signal processing chain approach could be implemented, but would entail a significant delta in NRE to work out, study, design, implement, and test all of the steps.

Proposed vs alternative architecture discussion

Both the proposed TALON/FSA and alternative architectures have much in common. The main difference is that the proposed architecture performs fractional delay correction/tracking in the time domain using a true delay FIR filter, whereas the alternative applies phase delay in the frequency domain after coarse and fine channel filtering.

To ensure the time domain/true delay filter output doesn't have a delay-rate effect on visibility amplitudes and phases (i.e. as delay slowly steps through all 1024 sets of tap coefficients between 0 and 1 sample of delay, each of which has a slightly different gain and phase response), re-sampling to a sufficiently different frequency is essential, so that the average amplitude and phase response of the ReSampler's sets of tap coefficients is obtained. Re-sampling does have some processing overhead, but as discussed above, all data x tap coefficient calculations are performed using ~1/2 of the (M20K) small-block distributed memory in the TALON VCC Stratix-10 FPGA.

The true delay filter implementation is a much simpler implementation and data management approach than phase delay, since final coarse and fine delay tracking occurs in one place and that is in the ReSampler (synchronized to a bulk delay change[32].) Once applied there, no additional phase or

[32] The incoming polynomial delay models are split into bulk and dynamic residual delays, with the bulk delay set in the VCC and the residual implemented in the ReSampler; the bulk delay component is changed concomitant with the residual on a cadence of every ~100s or so, as mentioned previously.

amplitude corrections or tweaks are needed in the real-time signal chain; any post-correlation gain corrections are pre-determined for a given AT.CBF configuration, time-invariant, and provided by AT.CBF for use (see requirement AT.CBF-0302.) The 64-tap, 1024-delay step [8] ReSamplers in AT.CBF's Imaging Correlation AFSPs consume ~2560 multipliers out of 11,520 and 2560 M20K memories out of 11,721 in the Stratix-10 SX2800 FPGA or ~22% of its resources (double this for the VLBI Beamforming AFSP.)

A phase-delay implementation is certainly possible however it entails more data management overhead of transporting, calculating, and applying phases and phase residuals at the various application points at the correct time—on Frequency Slices and then fine channels (residual), or just the latter if all phase-delay is applied on the fine channels. FPGA resource use for phase delay management and application is not known since this option has not been studied in detail.

The proposed architecture therefore has perhaps some small logic hardware overhead, but a much simpler implementation than the alternative phase delay. That, and the fact that many signal processing blocks in AT.CBF are copies or slight modifications of SKA1 Mid.CBF blocks and so have a low to zero NRE delta, the ReSampler allows for multiple delay centers on the sky with a Frequency Slice granularity, and the ReSampler de-couples fine channel bandwidth and sample rates from the antenna digitizer, makes the choice for the proposed AT.CBF implementation clear.

7 AT.CBF physical architecture, TALON Technology, and FPGA designs

This section presents the results of developing a physical architecture that will meet AT.CBF requirements defined in section 5, using TALON board & FPGA technology. Much of this work builds on the development of the SKA1 Mid.CBF system and is therefore well-supported with many person-years of effort.

7.1 AT.CBF physical architecture—data connectivity, data flow, and timing

Figure 7-1 is a simplified block diagram of the AT.CBF physical architecture and key data flows:

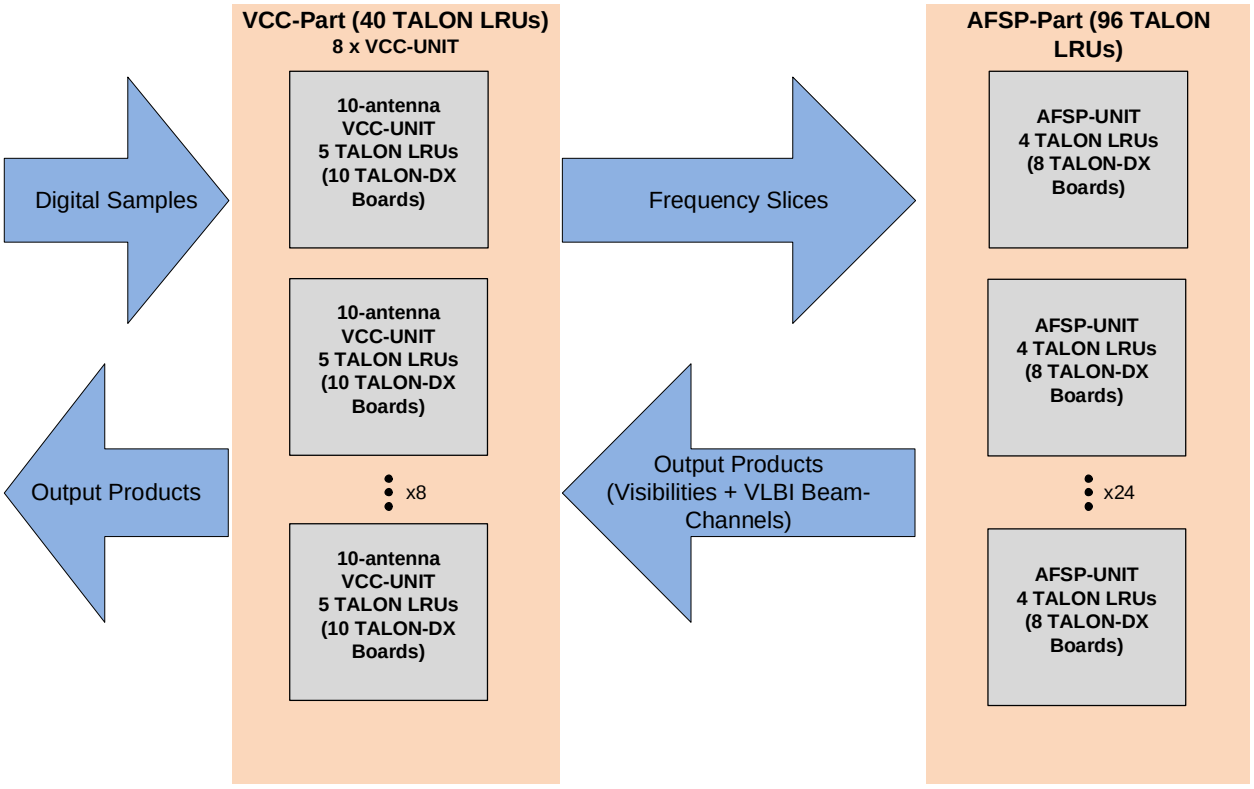

Figure 7-1 Simplified block diagram of the AT.CBF physical architecture.

In this diagram, digitized data from ALMA antennas flows from left to right and output data products flow from right to left, with final outputs to the AT.CDP (Switch) using either 40G or 100G Ethernet optics. This approach takes advantage of the full-duplex MBOs (optical modules) that are used in the TALON LRU to consolidate output data products produced in AFSP-UNITs[33] and flowing to the AT.CDP. Not shown is a huge unused output bandwidth from AFSPs' TALON LRUs that could be used, if desired, for a much higher output bandwidth pipeline (16 x 100G links for each of 24 AFSP-UNITs.)

A more detailed block diagram of AT.CBF is shown in Figure 7-2:

[33] The "UNIT" designation, as will be seen, is to denote a "convenient collection of TALON LRUs" for a specific purpose (such as an AFSP), or to allow fiber bundle groupings (such as for the VCCs).

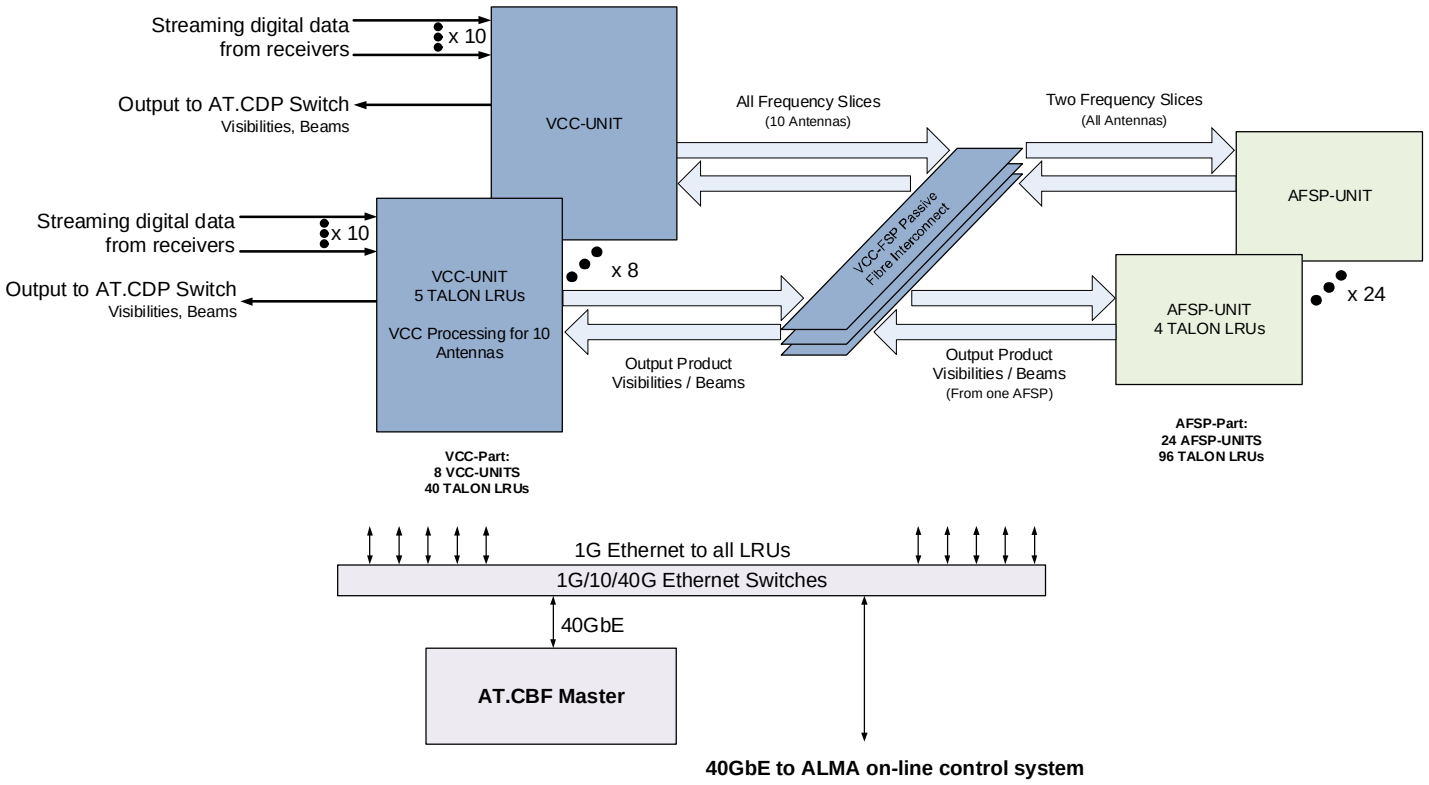

Figure 7-2 A more detailed block diagram of AT.CBF processing nodes and connectivity.

This diagram shows VCC-UNIT to AFSP cross-connect functionality for both data flow directions, but not precisely how it is accomplished. Figure 7-3 shows, in more detail, intra-connectivity in AT.CBF. A VCC-UNIT is chosen to be 5 TALON LRUs (10 TALON-DX boards/Stratix-10 FPGAs), where each FPGA performs VCC processing for 1 ALMA antenna. The grouping of 10 allows 1 fiber, containing 2 Frequency Slices, from each of 10 antennas to be grouped into an MTP-24 fiber connector (12 transmit, 12 receive.) Then, 8 such 10-antenna fiber groupings on 10 MTP-24 fiber cables, containing a pair of Frequency Slices, route—point-to-point—to a single AFSP-UNIT. Each MTP-24 fiber cable, containing 10 antennas' 2 Frequency Slices, plug into an MTP-24 port of a TALON LRU, with 2 such ports in each of 4 LRUs populated. Thus, an AFSP-UNIT has data for 2 Frequency Slices from all 80 antennas.

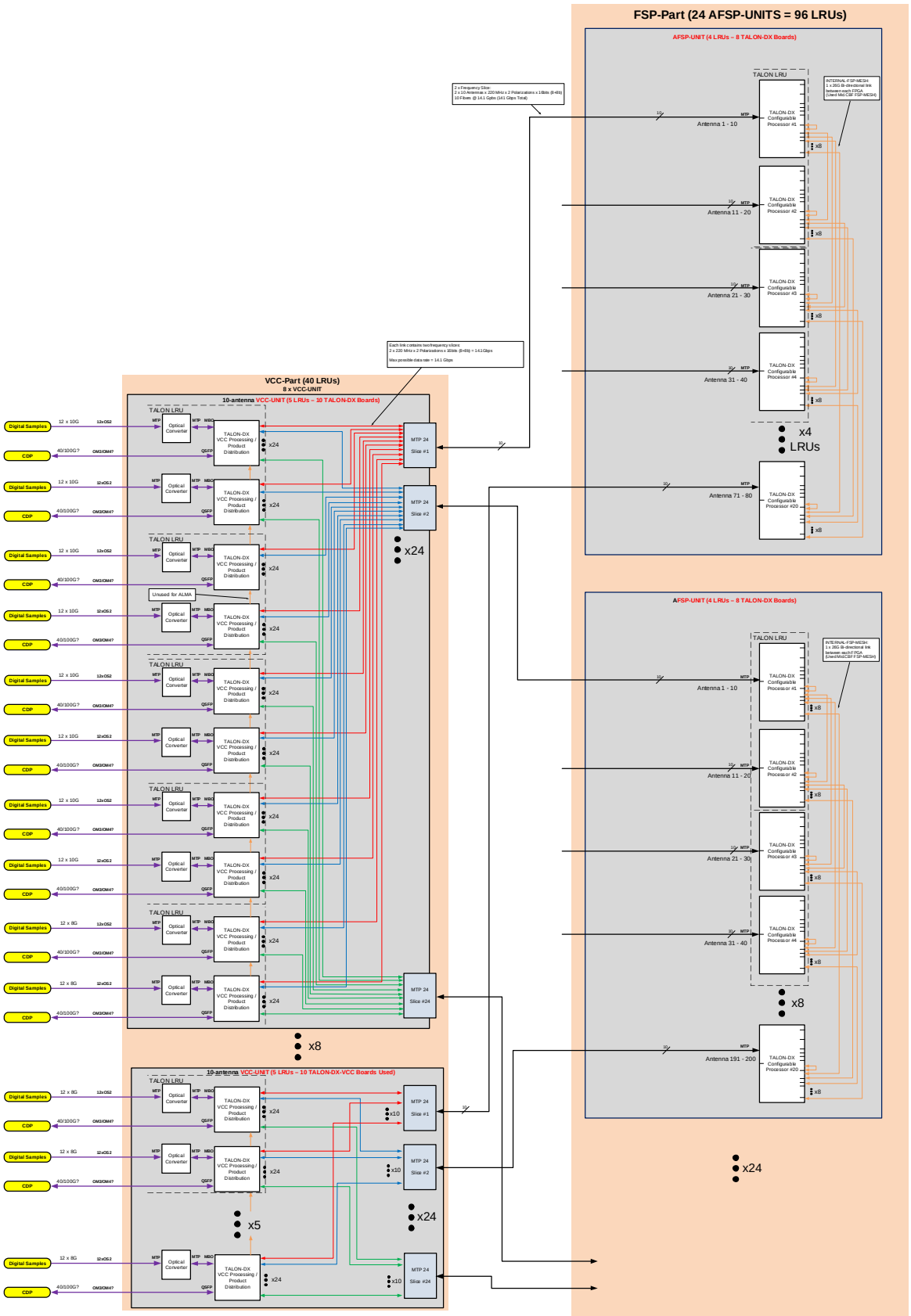

Figure 7-3 AT.CBF detailed connectivity diagram.

Within each AFSP-UNIT, after the ReSampler and 16k fine filterbank (and similar for the VLBI signal chain), 1/8th of the 14880 channels to be correlated (i.e. 1860) for all 80 antennas, are distributed to all FPGAs via a fiber mesh internal to each AFSP-UNIT. Thus, each AFSP TALON Stratix-10 FPGA performs both antenna-based (ReSampler, filterbank) and baseline-based (correlation, beamforming) processing, with a uniform processing load distribution across FPGAs.

Once visibilities and beams are formed, the partial-result output from each FPGA (and in the case of VLBI beamforming, the final 80-antenna beamformed output), flows back to the VCC-UNITs in the opposite direction, but on the same fiber and fiber bundle path, as the Frequency Slices to be processed. One (or two) of the unused 40G[34] or 100G ports of the TALON-DX board are then used to transmit output data products to the AT.CDP Switch, for distribution to AT.CDP processing nodes and VLBI recording equipment. There are therefore 80 such 40G or 100G ports of data flowing to the AT.CDP switch, although fewer could be used.

The fiber meshing connections in the VCC-UNIT and AFSP-UNIT of Figure 7-3 seem complicated, but a clean, packaged, user-defined COTS solution exists, where each such mesh circuit consisting of MTP-24 (i.e. 12 transmit, 12 receive) connector ports, is packaged in a passive 1-U rack-mount LRU. Figure 7-4 is a picture of such a mesh circuit contained in a 1-U LRU (the LRU itself not shown.) There is one such mesh design for the VCC-UNIT and one for the AFSP-UNIT, both of which may be the same as Mid.CBF.

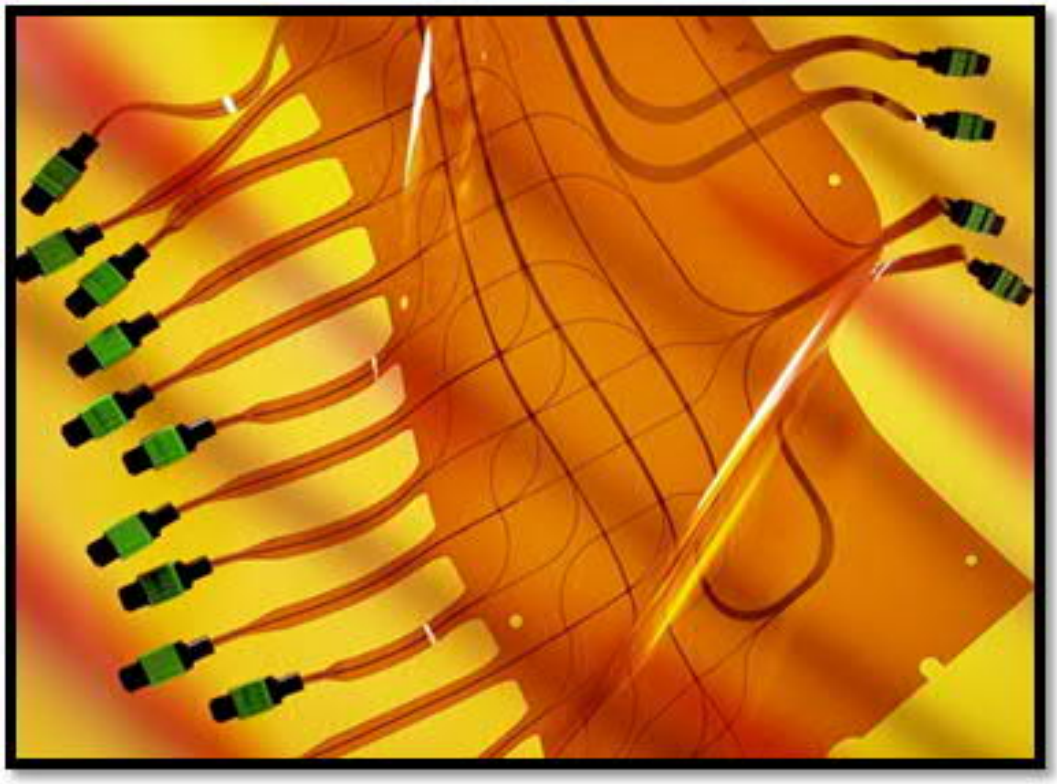

Figure 7-4 Photo of a passive fiber mesh circuit with MTP-24 fiber connector I/Os, each packaged in a 1-U LRU (not shown.)

[34] i.e. the TALON-DX board contains dual QSFP28 optical module "cages", each of which can be populated with a 40G or 100G module.

Thus, all connections between TALON LRUs and mesh LRUs use 24-multi-mode fiber cables and MTP-24 connectors and all are point-to-point.

With these connections and meshes in place, with appropriately-chosen Frequency Slices and fine channel sample rates, and with synchronization signaling and timing distributed to all TALON-LRUs via "Timecode" (see below) and embedded in data streams, each VCC-UNIT FPGA and AFSP-UNIT FPGA performs all processing within its own context without regard to other FPGAs. Furthermore, for AT.CBF there are two[35] flavors of TALON LRU—one to be used in VCC-UNITs and one to be used in AFSP-UNITs, so the number of different AT.CBF electronics modules that have to be sourced and maintained is minimal.

The proposed AT.CBF (and SKA1 Mid.CBF) is designed to be provided with a reference clock and epoch, derived from the Central Timing Reference (CTR) of the telescope. For AT.CBF, this is a 125 MHz reference clock and a 48 msec epoch, synchronous with the antenna Walsh cycle and coincident with a UTC 1-PPS every 6 seconds (TBC.) The 125 MHz clock is a "digital quality" clock, meaning that its jitter and phase wander performance compared to the digitized data streams only needs to be such that the FPGA can lock onto the clock and that internal elastic buffers don't overflow, which could occur if there were too much low-frequency phase wander c/w the CTR.

The 125 MHz and 48 msec are ingested into a select VCC-UNIT TALON LRU (or 2, for 1+1 redundancy) and then distributed to all TALON LRUs in the system using 125 Mbps fiber optics and Timecode mesh optical circuits ("TCD-MESH") similar to those just described. The 125 MHz and 48 msec ingest LRU also gets UTC time, via an NTP server, to tag each epoch (1 sec and 48 msec) in Timecode with actual UTC. Thus, each TALON FPGA gets time and a clock it can use for developing its internal processing clocks, and when sync'd to them (see [7] for further details, including synchronization for delay tracking), can operate without regard to other FPGAs.

If a CTR 125 MHz and 48 msec epoch are not available to provide to AT.CBF, then a small FPGA circuit in a separate LRU, fed at least one copy[36] of streaming digitized data from an ALMA antenna, can be used to produce them for AT.CBF use. In principle an asynchronous design is possible wherein there is no reference 125 MHz or 48 msec, both essentially being derived from the streaming data. However, in this case, AT.CBF could not recover (to the same phase) from a link dropout to an antenna (see requirement AT.CBF-0402), since there isn't a packet counter in the streaming data of sufficient length [16] and, at least the primary author of this report maintains, is a more complex and less robust approach.

Looking under the hood in a bit more detail, Figure 7-5 shows the use of fiber optic modules inside the AT.CBF VCC-UNIT and connections to equipment external to the VCC-UNIT. Heavy use is made of Mid-Board Optical (MBO) modules, the one on the TALON-DX board being the FCI LEAP MBO, with 12 Tx and 12 Rx multi-mode fibers at up to 25G each. The "Optical Converter" module (see below) is needed to convert 12 single-mode fibers from each ALMA antenna, to multi-mode for ingest into the FPGA via an FCI LEAP MBO on the TALON-DX board.

[35] Needed because of 10G optics media converters required for ALMA antenna digitized data ingest into VCC-UNIT TALON FPGAs, as will be discussed later, although AFSP-UNITs could be populated with this module if desired even though it is unused.
[36] In practise, more than one copy is required for fault-tolerance.

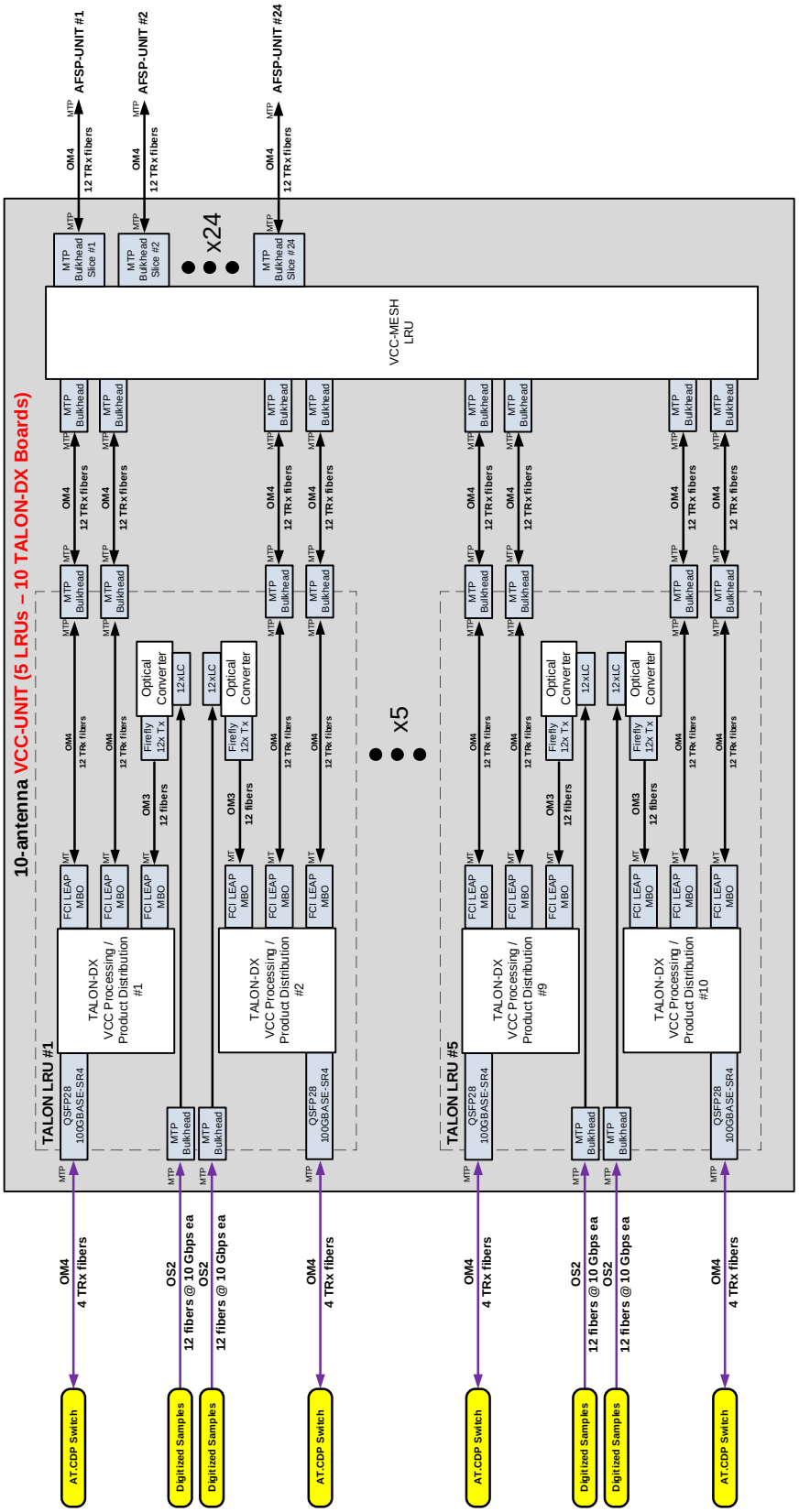

Figure 7-5 AT.CBF VCC-UNIT fiber module/connectivity detail.

Not shown in Figure 7-5 is the fact that there is spare MBO bandwidth that, if used, allows for up to 44 AFSPs in AT.CBF (replacement for the existing BLC), for more concurrent (with full bandwidth imaging correlation) Zoom Window and/or VLBI beamforming bandwidth than the costed 24 AFPs. Such would require a different VCC-UNIT mesh design and 20 more AFSPs (80 more TALON LRUs), but no additional design work. For AT.CBF-2030, costed here for 48 AFSPs, up to 88 AFSPs could be employed assuming TALON-DX implementation—see section 11.2 for further discussion about AT.CBF (BLC replacement) to AT.CBF-2030 migration.

A block diagram of the "Optical Converter" module in the VCC-UNIT TALON LRUs, including connectivity to it, is shown in Figure 7-6:

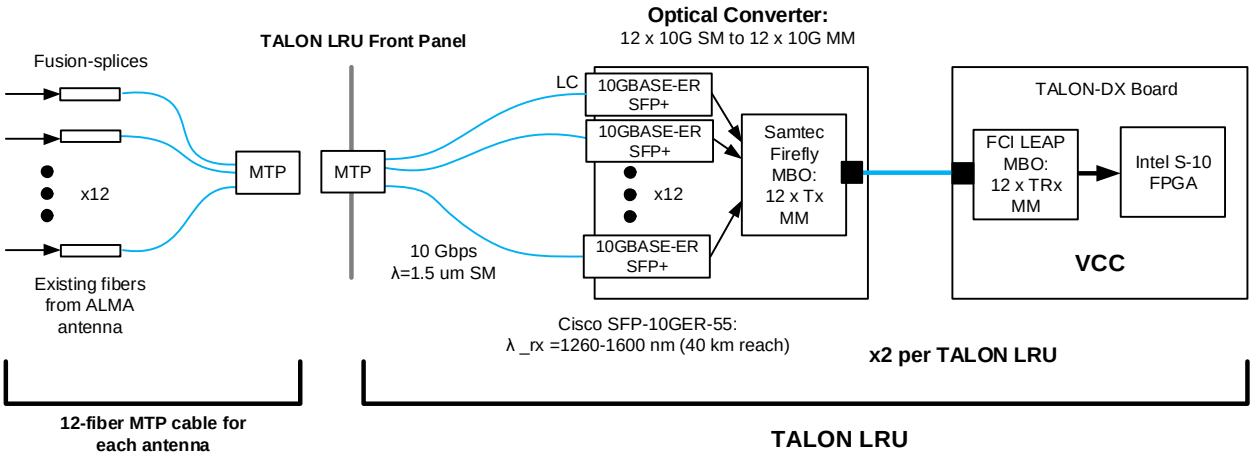

Figure 7-6 Optical Converter and connectivity for AT.CBF to replace the existing BLC.

The Optical Converter contains 12 x SFP+ cages, populated with (for example) 10GBASE-ER SFP+ fiber optic modules with wavelength compatible with the current ALMA 10G 1.5 µm optical transmitters. These get converted and consolidated into a 12 multi-mode fiber ribbon cable using a Samtec FireFly 14G MBO for connection to a TALON-DX FCI LEAP MBO. See Figure 7-17 for further information about this module and how it might be integrated into VCC-UNIT TALON LRUs. For AT.CBF-2030, this Optical Converter module very likely won't be required since more modern fiber-optics will presumably be used.

Figure 7-7 is a more detailed view of the AFSP-UNIT, similar to Figure 7-5 for the VCC-UNIT. If more TALON-DX FPGAs are required for AFSP processing (as mentioned in section 12.2), say 10 rather than 8, the AFSP-UNIT grows in size by 2U (a TALON LRU is 2U in height), the AFSP-MESH is built for 10 rather than 8 MTPs[37] for input data from VCC-UNITs, each FPGA processes 8 instead of 10 antennas and correlates fewer channels, but otherwise the design and function of the AFSP is the same.

[37] And the VCC-UNIT is downsized to 4 TALON LRUs to provide 8 antennas on a VCC-MESH MTP output.

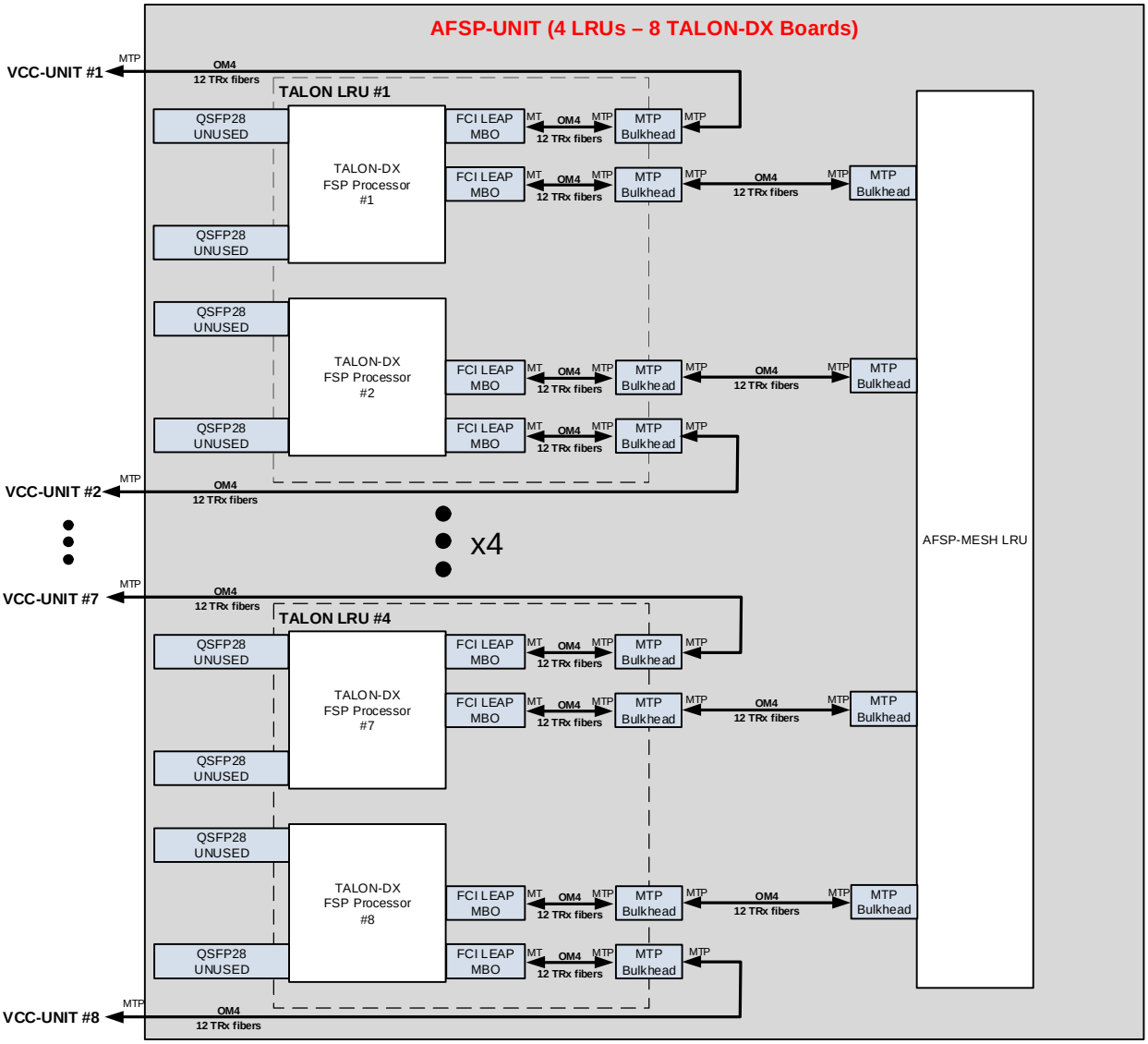

Figure 7-7 AT.CBF AFSP-UNIT fiber module/connectivity detail.

All of the TALON LRUs, fiber mesh boxes, Ethernet switches, and server CPUs must be placed in racks in a real system. A notional profile of a Signal Processing Rack "stack up" is shown in Figure 7-8 (although as discussed in section 11.2 a 2U form factor for the VCC-MESH allows for ALMA 2030 transition.) This shows dual 1U (1/10G) Ethernet switches for 1+1 fault-tolerant redundancy of M&C communications to embedded processors in TALON-DX FPGAs, if desired. There is only 1U of spare vertical space in this stack up—if 5 TALON LRUs are required for the AFSPs as previously discussed, then only two AFSPs (and a VCC-UNIT) fit in a rack and so more than 8 such racks are required, or a 48U rack is used instead.

Additional racks are required for the AT.CBF Master CPU server, Ethernet switches, and the AT.CBF, not shown or studied in further detail in this report. Likely another 2-4 racks, depending on AT.CDP processing requirements, are needed.

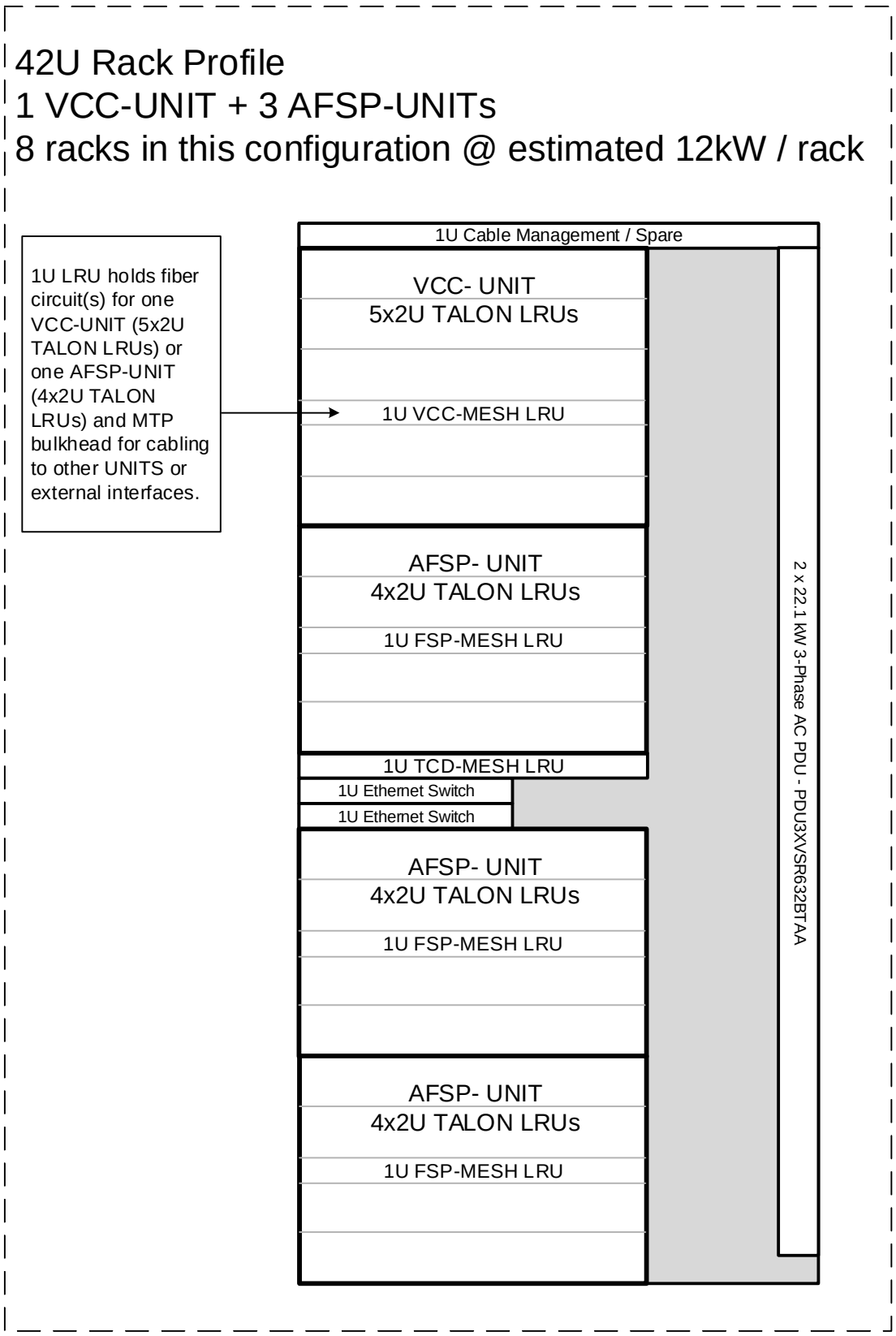

Figure 7-8 AT.CBF Signal Processing Rack profile for a standard-height 42U server rack.

7.2 TALON Technology

The TALON LRU designed, prototyped, tested, and planned for SKA1 Mid.CBF construction contains two "TALON-DX" PCB assemblies ("boards"), each one featuring the largest Intel Stratix-10 FPGA available, the SX-2800. This FPGA contains, among other things, 64 25G SERDES (serial transmit/receive) channels, ~11,000 18-bit multipliers operating at up to 500 MHz each, 4 DDR4 DIMM I/O channels, and a quad-core embedded ARM processor referred to as the "HPS" (Hard Processor System.) This FPGA is in a 50 mm x 50 mm package and can dissipate in excess of 200 W, including up to 200 A of core current at 0.85 V. This, coupled with the many high-speed I/Os used, makes board design challenging compared to previous generations. These challenges have been overcome by using advanced Mentor Graphics signal integrity design and modeling tools and 4 "spins" of prototyping[38] with 13 prototypes built and the latest believed ready for pre-production prototypes. However, the processing and I/O capacity of the FPGA is the key enabling technology for SKA1 Mid.CBF and for the AT.CBF proposed here.

A block diagram of the TALON-DX board is shown in Figure 7-9. Key features of this board are as follows:

- Intel Stratix-10 SX280 FPGA. A uSD card and fast bitstream ("FPGA executable 'program'") boot via the HPS (on-chip hard processor) allows for FPGA bitstream configuration, including partial configuration[39], in ~5 sec, essential for SKA Mid.CBF fast Band changes. The uSD card contains all FPGA bitstreams needed for its deployment in the AT.CBF system namely the VCC and the AFSP Imaging Correlation and VLBI Beamforming Function Modes, and new bitstreams may be uploaded into the uSD card whilst in-system. The uSD card is also used to hold the Linux OS and software executables. The HPS runs Linux, has one dedicated DDR4 DIMM with 64 GB nominal capacity, internal Avalon/AXI-4 bus access to FPGA code blocks, and dual 1 Gb Ethernet connections to the outside world.
- JTAG connector for direct loading of bitstreams into the FPGA and initialization of the uSD card.
- 4 x FCI LEAP 12 Tx/Rx 25G MBO fiber modules to provide all intra-AT.CBF high-speed serial connectivity (i.e. via the VCC-MESH and AFSP-MESH), as well as ingress from the "Optical Converter" (Figure 7-6) module for streaming antenna data. A 5th MBO is populated with 8 Tx/Rx 25G channels for dual 100G Ethernet (on multi-mode fiber) or other use (such as AFSP expansion.)
- Dual QSFP28 cages, meant for40G or 100G QSFP fiber optic modules, each of which may be short-reach multi-mode or long-reach (up to 40 km) single-mode.
- 4 x DDR4 DIMMs, 1 for the HPS and 3 connecting to FPGA "fabric"[40].

[38] One spin of which incorporated changes due to alignment of the PCB material weave relative to 25G copper traces causing destructive impedance discontinuities, fixed with a ~10 degree rotation between the two!
[39] Wherein only select parts of the FPGA are re-configured with a partial bitstream. The utility in this for AT.CBF is that it allows all DDR4 and SERDES I/O to remain active whilst the core function (e.g. Imaging Correlation or VLBI Beamforming) is changed.
[40] A term used to refer to programmable logic in the FPGA.

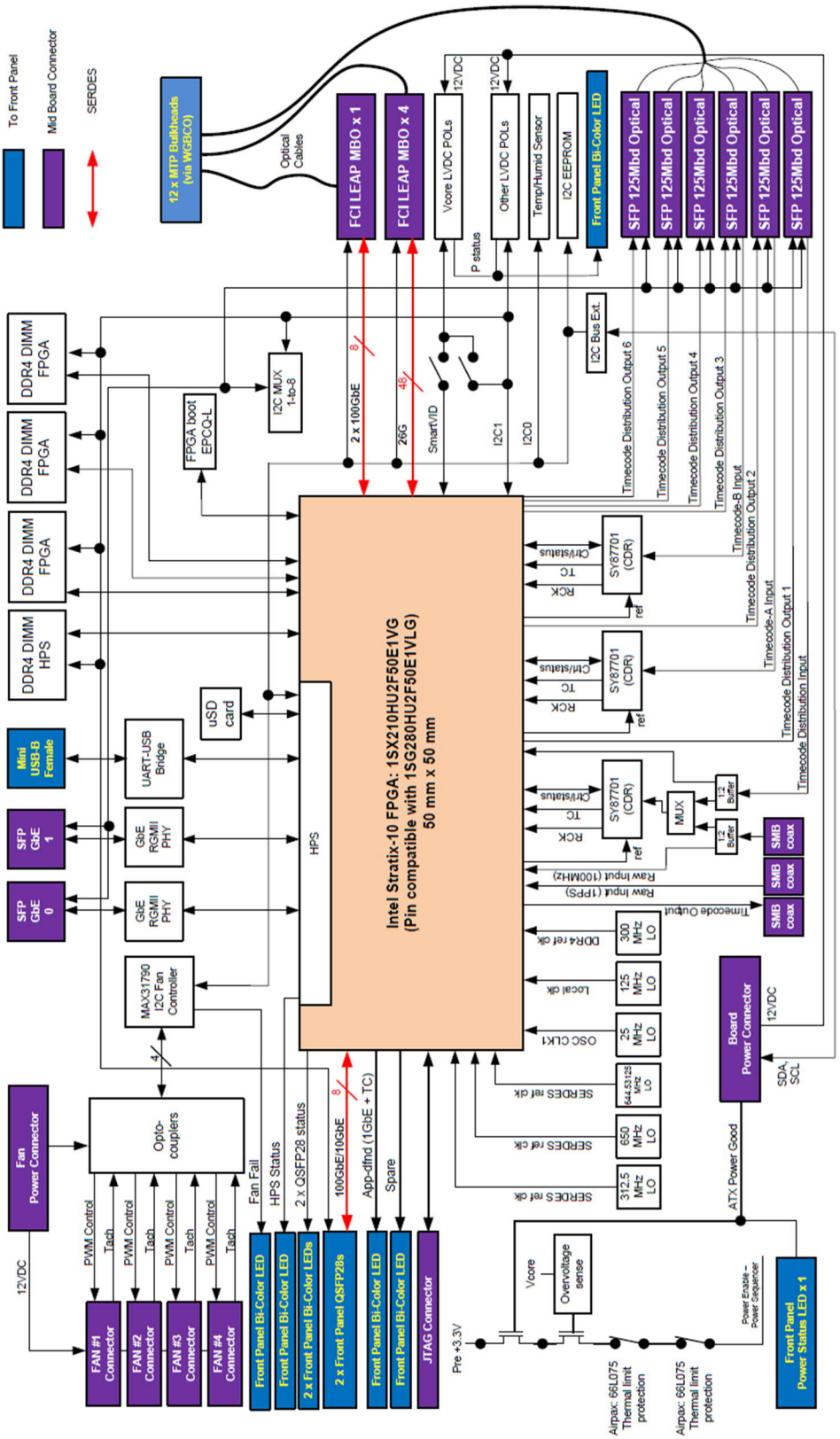

Figure 7-9 TALON-DX board block diagram.

- Multiple SFP 125 Mbps optical cages for Timecode distribution in AT.CBF.
- 3 coaxial connectors for clock I/O. In AT.CBF, one is used for the 125 MHz reference and one is used for the 48 msec pulse/square-wave (TBC.) The other connector is a programmable output from the FPGA.
- Connectors and controllers for 4 cooling fans.
- Multiple crystal oscillators for the various I/O channels (serial, DDR4) and for the HPS.
- Dual redundant dead-man thermal overload protection to prevent thermal runaway in the event of cooling system failure.
- +12VDC main power supply connector as well as a separate main power supply connector for the fan power.
- Stacked-fin copper heatsink (see Figure 7-12) for front-to-back air-cooling designed for the DX board complete with FPGA backing structure (see Figure 7-13) to avoid board warpage.

A layout diagram of major components of the TALON-DX board is shown in Figure 7-10 and a picture of a populated board, without the stacked-fin heatsink is shown in Figure 7-11[41]. Figure 7-12 shows the board with the copper stacked-fin heatsink in place, and Figure 7-13 shows the rear side of the board with the FPGA backing structure needed to ensure the board doesn't warp when the heatsink is fastened.

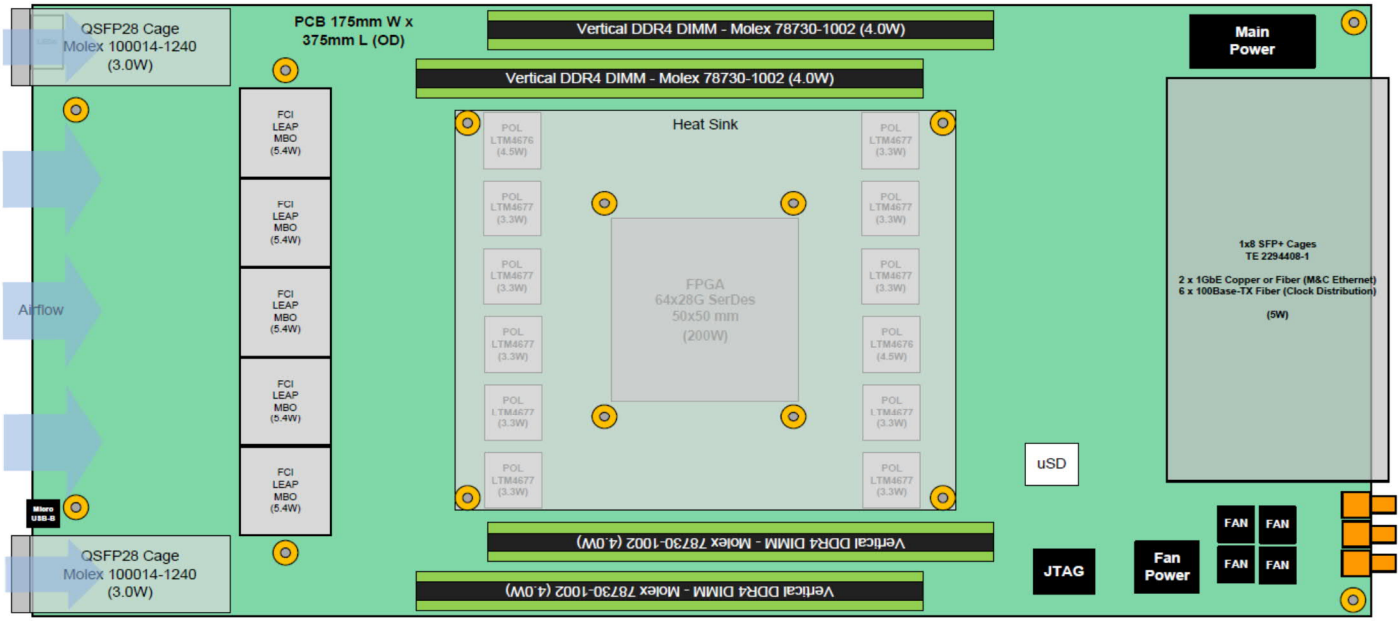

Figure 7-10 TALON-DX board layout diagram showing major components.

[41] More recently-constructed semi-production TALON-DX boards and LRUs are available, however pictures aren't due to COVID-19 NRC site access restrictions.

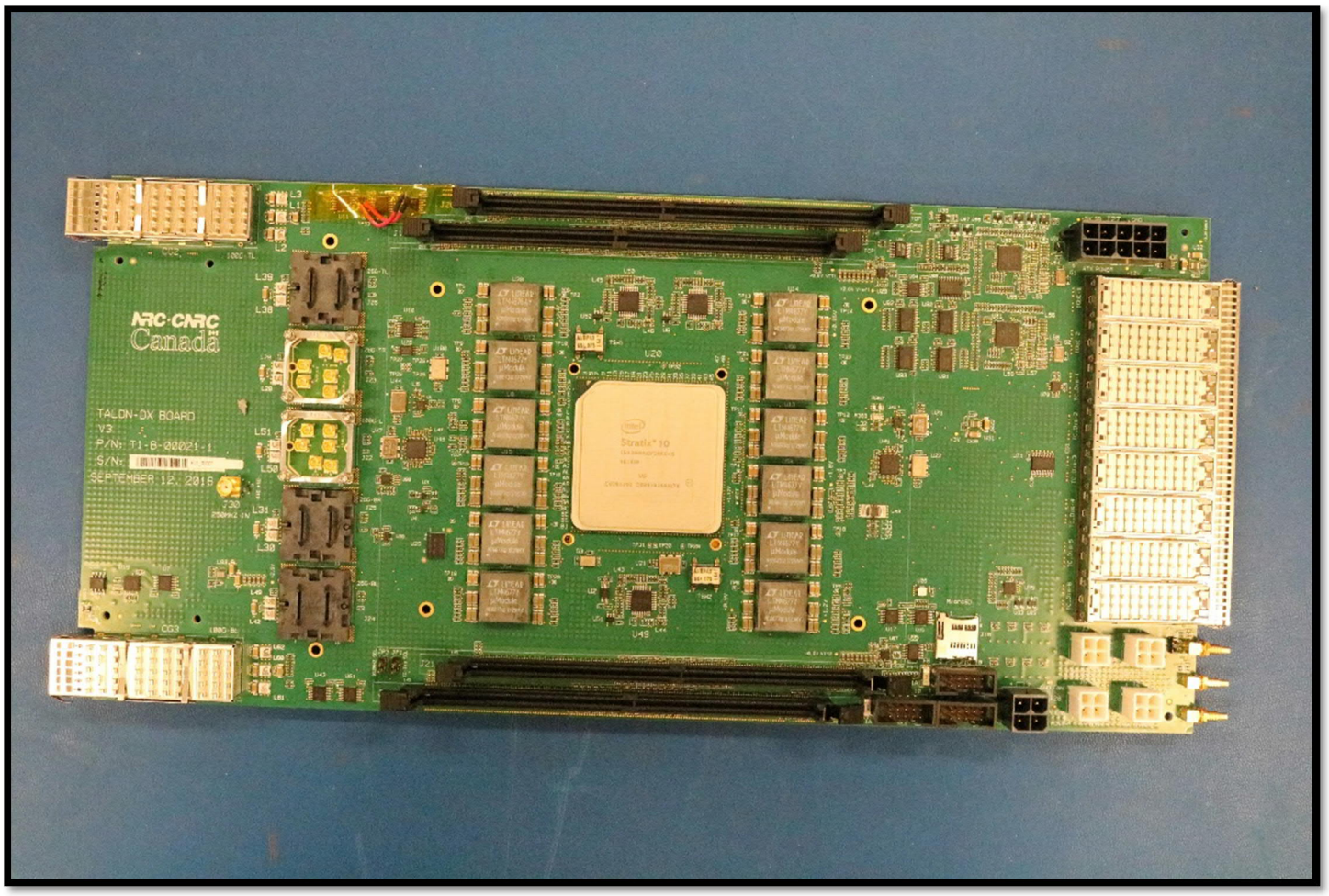

Figure 7-11 TALON-DX board front view without the stacked-fin heatsink. The Intel Stratix-10 FPGA is in the center and the square chips surrounding it are LVDC (Low Voltage DC) power supplies, at up to 26 A each, supplying it with power.

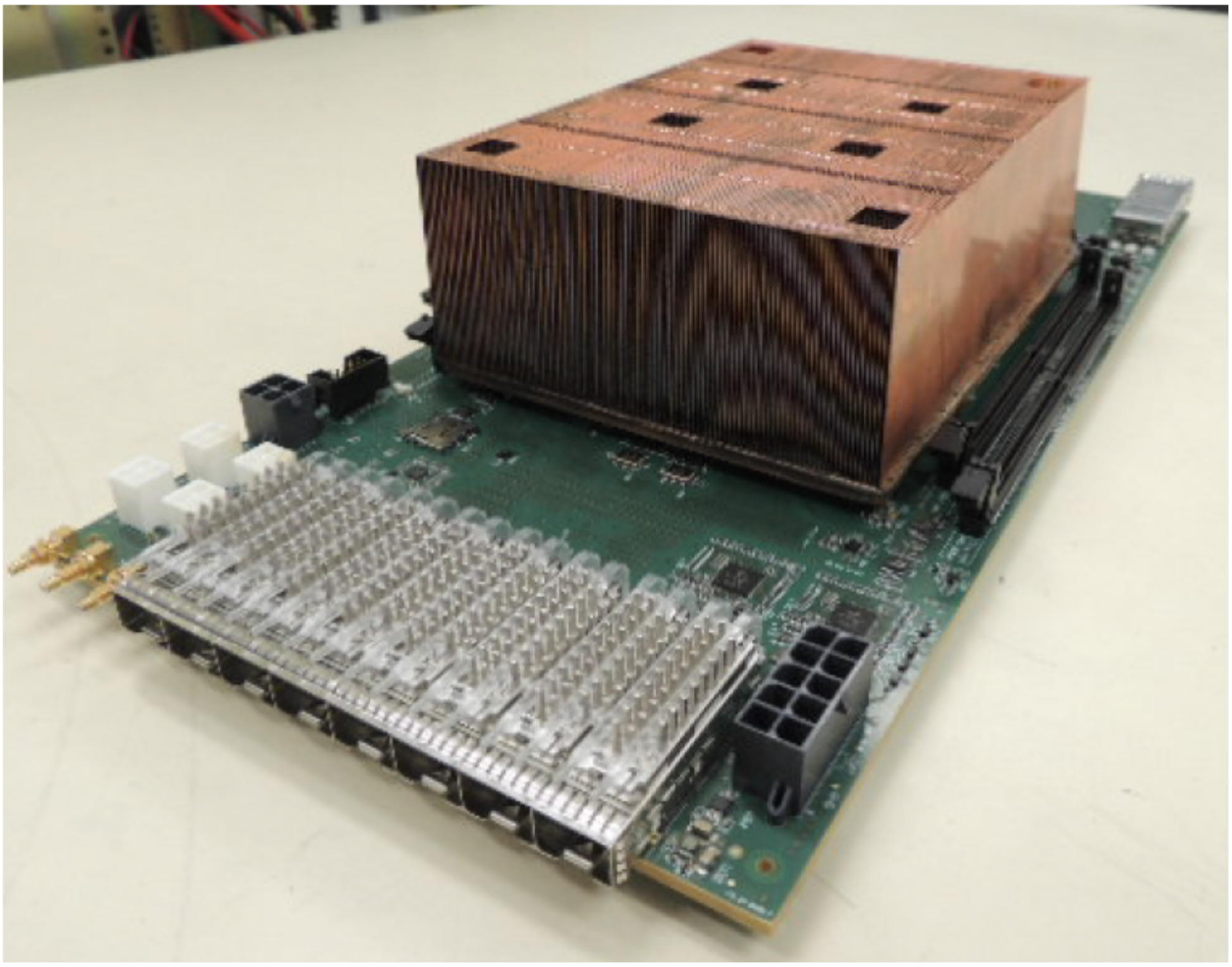

Figure 7-12 TALON-DX board with the copper stacked-fin heatsink attached.

Figure 7-13 TALON-DX board showing the rear side FPGA backing structure.

As mentioned, two TALON-DX boards are mounted in a TALON LRU (Line Replaceable Unit) and pictures of it, undergoing prototype testing are shown in Figure 7-14 through Figure 7-16:

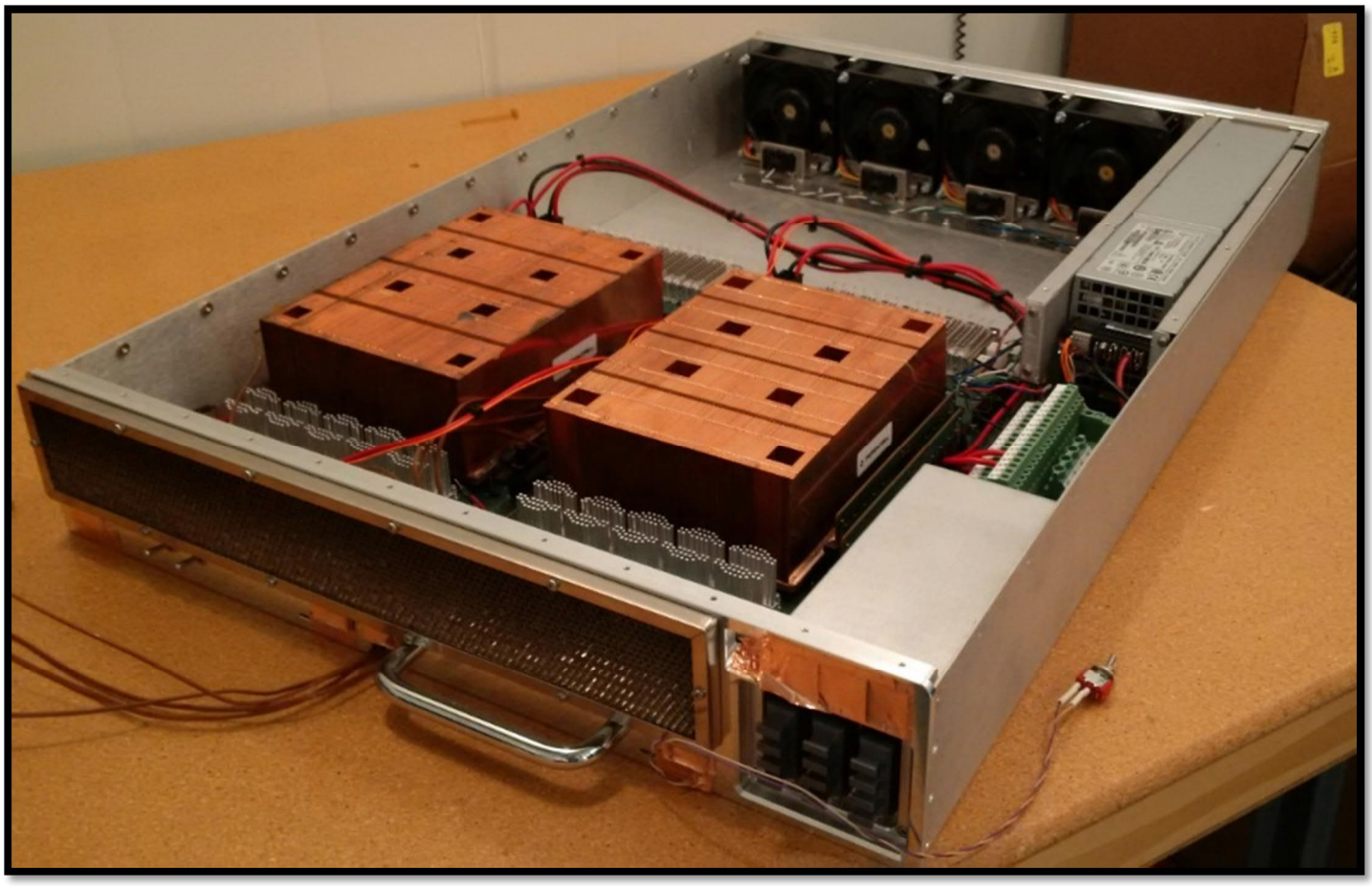

Figure 7-14 TALON LRU prototype under test showing dual TALON-DX boards c/w copper stacked-fin heatsinks. The MBOs' pin-fin heatsinks are visible. The terminal block (center-right) is for prototype testing only.

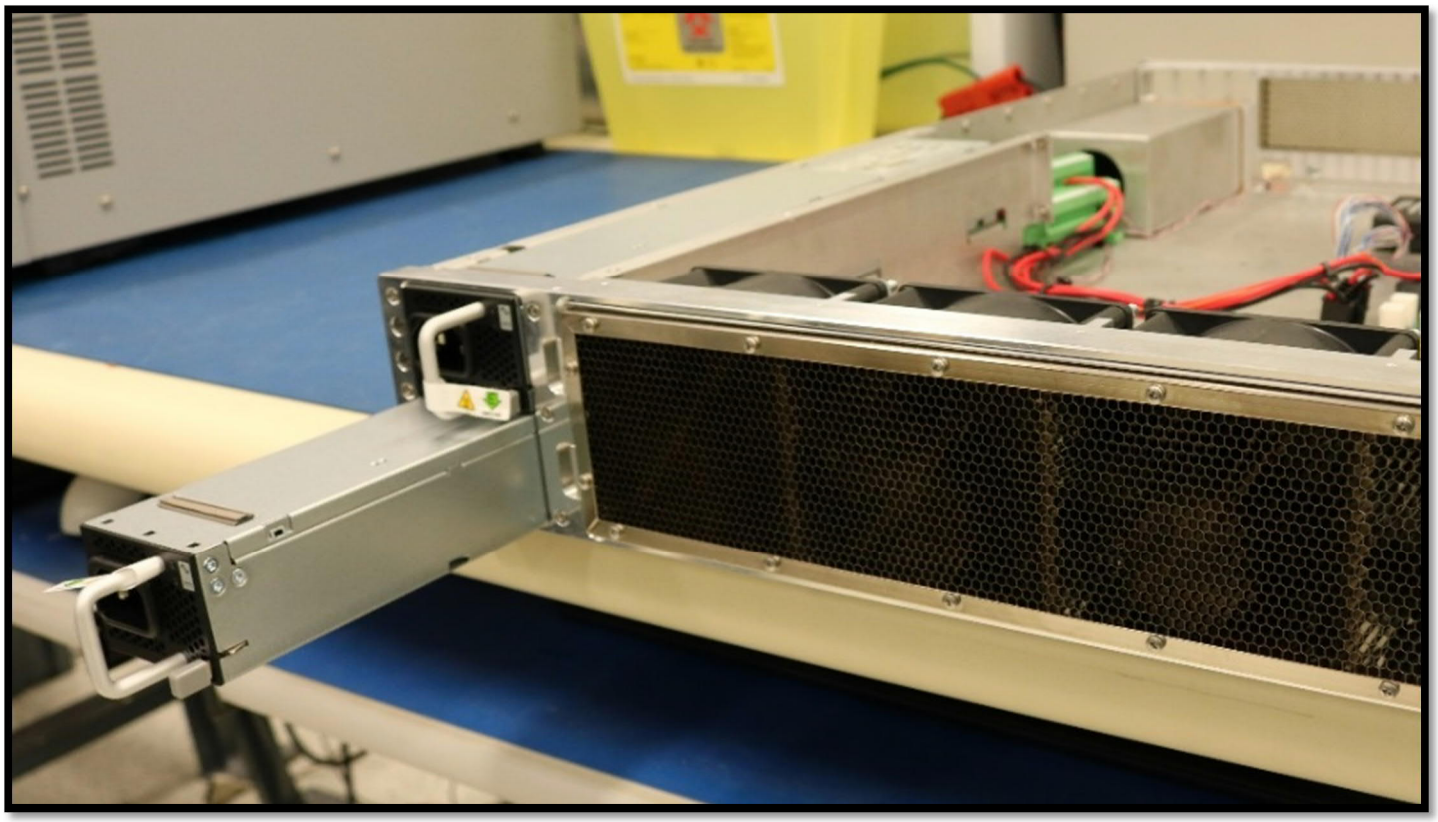

Figure 7-15 Rear panel of the TALON LRU showing redundant hot-swap replaceable AC-to-DC mains supplies and fans.

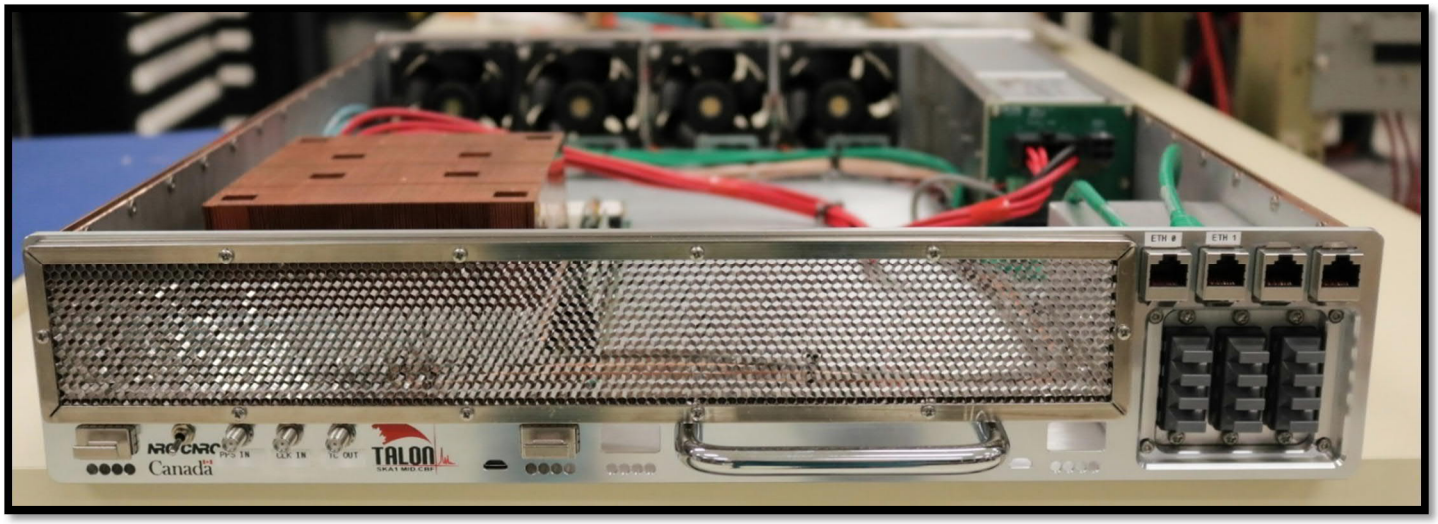

Figure 7-16 Front-panel view of the TALON LRU showing MTP bulkheads, QSFP28 cages with plugs, RJ-45 connectors for 1 GbE into the FPGAs' HPS, and coaxial connectors for clock and timing I/O.

The TALON LRU fits in a standard COTS 19" server rack but, due to width requirements, uses pre-installed "shelf rails" rather than conventional sliding rails for mounting. Also, to facilitate fiber cable routing up the front right and left of the server rack, the LRU is not outfitted with the usual 19" rack-mount mounting "ears", but rather a pull handle (shown in Figure 7-16) and with hand-actuated mechanical fastening "toggles" at the rear panel.

A top-view of the TALON LRU of the notional size and placement of the "Optical Converter" modules for accessing ALMA antenna data (according to Figure 7-6) is shown in Figure 7-17.

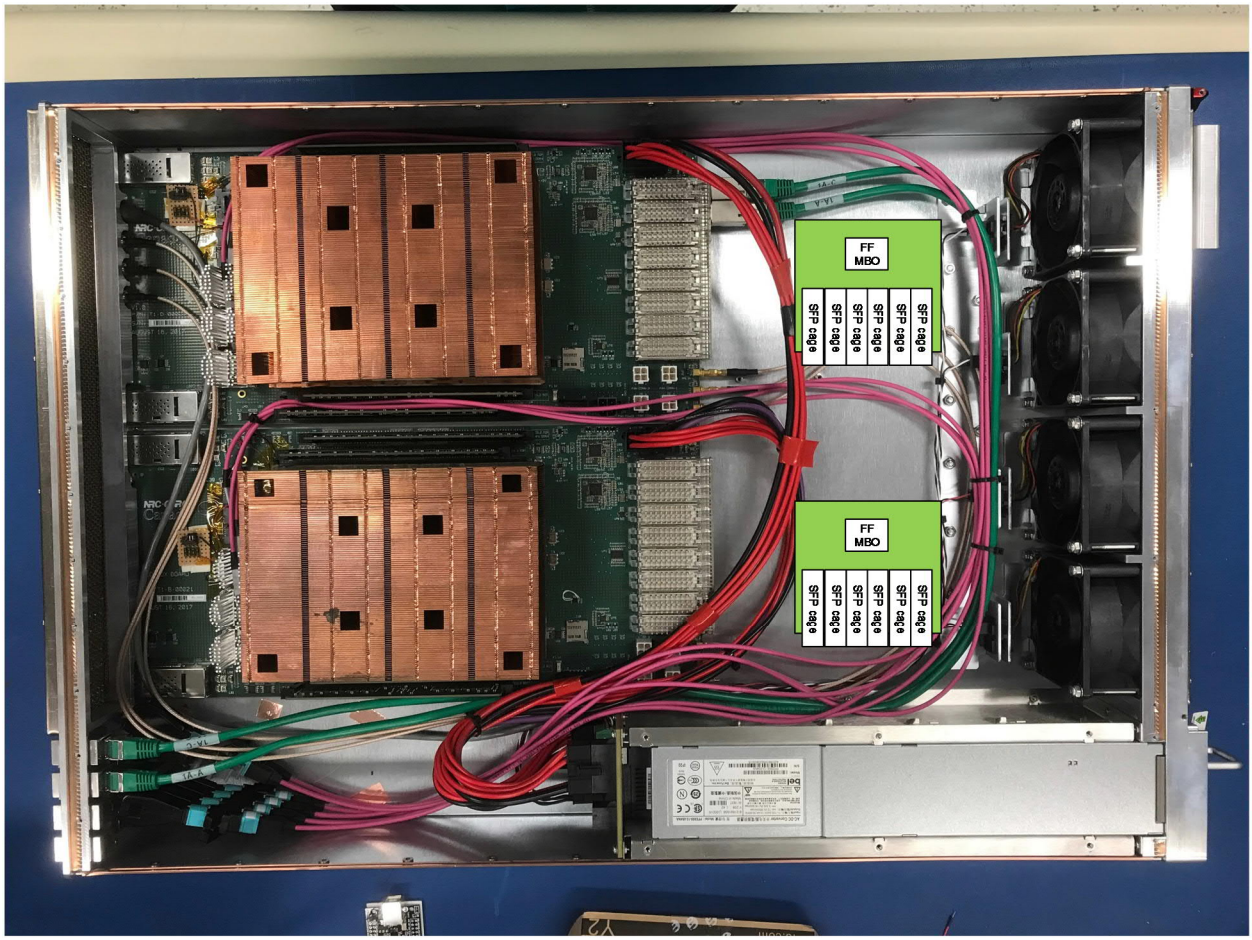

Figure 7-17 Notional placement of the Optical Converter Modules in each TALON LRU in the VCC-Part. Each converts 12 x 10.0 Gbps single-mode λ=1.5 µm coming from an ALMA antenna to 12 x 10.0 Gbps multi-mode for entry into a TALON-DX FCI LEAP MBO. Six SFP(+) cages are shown for each, but there are actually 12, with the other 6 mounted on the rear side.

7.3 FPGA designs

There are three complete FPGA designs required for AT.CBF: one for the VCC, one for the Imaging Correlation AFSP, and one for the VLBI Beamforming AFSP. Block diagrams of these designs are shown in Figure 7-18 to Figure 7-20. The ALMA 2030 VCC design is of course different, depending on technology and bandwidth. However, the AFSP designs and installed hardware are the same unless a technology update occurs.

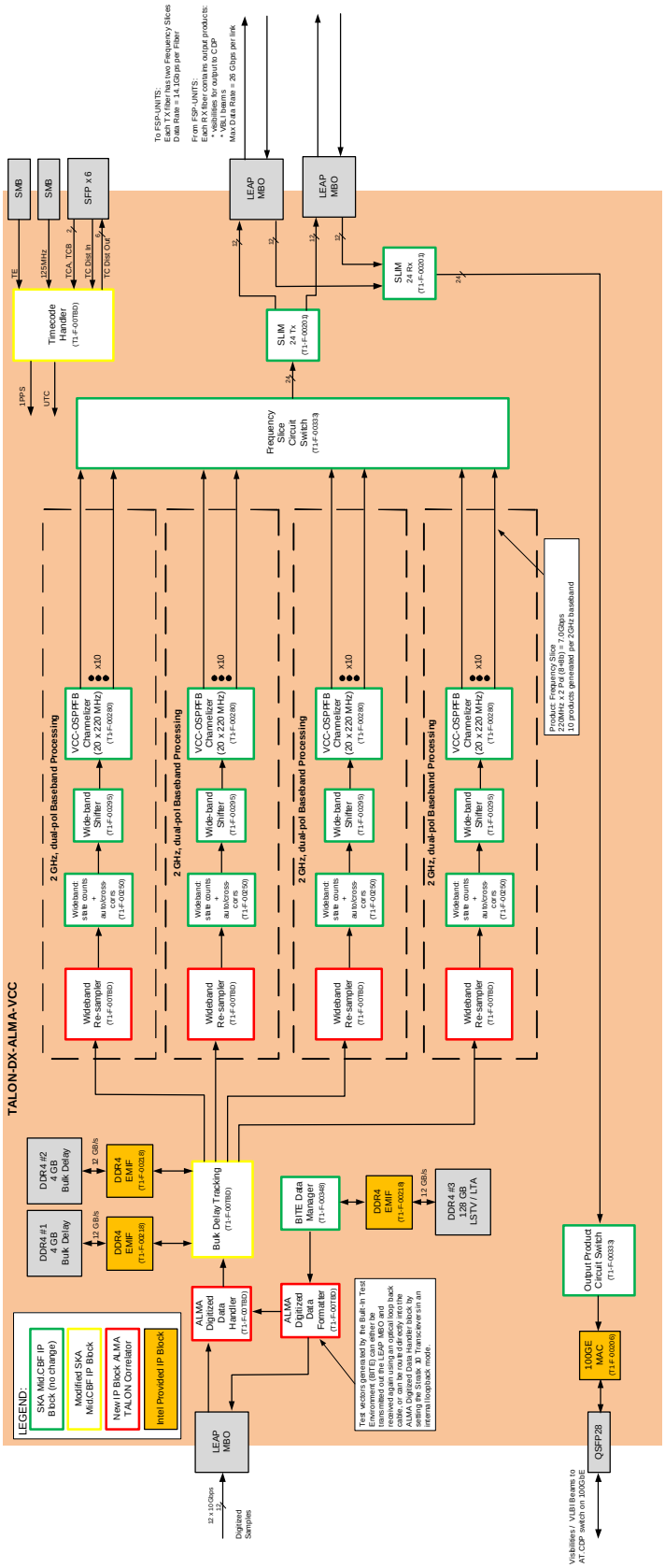

Figure 7-18 AT.CBF VCC FPGA block diagram for existing bandwidth BLC replacement.

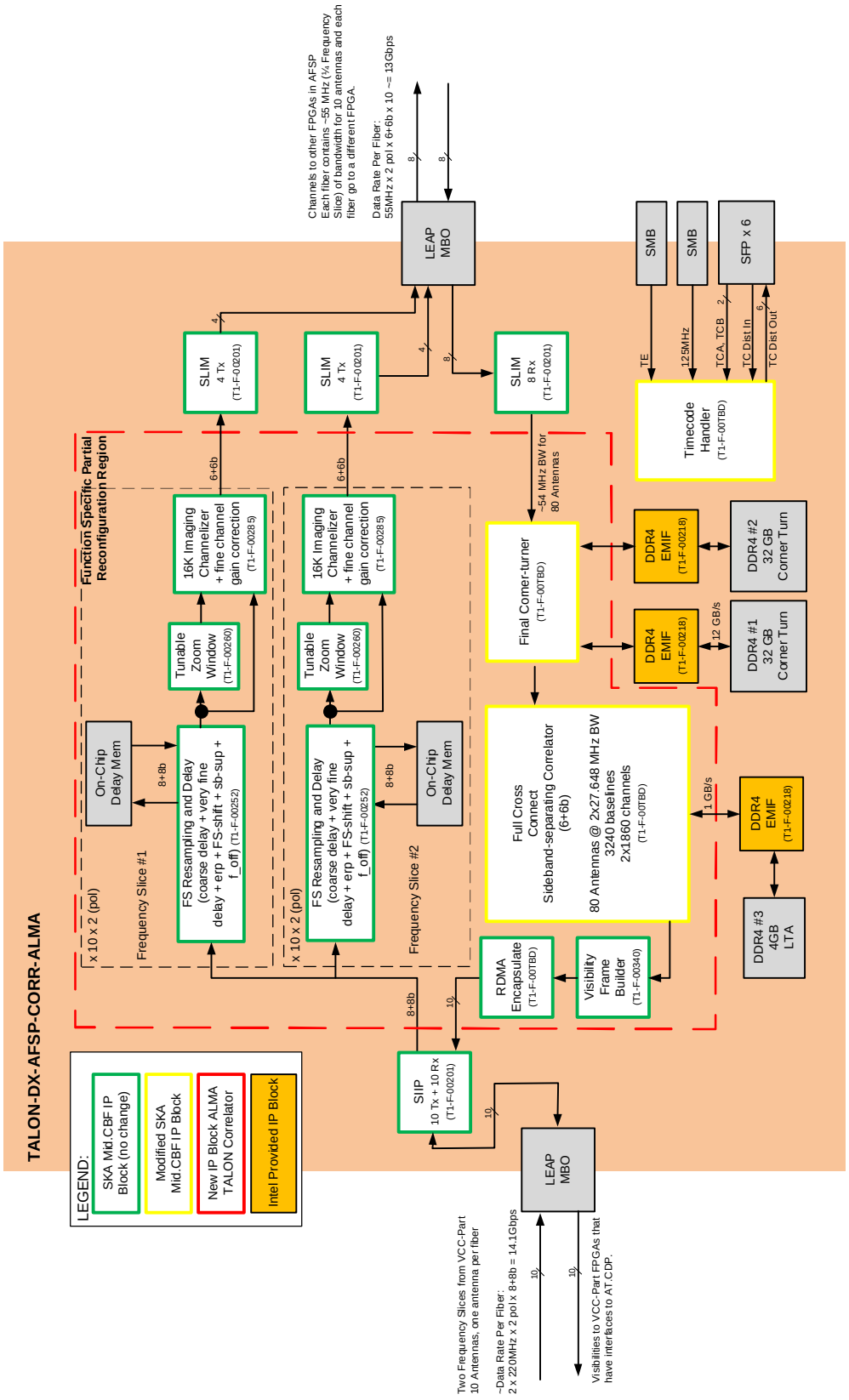

Figure 7-19 Imaging Correlation AFSP FPGA block diagram.

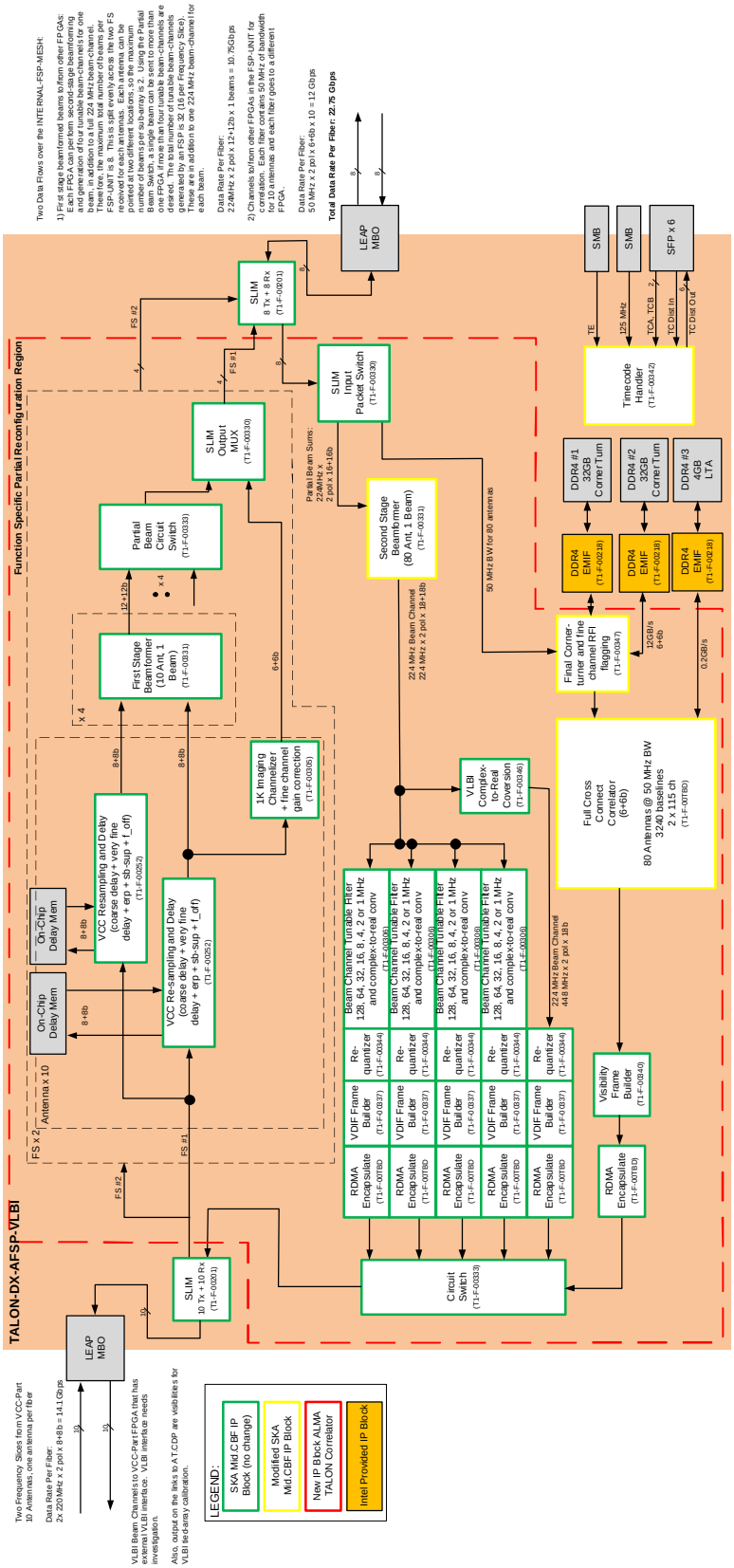

Figure 7-20 VLBI Beamforming AFSP FPGA design.

Critical FPGA resource utilization estimates and external DDR4 memory bandwidth requirements for the 3 FPGA designs are summarized in the following table:

Table 7-1 AT.CBF FPGA critical resource utilization estimates.

FPGA Design	% Multipliers	% M20K RAM	% DDR4 Bank 1 BW	% DDR4 Bank 2 BW	% DDR4 Bank 2 BW
AT.CBF VCC	39	66	50	50	50
AFSP Imaging Correlation	66	86	50	50	6
AFSP VLBI Beamforming	79	45	50	50	6

As well, it must be noted that all FPGA designs' clock speeds are 450 MHz or less, a reasonably comfortable regime for this 14 nm FinFET technology node, to ensure FPGA "timing closure" can be achieved.

AT.CBF contains a large number of high-speed serial (SERDES) fiber connections between FPGAs in the same TALON LRU, in the same rack, and across different racks, and all through passive fiber mesh circuits. Many of these connections are of different lengths and on system start up each point-to-point serial connection must be configured[42] for transmitter strength and receiver gain and equalization to ensure a reliable connection. This means that each FPGA SERDES channel must be set accordingly and, once set, not interrupted so that the system is stable. An efficient custom code Serial Line Interface Module (SLIM) shown in all of these figures provides the FPGA fabric-to-SERDES IP block interface, complete with frame alignment, identification, and error checking.

Since there is only one VCC FPGA design required, its FPGA bitstream does not need to be dynamically changed and so its FPGA SERDES channels' configurations are static. However, the AFSP FPGA bitstream needs to be changed every time the AFSP's Function Mode is changed from Imaging Correlation to VLBI Beamforming, and vice-versa. To ensure this happens quickly and to avoid unnecessary error generation and re-configuration delay, the AFSP FPGAs are "partially re-configured", i.e. changing the core of the design for the new AFSP Function Mode whilst leaving the periphery unchanged. The Intel Stratix-10 FPGAs are capable of doing this and Figure 7-21 shows how the external I/Os are left unchanged, whilst the internal Function Mode specific "partial reconfiguration region" is changed accordingly.

[42] On initial system startup these settings are "discovered" through an iterative process. After that, they are saved and subsequently recalled and applied, fixing/modifying any complaining connections accordingly.

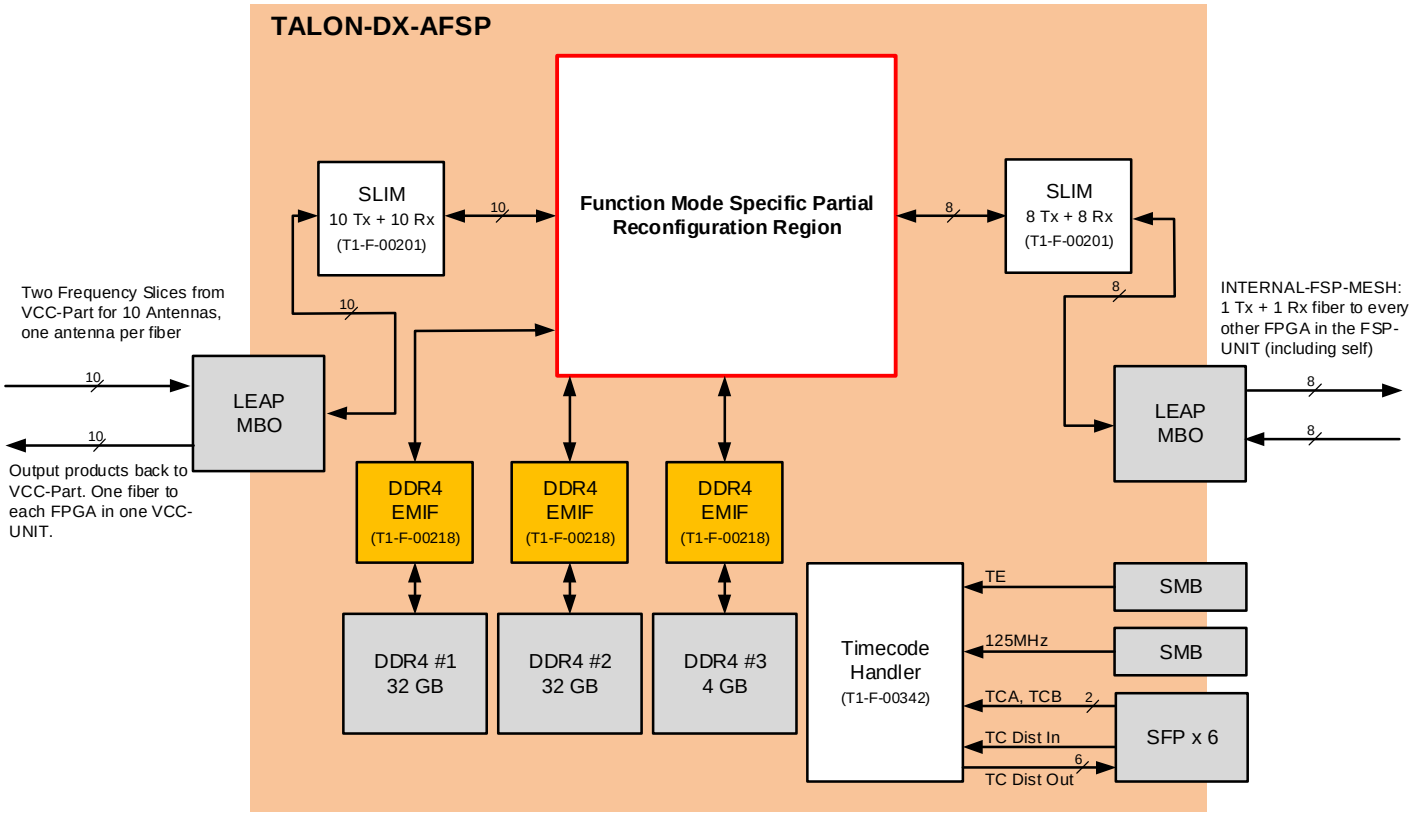

Figure 7-21 AFSP FPGA partial reconfiguration block diagram.

8 Monitor and Control

As discussed in section 4.3, AT.CBF M&C (Monitor and Control) is largely copied from the SKA1 Mid.CBF design, with capabilities not required by AT.CBF pruned out. The entire AT.CBF M&C infrastructure is built on TANGO [6] messaging and devices, copying as much as possible from SKA1 Mid.CBF, with details in [7].

Figure 4-7 shows the Command and Control "Primary Presentation" of the SKA1 Mid.CBF system. Other views, extracted from [7] are shown in the figures below. AT.CBF views will be the same with aspects of Mid.CBF not applicable to ALMA pruned out and specific aspects of AT.CBF included and adapted as needed. Recall from section 4.3 that the bubble "CSP.LMC" in all views, for ALMA, is the ALMA online executor/controller; the utility of CSP.LMC for SKA1 is a bridge between TM (Telescope Manager, the SKA1 online executor/controller) and Mid.CBF, Mid.PSS (pulsar searching), and Mid.PST (pulsar timing.)

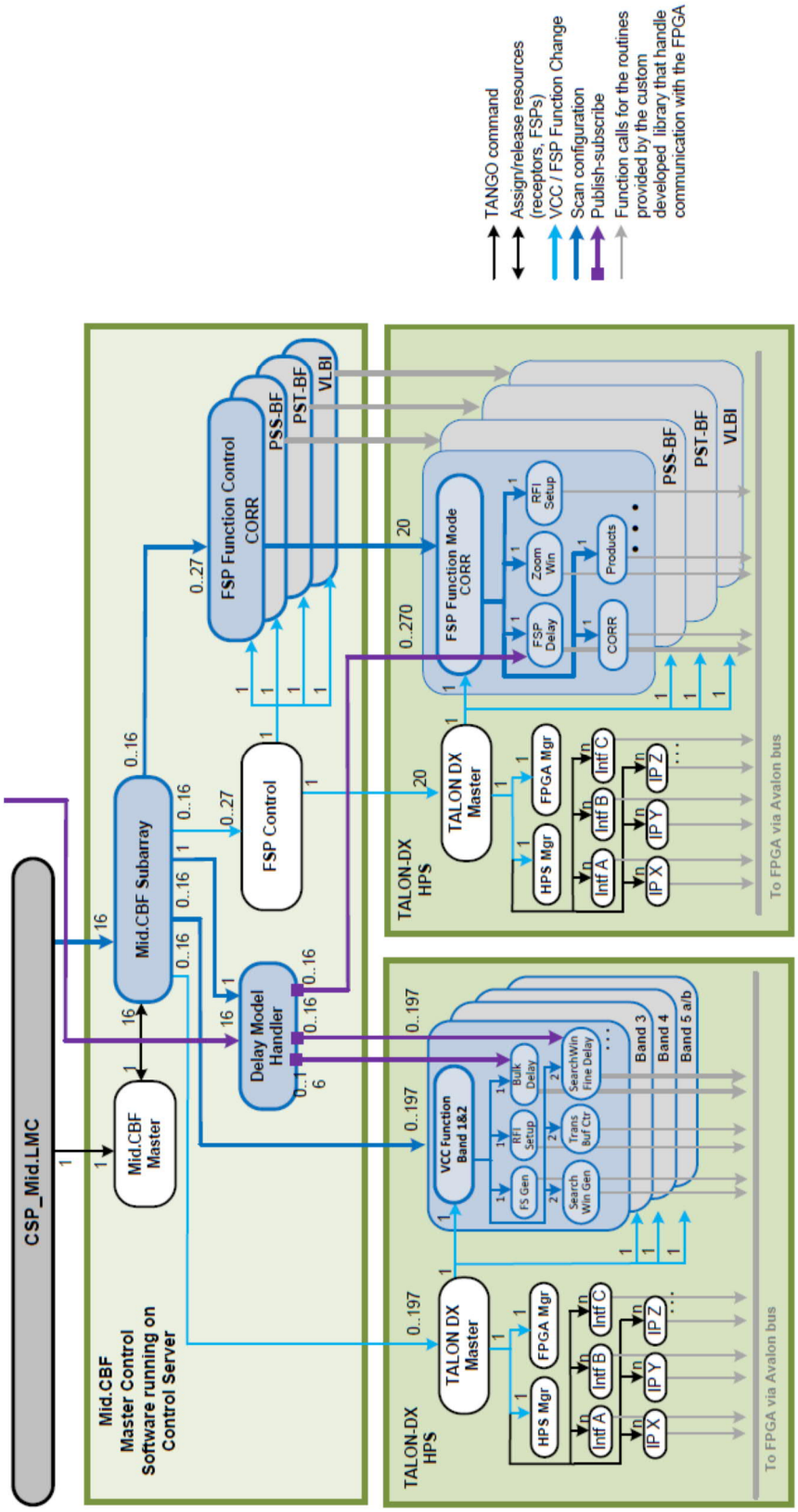

Figure 8-1 SKA1 Mid.CBF Sub-array Configuration and Control view Primary Presentation.

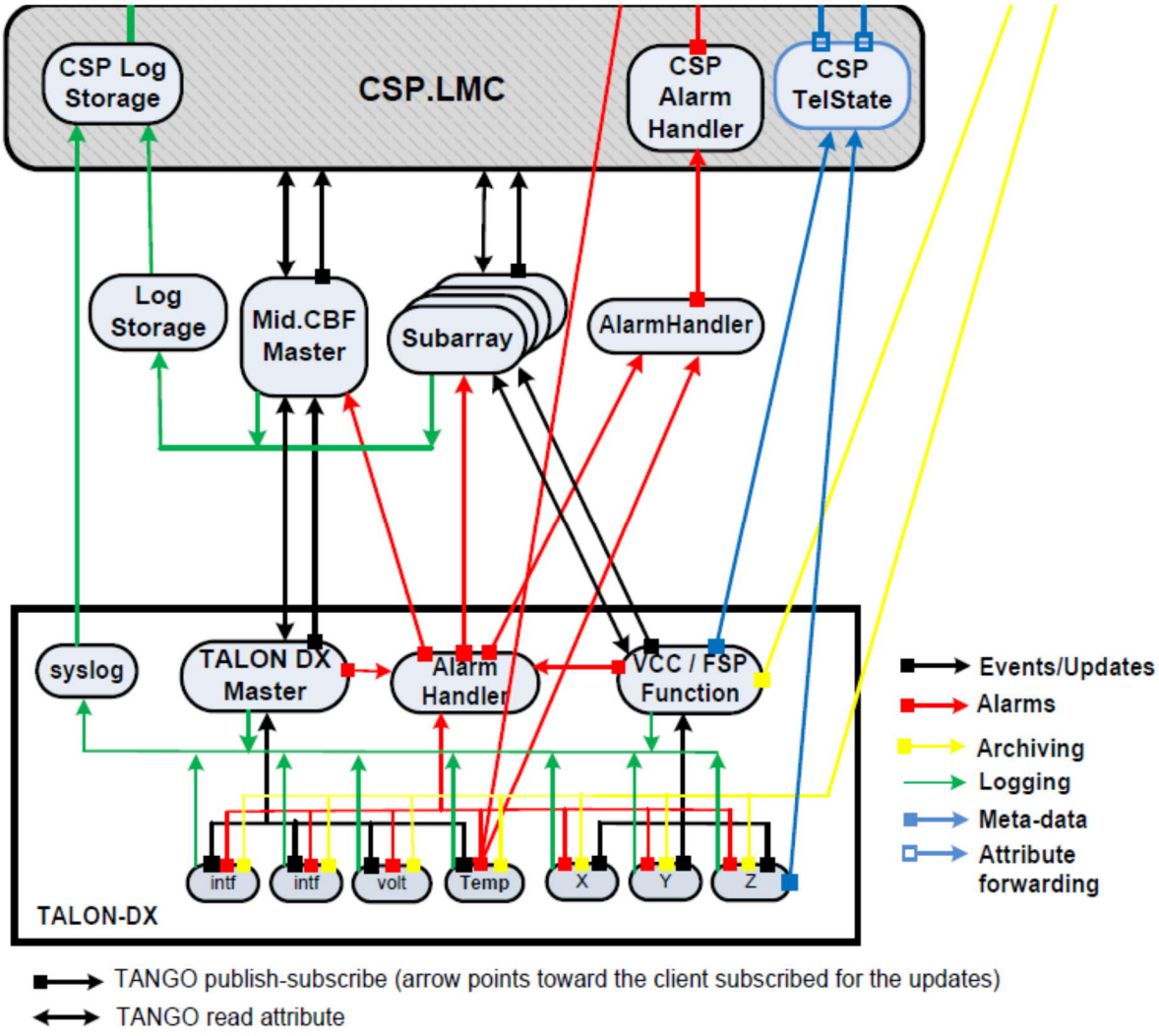

Figure 8-2 SKA1 Mid.CBF Monitoring, Archiving, and Logging Primary Presentation.

As mentioned in section 4.3, configuration of a sub-array in AT.CBF occurs when a JSON configuration file is provided to AT.CBF Master by the ALMA online executor, having been previously generated by an off-line observation preparation/configuration tool specifically built for AT.CBF capability.

An example SKA1 Mid.CBF JSON file, not including sub-array antenna selection (which is done separately and in advance, although such could be included in the JSON file at the same time), is shown below:

```
{
    "id": "Test1",
    "frequencyBand": "1",
    "delayModelSubscriptionPoint": "host1/csp_subarray_01/delayModel",
    "rfiFlaggingMask": {},
    "fsp": [   // configuration for FSP that correlates the full FS bandwidth
        {
            "fspID": 1,
            "functionMode": "CORR",
            "frequencySliceID": 1,
```

```
            "corrBandwidth": 0,                 //  bandwidth to be correlated
calculated as FSBW / 2⁰
            "integrationTime": 140,          //  msec
            "fspChannelOffset": 14880,   // used to calculate ChannelID to be inserted
in the output data
            "channelAveragingMap": [     // averaging in frequency per group of 744
channels
                [0, 8],
                [744, 8],
                [1488, 8],
                [2232, 8],
                [2976, 8],
                [3720, 8],
                [4464, 8],
                [5208, 8],
                [5952, 8],
                [6696, 8],
                [7440, 8],
                [8184, 8],
                [8928, 8],
                [9672, 8],
                [10416, 8],
                [11160, 8],
                [11904, 8],
                [12648, 8],
                [13392, 8],
                [14136, 8]
            ],
            "outputLinkMap": [     //  output links
                [0, 4],
                [744, 8],
                [1488, 12],
                [2232, 16],
                [2976, 20],
                [3720, 24],
                [4464, 28],
                [5206, 32],
                [5952, 36],
                [6696, 40],
                [7440, 44],
                [8184, 48],
                [8928, 52],
                [9672, 56],
                [10416, 60],
                [11160, 64],
                [11904, 68],
                [12648, 72],
                [13392, 76],
                [14136, 80]
            ],
            "outputHost": [[0, "192.168.0.1"]],  //destination for output products
            "outputPort": [[0, 9000, 1]]
        },
    "fsp": [   // example of FSP configuration for zoom window correlation
        {
            "fspID": 4,
            "functionMode": "CORR",
            "frequencySliceID": 2,
```

```
            "corrBandwidth": 2,   // bandwidth to be correlated calculated as FSBW /
2²
            "zoomWindowTuning": 4700000,  // window center frequency
            "integrationTime": 140,
            "fspChannelOffset": 29760,
            "channelAveragingMap": [
                [0, 8],
                [744, 8],
                [1488, 8],
                [2232, 8],
                [2976, 8],
                [3720, 8],
                [4464, 8],
                [5208, 8],
                [5952, 8],
                [6696, 8],
                [7440, 8],
                [8184, 8],
                [8928, 8],
                [9672, 8],
                [10416, 8],
                [11160, 8],
                [11904, 8],
                [12648, 8],
                [13392, 8],
                [14136, 8]
            ],
            "outputLinkMap": [
                [0, 1],
                [744, 5],
                [1488, 9],
                [2232, 13],
                [2976, 17],
                [3720, 21],
                [4464, 25],
                [5206, 29],
                [5952, 33],
                [6696, 37],
                [7440, 41],
                [8184, 45],
                [8928, 49],
                [9672, 53],
                [10416, 57],
                [11160, 61],
                [11904, 65],
                [12648, 69],
                [13392, 73],
                [14136, 77]
            ],
        }
    ]
```

The 744-channel "averaging group" is because in Mid.CBF each FSP contains 20 FPGAs (14880/20=744 channels) and there can be a different channel averaging factor in each one. For AT.CBF, there are notionally 8 FPGAs in an AFSP, so the group size is 14880/8=1860, as described in detail in section 6.1.2.

The "output link map" parameters tell Mid.CBF which of 80 100G output links (to the SDP) are to be used for streaming visibilities, allowing for TM to load-balance traffic across links.

AT.CBF Master, when presented with a JSON file, will check to ensure that its configuration doesn't use AT.CBF resources that are already in use[43], and reject it if it does. To avoid this, an ALMA observation scheduler will naturally want to perform this function in advance.

A key aspect of Mid.CBF and therefore AT.CBF Imaging Correlation configuration is that AT.CBF is told the center frequency of the Frequency Slice, which to correlate in which AFSP, and channel averaging factors etc., but not the actual spectral channel center frequencies. These are determined internally, taking into account the various frequency shifts that occur (including that required to align spectral channels across Frequency Slices—see Figure 6-3), and then fed as values to be used by AT.CDP[44] to label the output visibilities appropriately.

Finally, SKA1 Mid.CBF is provided with delay-tracking polynomials, valid for up to 10 seconds, from an external CALC[45] server (see Figure 8-1 "Delay Model Handler" input path.) For AT.CBF, a similar approach is envisioned, replacing the existing ALMA/BLC approach of higher-cadence, lower-order models being produced and applied directly. Internally, AT.CBF then takes these high-order polynomials and, every 10 msec, performs a least-squares point-slope fit, whose coefficients then drive TALON FPGA hardware delay synthesizers, providing precise, continuous, and deterministic delay tracking.

[43] Primarily AFSP Function Modes; if enough AFSPs are instantiated so that Function Mode changes are unnecessary, then most conflict is removed, only antenna sub-array allocation contention being possible.
[44] In SKA1 Mid, these values are fed to TM (Telescope Manager), which then informs SDP (Science Data Processor).
[45] NASA/GSFC-maintained program used by many radio telescopes around the world.

9 Test and Verification

Functional test and verification of AT.CBF of course closely mirrors that of SKA1 Mid.CBF [15]. Generally this means that, at each level, from firmware IP block up to the full system, I&T (Integration and Test) occurs followed by formal verification through execution of a set of test cases and analysis of results. The specification of each item—at whatever level—that is to undergo verification includes development of a Verification Test Plan (VTP), execution of it, and with results captured in a Verification Test Report (VTR.) By using this rigorous approach, a more robust and thoroughly tested system is the outcome with the goal of minimizing on-site testing and ALMA telescope down time as AT.CBF is brought online.

At the TALON LRU and AT.CBF system level, a key feature of Mid.CBF (and that will be adapted for AT.CBF) is the Built-In Test Environment (BITE.) A block diagram of BITE, extracted from [15] is shown in Figure 9-1 below:

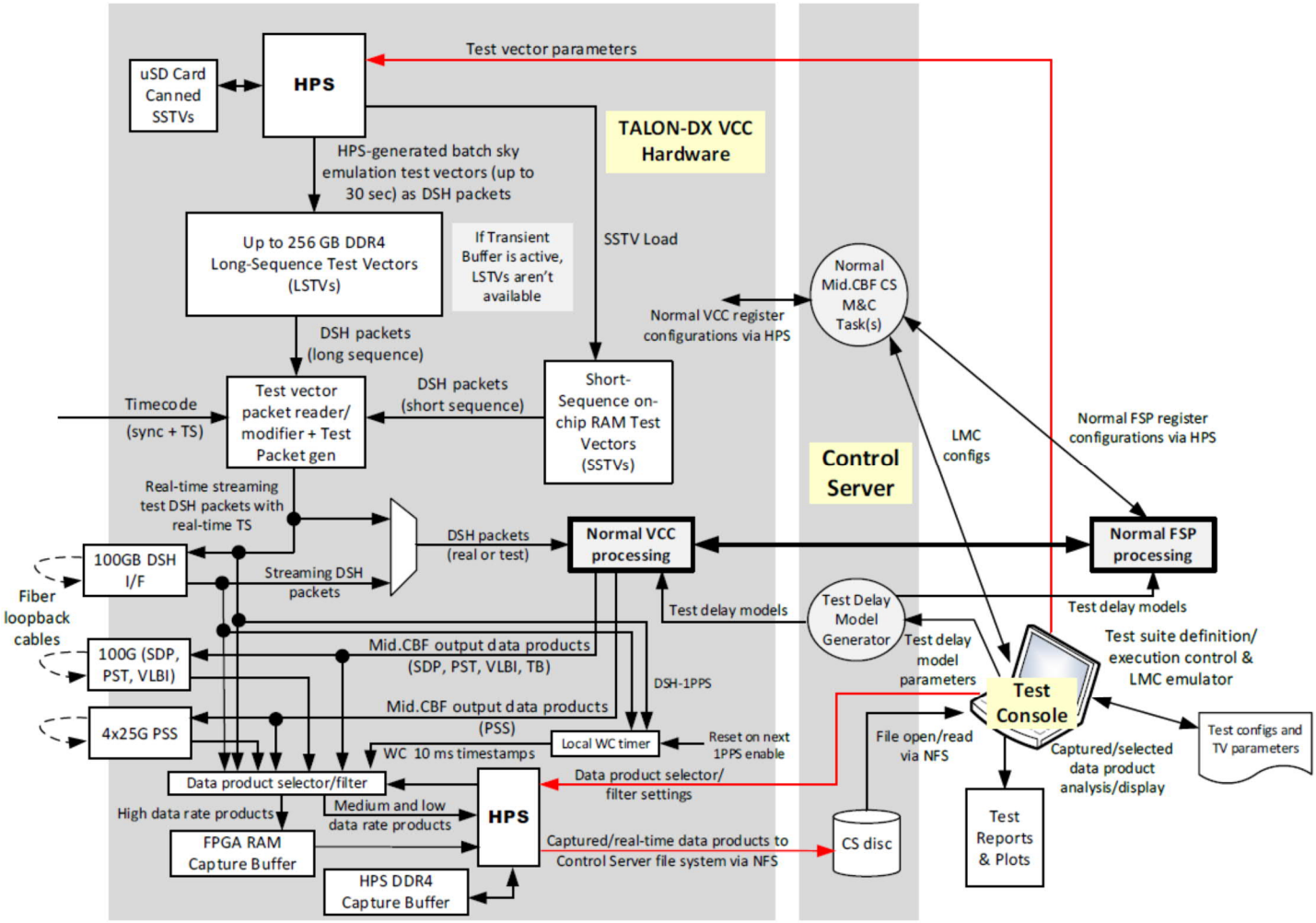

Figure 9-1 SKA1 Mid.CBF BITE block diagram.

Key aspects of BITE are as follows:

- Two kinds of test vectors may be generated. Short Sequence Test Vectors (SSTVs) are generated in digital hardware and thus continuously stream through the entire signal chain. Processing these won't result in cross-correlated fringes, but they are sufficient for stimulating the signal chain to assess/set levels, gather statistics, acquire autocorrelation spectra, and detect noise-limited artefacts since they can be very long and essentially never repeat[46]. Long Sequence Test Vectors (LSTVs) are finite duration (up to ~30 sec) offline computer-generated test vectors that simulate point sources, on or off boresight, and allow for full performance evaluation[47] of the signal chain. With these, cross-correlation fringes are obtained and coherent beams can be produced.
- Capture of correlated visibilities and VLBI beamformed data for offline analysis (by the Test Console shown, or other computer(s).)
- Can be operated with or without loopback cables on the 100G I/O ports.

With BITE it is possible to fully functionally test each FPGA design starting at the TALON LRU level all the way up to the system level before, during, and after deployment to the ALMA site, including after commissioning. BITE is built into the entire fabric of the Mid.CBF and therefore AT.CBF design.

For non-functional verification (e.g. safety, EMC), the approach is to use already certified COTS equipment wherever possible and, within the TALON LRU, use COTS items where certification of custom items would be labour and cost intensive. One example is that the TALON LRU uses COTS AC-to-12VDC pluggable power supplies, as shown in Figure 7-15, eliminating the need for explicit electrical safety certification. For rack installation and electrical wiring, COTS items are used, requiring a certified electrician during installation to ensure all wiring is according to code. For SKA1 Mid.CBF, at least FCC/CISPER Class A radiated and conducted EMI emissions levels must be met and the TALON LRU is designed and tested accordingly. Although this is likely not strictly required for ALMA, meeting this spec means that there likely won't be an EMC problem between TALON LRUs and other COTS equipment.

[46] E.g. using multiple 64-bit LFSR digital circuits, at 450 MHz, yields sequences that repeat only every ~1300 years. The name "Short Sequence" is therefore something of a misnomer since at the time of BITE conception this kind of time duration wasn't considered.

[47] Except for of course long integrations, needed where one wants to determine if there are spurious products that appear above the noise floor, whilst obtaining a low-level correlated result.

10 Development Plan

As of this writing, the SKA1 project has completed the pre-construction design and development phase, and is transitioning to full construction. What this means for Mid.CBF is that a design has been developed, TALON LRU prototypes have been built and tested, firmware has either been developed or its resources and development costs have been estimated, total system costs have been generated, and all has been expertly externally reviewed[48]. In short, SKA1 pre-construction for Mid.CBF has been a ~60 person-year design and de-risking effort, with much detailed design and testing remaining to be done during construction remaining. Thus, Mid.CBF construction is "build to spec" rather than "build to print", although critical Mid.CBF "prints" have been developed and tested.

The development plan for AT.CBF largely parallels that of Mid.CBF, but enthusiastically inviting NRAO and ALMA office personnel to engage in all aspects of AT.CBF-specific development primarily in software and testing, but also project management & system engineering, FPGA firmware development and testing, AT.CBF system design, and AT.CBF system testing. As mentioned, the offline observation preparation/configuration tool that generates AT.CBF JSON configuration files will need to be developed as well, which we understand will be a European ALMA responsibility (ref: discussions with Brogan.)

Key aspects of SKA1 Mid.CBF, and therefore AT.CBF construction, are as follows:

- Development and delivery will be via a government and industry collaboration. MDA corporation (www.mdacorporation.com) was contracted for SKA1 Mid.CBF pre-construction but for construction, selection of an industry contractor will be via a competitive process.
- Key NRC personnel (see section 16) will be actively intellectually involved in development including reviewing design artefacts, participating in design reviews, reviewing test plans and results etc. and providing expert design when needed.
- NRC retains and owns all contractor-developed IP and design sources/artefacts, including FPGA firmware, software, test plans, test results, documentation etc. All such IP and documentation is included with AT.CBF delivery.
- TALON LRU production is full turn-key production by a North American "contract manufacturer", with fully assembled, loaded, and tested units delivered to development sites in North America as well as the ALMA site itself. It is most efficient if a single contract manufacturer is used for both Mid.CBF and AT.CBF TALON LRUs, but if there is some programmatic reason why AT.CBF TALON LRUs must be manufactured in the U.S., such can be arranged but likely with additional contract manufacturer tooling costs, including full assembly and functional test. It is not essential that all Mid.CBF and AT.CBF TALON hardware be built at exactly the same time, but within at least a 1 year timeframe is likely prudent to take advantage of volume component purchasing price reductions and to avoid storage and "shelf-life[49]" costs.
- A representative subset of the entire system is built offsite (at one or more development locations) with the full AT.CBF system only put together in stages at the final ALMA site (see section 11.) The representative subset is initially and at minimum, one or a few TALON LRUs for

[48] Including and especially Larry D'Addario, one of the most critical expert reviewers available!
[49] i.e. of both components and processes.

early development and testing, fleshing out to at least one VCC-UNIT and one AFSP-UNIT for final offsite testing (both of which can fit in one 19" rack.) This is because in order to test the full functionality of the VCC and AFSP, only one VCC-UNIT (Figure 7-5) and one AFSP-UNIT (Figure 7-7) are needed. Even though a VCC-UNIT includes only 10-antenna processing capability and therefore the AFSP can only correlate 10 antennas, the other 70 inputs can be populated with copies of the same or different Frequency Slice(s) out of the VCC-MESH, but labelled as coming from different antennas. Thus, both the VCC-UNIT and AFSP-UNIT are operating in a context that is essentially identical to a full system, with simulated antenna data provided by the BITE.

NRC and an industry contractor are currently working on the TALON Demonstration Correlator (TDC), a system that contains all Mid.CBF signal processing blocks, but scaled down to optimally use just a few TALON LRUs to correlate up to 16 antennas and 800 MHz (4 Frequency Slices) of bandwidth. The TDC will be used during initial Mid.CBF deployment in South Africa and a copy of it is also to be used as a correlator for a local NRC-Penticton site telescope update project.

11 Deployment Plan

11.1 Existing bandwidth AT.CBF

Once all offsite development and testing is complete using at least one VCC-UNIT and one AFSP-UNIT as described above, deployment to site is the next step[50]. Deployment to site notionally occurs as follows:

- Deploy a single-rack system, referred to here as "AT.CBF-10A", including one VCC-UNIT, at least one AFSP-UNIT, and support computers and network switches including AT.CBF Master, an AT.CDP switch, and a scaled-down AT.CDP to the ALMA site. Perform testing using BITE to verify that this system is working according to specifications before connecting to ALMA antennas. This includes performing the same formal verification that was done on the same system off-site, to verify it is functioning correctly after delivery and installation.
- Connect up to 10 ALMA antennas to AT.CBF-10A and perform correlation/beamforming testing as well as science data reduction and imaging. Ensure that there are no anomalies or bugs before moving onto the next stage. Although it is desirable to have AT.CBF-10A operate concurrently with the BLC (i.e. both correlating the same antennas at the same time) so output data can be directly compared, such is likely difficult to arrange in practise. Thus, observing time on up to 10 antennas (4 minimum) will need to be arranged to adequately test AT.CBF-10A in a reasonable timeframe. Also, switching antennas between AT.CBF-10A and the BLC may be done manually via patching, with fiber-optic splitters, or by using the Optical Converter (see Figure 7-6) SFP+ 10G output to repeat the antenna data for input to the BLC[51]. For this testing, the ALMA online controller/executor might be used directly, or likely a simulator is used instead to not be invasive to ALMA operations. The infrastructure of the ALMA HIL (Hardware In the Loop) project now in progress can likely be used/shared for this phase of testing (https://osf.io/962yj/).
- If, in the previous step, less than 10 antennas have been used, and/or only a small amount of bandwidth has been processed, the next step is full 10-antenna science testing with sufficient bandwidth for full AT.CBF evaluation, since the next step is full switchover of ALMA to use the AT.CBF. This system is referred to here as AT.CBF-10B. This may mean deploying the entire AT.CBF system to site, particularly if it is located at the OSF and therefore doesn't collide with the BLC and ALMA operations. For this testing, a full AT.CBF-capable ALMA online controller/executor is used as well as the observation preparation tool to generate observing configurations, AT.CBF data flow to the AT.CDP and on to the Archive and science processing, as well as VLBI beamforming and verification in a (external) VLBI correlator with other mm-wave VLBI antennas.
- The next step is full deployment and switchover of all ALMA operations to the full AT.CBF. If all previous steps have been rigorously tested, this should be quite quick[52] (i.e. a few weeks.)

[50] With, of course, significant pre-site-deployment site and logistics preparation, not described here.
[51] This latter option possibly only if the AT.CBF is located in the correlator room at the high-site.
[52] However, experience with the VLA and full switchover to the WIDAR correlator is a cautionary counter example, since anomalies were found with WIDAR and surrounding systems not detected in the 10-antenna system, which took some time to resolve.

11.2 AT.CBF upgrade and deployment for ALMA 2030

For ALMA 2030 antenna technology deployment to the installed AT.CBF as well as AT.CBF 2030 upgrades to handle increased bandwidth, the following points are of note:

- Likely additional hardware needed for increased bandwidth will use new technology[53] for cost and power savings. If this new technology uses different/upgraded electrical and serial fiber optic methods (e.g. PAM4 56G), then all existing AT.CBF hardware will need to be replaced. However if NRZ 25G serial methods and optics, compatible with the existing installed AT.CBF system using TALON LRUs as described in section 7.2 are used, then the existing (24, up to 44[54]) AFSPs may be left in place. There is believed to be no savings or utility in using faster serial rates and optics for AT.CBF than NRZ 25G.

- New AT.CBF VCCs, compatible with new ALMA 2030 digitizers and bandwidth, will need to be developed. Likely this will use new TALON technology for processing, although it is possible to use TALON LRUs, depending on interface requirements. If the latter is employed then an entire TALON LRU is required for each antenna, with each TALON-DX FPGA processing ½ of the total bandwidth. In this case it naturally leads to a "bank" approach, where there are 2 banks in AT.CBF-2030, each bank processing 8 GHz/pol. If the former (i.e. new technology) is used, all 16 GHz/pol may likely be implemented in a single FPGA and if the FPGA has more serial channels, then the same architecture as AT.CBF results (i.e. 2X more output Frequency Slices to handle 2X the bandwidth, but any AFSP may process any 2 Frequency Slices.)

As far as the transition of ALMA antennas to ALMA 2030 antennas, the AT.CBF FSA physical and signal processing architecture is ideally suited to facilitate continuing and virtually uninterrupted ALMA operations over the few years that it will take for this transition. For the following logistics discussion, assume that:

a) New hardware is used in the VCCs where one FPGA can process the entire 2X bandwidth,
b) the same VCC-to-AFSP NRZ 25G serial fiber optic signaling is used as the installed AT.CBF,
c) Frequency Slice bandwidth and sample rates stay the same,
d) 48 AFSPs (i.e. 2X) are sufficient for 2030 correlation and beamforming, although 80[55] is possible and,
e) the number ALMA antennas upgraded to 2030 2X bandwidth, and merged into the active array at a given time (i.e. antenna upgrade granularity), is not matched to the VCC-UNIT size of 10 antennas. This means each new VCC-UNIT must be backwards compatible with original ALMA antennas.

Logistics for these assumed conditions are envisioned as follows:

- VCC hardware is replaced one VCC-UNIT at a time. New VCC-UNITs handle 2X the bandwidth of the original, but in the same form factor (i.e. 5 TALON-NEW LRUs and a "VCC-MESH-NEW"), and

[53] Unless, of course, the replacement AT.CBF is populated with all hardware required for ALMA 2030, which is a possibility if TALON Intel Stratix-10 FPGA technology is deemed acceptable for use in a ~2030 system.
[54] Up to 88 if a double existing ALMA bandwidth AT.CBF system was originally deployed.
[55] Also, a 2U form factor allows for up to 144 MTP outputs, easily handling 40 connections to VCC TALONs and 80 outputs to 80 AFSPs for full 2030 bandwidth concurrent Imaging Correlation and VLBI Beamforming, if desired.

each TALON-NEW FPGA can be programmed and has interfaces to handle data from either an ALMA-2030 antenna or from an old one. The VCC-MESH-NEW requires 40 x MTP-24 ports and 48 x MTP-12 ports, for a total of 88 ports. This exceeds the 72-port restriction of a 1U box ([7], Figure 21-2), and therefore it is prudent that the VCC-MESH for AT.CBF be a 2U form factor rather than 1U as in Figure 7-8 to facilitate this transition[56]. There will be a short period of time, likely an hour or so, to replace the VCC-UNIT TALONs and the VCC-MESH-NEW, so the affected rack will need to be powered-down during replacement.

- Another 24 (up to 40, see above) MTP-24 cables exit each VCC-UNIT's VCC-MESH-NEW to handle the new bandwidth. These can likely be installed and routed in overhead cable trays without interrupting power, however, it may be prudent to install these during the original AT.CBF installation so they are ready for use for ALMA 2030.
- The new VCC-UNIT's output will contain a mixture of original and new ALMA antenna data as will the entire AT.CBF system until all antennas are upgraded. However, wideband frequency shifting (see Figure 6-2) and Frequency Slice generation[57] means that from the AFSP's viewpoint, there is no difference. This allows all antennas to be cross-correlated at the bandwidth available for each baseline, with any sub-array consisting of a mixture of antennas. Existing bandwidth and new bandwidth is correlated in any and all AFSPs that are available.
- Likely in advance, but at any time, racks are added to house an additional 24 AFSPs to correlate and beamform more bandwidth. These can be built with the existing TALON LRU technology[58], or TALON-NEW LRUs, but in any case will have been thoroughly tested and have the same functionality and therefore can be brought online as required to correlate and beamform the increased bandwidth.
- The AT.CDP and AT.CDP Ethernet switch in front of it also needs to be upgraded to accept more 100G ports (or likely a mixture of 100G and 400G, the latter presumed from TALON-NEW LRUs), as well as double the visibility data flow volume. The plan of how to do this is not discussed here, but should be reasonably straightforward.

In the alternative scenario where a TALON-NEW FPGA still only processes 8 GHz/pol bandwidth but likely with a different fiber input group, data format, and data rate from the antenna, then the new AT.CBF will be comprised of two "banks" as mentioned above. The first bank is the existing installed system, and VCC-UNIT TALONs are upgraded as described above[59], with ALMA 2030 antennas' bandwidth split in two, one-half of which is fed into this bank. The 2nd bank is another 8 racks with TALON-NEWs in the VCC-UNITs and original or TALON-NEWs in the AFSP-UNITs.

[56] And allow for 80 AFSPs as mentioned.
[57] As well as, as previously mentioned, ALMA 2030 digitizer frequencies chosen for compatibility for this transition.
[58] If not procured at the original AT.CBF production time, there is of course a risk of component and process obsolescence.
[59] Or, left as is with a new Optical Converter module installed to handle the new antenna fiber group and format, and of course with the TALON FPGA programmed to deal with the new data as well.

12 Risks

12.1 Programmatic risks

Table 12-1 AT.CBF programmatic risks.

ID	Programmatic Risk	Impact	Probability	Mitigation
PR-1	SKA1 Mid.CBF funding isn't available or is not available on a timeline amenable with AT.CBF development, production, and deployment.	AT.CBF will cost more. See section 13.	30%	NRC plans to continue development in any case as there is a commitment for a TDC for the ARTTA-4 project, as discussed in section 2.
PR-2	Sufficient FPGA developers are not available for AT.CBF firmware development from NRC or the SKA1 Mid.CBF prime contractor.	AT.CBF development may take longer and cost more.	10%	Sub-contract firmware development, separately from the prime if needed. Also, rely on NRC and NRAO for AT.CBF-specific firmware development.
PR-3	ALMA AT.CBF decision and funding availability is not available in time for optimal meshing with SKA1 Mid.CBF development.	AT.CBF development and deployment will take longer and cost more.	30%	Coordinate ALMA decision and funding timelines with expected SKA1 Mid.CBF as much as possible.
PR-4	Formal ALMA correlator/ beamformer requirements available in January 2021 exceed those of AT.CBF proposed here.	AT.CBF development and deployment may take longer and may cost more.	20%	Provide feedback/input to ALMA correlator/ beamformer requirements definition.
PR-5	AT.CBF development costs are more than currently estimated.	AT.CBF will cost more.	20%	More funding will need to be made available.
PR-6	Loss of one or more key NRC or contractor personnel.	Development and deployment delay.	10%	Document designs thoroughly. NRC has a very low staff turnover and overlap in personnel skill sets on several fronts including system design and signal processing.

12.2 Technical risks

Table 12-2 AT.CBF technical risks.

ID	Technical Risk	Impact	Probability	Mitigation
TR-1	AT.CBF VCC processing does not fit into FPGA resources as estimated here.	More (2X) TALON LRU hardware required in the	5%	Process ½ the bandwidth in each TALON FPGA,

		VCCs, but otherwise there is no change to the system connectivity or signal processing design. More racks are required.		requiring 1 TALON LRU for each antenna.
TR-2	AT.CBF AFSP processing does not fit into 8 FPGAs as estimated here.	More TALON LRU hardware required in each AFSP, likely 1 more LRU (10 FPGAs), but otherwise the impact to the design is minimal (see p. 52 discussion.) More racks are required.	10%	Add another TALON LRU to each AFSP. Design correlator corner-turner, correlator, and beamformer accordingly.
TR-3	TALON-DX hardware fails to perform as current prototypes indicate (this is listed here since the TALON-DX hardware prototype/engineering models are not yet volume production-ready.)	Possible delay in schedule.	5%	TALON-DX re-design/re-spin.
TR-4	The ALMA RFI environment is or becomes significant.	More bits per sample are required. RFI detection and flagging is required.	10%	Carry 12+12b between the VCCs and the AFSPs rather than 8+8b (Figure 6-2, Figure 6-4, Figure 7-3.) This should be more than enough and does not impact the system design since ~21 Gbps serial data rate results, which is within the 25 Gbps maximum. So as not to increase the correlator size, accept that with 6+6b, some channels may saturate due to RFI.

				Re-instate the RFI flagging and detection in SKA1 Mid.CBF into the AT.CBF design.

13 Cost and Schedule

13.1 Cost

The estimated cost of a BLC-replacement (existing 8 GHz/pol bandwidth) AT.CBF—assuming that SKA1 Mid.CBF construction is approved—is according to Table 13-1, totaling ~$13.5M USD[60]. Labour costs use industry charge-out rates used in Mid.CBF construction cost estimations. This cost table does not include the AT.CDP (100G) switch, AT.CDP compute cluster, or AT.CDP software development. The hardware items are relatively low-cost COTS items, and the software effort for AT.CDP was not investigated but is not likely a major cost item.

Table 13-1 Existing bandwidth AT.CBF cost table, assuming that SKA1 Mid.CBF construction is approved.

WBS	Labour PDs															
	PM:Sr	PM:Int	Eng:Sr	Eng:Int	Eng:Jr	Sci:Sr	Sci:Int	Con	Admin				Non-Labour			
Category	€ 1,057	€ 881	€ 939	€ 851	€ 705	€ 998	€ 822	€ 881	€ 470	Total PDs	Labour PD%	Labour Cost	Cost	Travel Cost	Contingency	TOTAL COST (USD)
MGT	165	0	99	66	0	0	0	50	116	495	12.1%	€ 421,427	€ 0	€ 207,000	€ 62,843	$816,873
SE	0	0	18	183	0	0	0	0	0	202	4.9%	€ 173,232	€ 0	€ 174,800	€ 34,803	$452,396
PD	0	0	0	0	0	0	0	0	0	0	0.0%	€ 0	€ 0	€ 0	€ 0	$0
HW	0	0	0	0	0	0	0	0	0	0	0.0%	€ 0	€ 153,468	€ 0	€ 20,632	$205,734
FW	0	0	0	705	0	0	0	0	0	705	17.3%	€ 600,287	€ 360,000	€ 0	€ 189,680	$1,358,916
SW	0	0	0	1042	0	0	0	0	0	1042	25.5%	€ 886,636	€ 240,000	€ 0	€ 180,494	$1,544,635
SII	0	0	0	0	0	0	0	0	0	0	0.0%	€ 0	€ 30,793	€ 13,400	€ 6,027	$59,345
I&T	0	0	115	798	0	0	7	0	0	919	22.5%	€ 792,294	€ 0	€ 256,200	€ 244,080	$1,527,435
AT	0	0	55	202	0	0	0	0	0	257	6.3%	€ 223,263	€ 100,247	€ 64,400	€ 31,033	$495,065
S&I	0	0	0	147	0	0	0	0	73	220	5.4%	€ 159,280	€ 40,000	€ 26,800	€ 19,218	$289,869
PHW	0	0	0	0	0	0	0	0	55	55	1.3%	€ 25,850	€ 4,620,802	€ 36,800	€ 466,092	$6,085,217
WTY	8	0	14	152	0	0	0	2	12	189	4.6%	€ 159,433	€ 277,266	€ 38,970	€ 62,371	$635,801
	173	0	301	3294	0	0	8	52	256	4084	100.0%	€ 3,441,701	€ 5,822,576	€ 818,370	€ 1,317,274	$13,471,287
												$4,067,058	$6,880,538	$967,068	$1,556,623	USD

For a 2X existing bandwidth AT.CBF, the cost increases to ~$19.5M[61] USD and, if SKA1 Mid.CBF construction is not approved—and therefore all AT.CBF NRE needs to be charged to ALMA—the NRE cost for either increases by an estimated $4.4M USD.

13.2 Schedule

The AT.CBF construction schedule is still somewhat uncertain due to uncertainties in the start of Mid.CBF construction because of COVID-19 and because funding for it has not yet been secured, although current estimates place construction start in mid-2021. Nevertheless, what follows assumes that Mid.CBF construction starts on or before AT.CBF construction.

Based on the latest call for ALMA development proposals for a new correlator (https://science.nrao.edu/enews/13.7/index.shtml#alma_news), the earliest AT.CBF project execution start date is the ALMA Board meeting date of November 21, 2021, although a start of funding date is not yet known and is likely sometime after this meeting.

We expect that the total elapsed calendar time from start of funding until engineering commissioning of AT.CBF at the ALMA site (or OSF) is up to 5 years. The first ~3 years entails off-site development and

[60] For a 0.84624 USD vs the Euro, the latter of which is the base currency for Mid.CBF cost estimations.
[61] Assuming the TALON-DX Intel Stratix-10 technology node.

testing using one or more[62] off-site development systems as described in section 10. The next 2 years entail on-site integration and testing and formal verification, we believe leaving plenty of slack to deal with unforeseen issues.

Thus, if the start of project execution is ~January 2022, it is expected that a new AT.CBF system could be on-site and fully operational up to 5 years later or ~January 2027.

[62] More than one development system or portion thereof may be required depending on the location of developers.

14 References

[1] Gunaratne T., Carlson B., Comoretto G., Novel RFI Mitigation Methods in the Square Kilometre Array 1 Mid Correlator Beamformer, Journal of Astronomical Instrumentation, Vol. 08, No. 01, 1940011 (2019.)

[2] Carlson B., Pleasance M., TRIDENT Correlator-Beamforer for the ngVLA Preliminary Design Specification, TR-DS-000001, Revision 1 (RELEASE), 2018-09-19.

[3] Warmels R., ALMA Cycle 6 Technical Handbook, Doc 6.3, ver. 1.0, 20 March 2018.

[4] Bhatia R., Yahoubov P., ALMA system block diagram, SYSE-80.04.01.00-004-R-DWG, Version R, 26 May 2016.

[5] Metzner P., Ashton S., Kurlandczyk H., "DTS Theory of Operations", BEND-53.00.00.00-005-A-DSN, Version A, 2010-07-28.

[6] The TANGO Control System Manual, http://ftp.esrf.fr/pub/cs/tango/tango_92.pdf

[7] Pleasance P. et. al., SKA CSP Mid Correlator and Beamformer Sub-element Detailed Design Document (EB-4a), SKA-TEL-CSP-0000066, Revision 1, 2017-12-18.

[8] Gunaratne T., SKA1 CSP Mid Array Correlator and Central Beamformer Sub-element Signal Processing MATLAB Model (EB-7), SKA-TEL-CSP-0000069, Revision 4, 2018-08-16.

[9] Introduction to Software Engineering Institute Processes for SKA Software CDR Deliverables, SKA-TEL-SKO-0000654.

[10] Escoffier R., et. al., Observational Modes Supported by the ALMA Correlator, ALMA Memo 556.

[11] Brogan C., The ALMA 2030 Correlator: Draft Requirements, ALMA 2030 Vision: Design Considerations for a Next ALMA Correlator, Charlottesville Va, Feb. 13, 2020.

[12] Carpenter J., et. al., The ALMA Development Roadmap, ALMA Memo 612, 2018-06-27.

[13] Conversations and notes from: ALMA 2030 Vision: Design Considerations for a Next ALMA Correlator, Charlottesville Va, Feb. 11-13, 2020.

[14] Gunaratne T., Generating Seamless Frequency Channels across Frequency Slices in the SKA1 Mid.CBF, TALON SKA1 MID.CBF Memo 009, 2017-09-07.

[15] Carlson B., Loubser N., SKA CSP Mid Correlator and Beamformer Sub-element Test Specification (EB-3), SKA-TEL-CSP-0000064, Revision 1, 2018-01-19.

[16] Freund R. W., Digital Transmission System Signal Protocol, ALMA Memo No. 420, 2002 September 6.

[17] Denman N., et. al. A GPU-based correlator X-engine implemented on the CHIME Pathfinder, 2015 IEEE 26th International Conference on Application-specific Systems, Architectures and Processors (ASAP), Toronto, ON, 2015, pp. 35-40, doi: 10.1109/ASAP.2015.7245702.

15 Appendix—Discussion Paper: ALMA Talon Correlator/Beamformer in the context of the original ALMA Baseline Correlator

This is a discussion paper written in early 2020, and provided to NRAO, to describe the AT.CBF within the context of the BLC. It is included here as useful auxiliary information, although some of the terminology is not entirely consistent with the main body of this document.

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This is a discussion of the architecture and capabilities of the proposed ALMA Talon Correlator/Beamformer (AT.CBF), starting out by drawing some parallels with the (existing) ALMA Baseline Correlator (BLC) capabilities and configurations to set it in context, but expanding to provide some core understanding of how it works and what it can do as a replacement for the BLC, with some final discussion on upgrading/transitioning to increased bandwidth.

The AT.CBF always operates with the equivalent of the BLC Tunable Filter Banks (TFB) active and all correlation and VLBI beamformer operations occur on TFB Sub-channel outputs.

In the AT.CBF, a TFB Sub-channel is referred to as a Frequency Slice (FS.) Each Frequency Slice is 220[63] MHz wide, with a fixed FS-to-FS separation of 200 MHz across the 2 GHz BB. There are thus 10 dual-polarization[64] FSs across each of the existing 2 GHz BBs, resulting in a total of 10 FSs/BB x 4 BBs = 40 FSs that can be correlated or VLBI beamformed. The amount of bandwidth that can be simultaneously correlated and beamformed depends on processing resources in the installed AT.CBF.

This 220/200 (or exactly 10/9) overlap allows for complete contiguous spectral coverage across each BB, with no gaps, "suck-outs", or spectral anomalies[65] anywhere in the correlator output that would betray FS boundaries. (If desired, the entire collection of 10 FSs can be optionally shifted up or down in frequency by 100 MHz for optimal placement of spectral lines near the middle of FSs although there is normally no need to do so.)

Downstream after FS generation, Frequency Slices are processed in Frequency Slice Processors (FSPs.) In the AT.CBF physical implementation, each FSP processes 2 Frequency Slices, and each FSP can be dynamically configured to be in either Correlator or VLBI (beamformer) "FSP Mode"; all sub-arrays[66] in a particular FSP must be doing either Correlator or VLBI processing, but not both.

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[63] All numbers defining frequencies are approximate for the purposes of this discussion, except where noted.
[64] In the AT.CBF, all processing is always full polarization and any mention of bandwidth includes the full polarized bandwidth.
[65] Well, there are anomalies at some level, but to less than 0.01% in amplitude and 0.001 radians of phase across the full correlated bandwidth, after bandpass calibration.
[66] The limit in the number of independent sub-arrays is the number of antennas in the array. However, for monitor and control purposes a limit of 16 sub-arrays is notional limit.

It is proposed that there are 24 FSPs in the AT.CBF installation to replace the BLC, allowing for processing 48 Frequency Slices, which is equivalent to simultaneous correlation of the full ALMA bandwidth as well as 1600 MHz for VLBI, or for 8 additional Zoom Windows on top of full bandwidth correlation if VLBI is not active. However, the minimum number of FSPs is 20 for full bandwidth correlation capability.

Each FSP receives two Frequency Slices from up to 80[67] antennas. Thus, each FSP has all it needs to perform full-array or multiple sub-array correlation or VLBI beamforming processing (depending on whether it is in Correlator or VLBI FSP Mode) on 2 Frequency Slices. Thus, there are no quadrants or quadrant restrictions as in the BLC.

In each FSP, each Frequency Slice input, for each antenna, can come from any FS in any BB, including duplicates. Thus, each FS can be processed once, multiple times in a different manner, or not at all.

In Correlator FSP Mode, in each FSP each sub-array can be configured independently for normal spectral line or zoom spectral line processing.

Furthermore, in each Correlator FSP independently, each sub-array can be on an independent delay center on the sky.

If so configured[68], at least 20 times faster than sidereal delay tracking can occur within each FSP independently, with no degradation in signal processing fidelity, supporting wide-field on-the-fly mapping.

In normal Correlator spectral line processing, exactly 14880 spectral channels, at a bandwidth of exactly 13440 Hz each and with at least 60 dB of channel-to-channel isolation, are correlated within the central 200 MHz of the FS. Internal processing ensures seamless and linear spacing of spectral channels across all FSs within a BB with virtually no spectral anomalies that would betray FS boundary locations, as mentioned above. Thus, 20 FSPs in Correlator FSP Mode produce 20 FSPs x 2 FSs/FSP x 14880 spectral channels/FS = 595,200 spectral channels.

To throttle the number of channels, post-correlation channel averaging in the AT.CBF by factors of 2, 3, 4, 5, 6, 8, and 10 can be selected in each Correlator FSP independently[69], again producing contiguous linearly-spaced channels across each BB even if each FS is set for a different channel averaging factor, including no channel averaging. Additionally, correlator integration times can be set from the minimum to more than 1 second to further throttle the correlator output data rate, with further integration and channel averaging in the BLC CDP back-end replacement[70], as needed.

[67] 80 antennas as mentioned in ALMA memo 605. The design is scalable up or down in number of antennas as needed, only affecting the number of resources (Talon FPGA boards) needed for processing.
[68] This requires the FSP is in a "Correlator-OTF" FSP Mode, with delay tracking and correlator dump rates synchronized, but otherwise with the same processing as Correlator FSP Mode. Thus, all sub-arrays in each FSP in Correlator-OTF FSP Mode must be similarly configured.
[69] Normally set the same for each FS, however sub-parts of FSs can be individually set for a different channel averaging factor, but not discussed further here.
[70] i.e. in the AT.CBF there is a need for a compute cluster to translate/format correlator visibilities to the required ALMA visibility format.

In Correlator zoom spectral-line processing, a pre-correlation filter, with bandwidth of /2, /4, …, /64 of a Frequency Slice, and tunable anywhere within the FS with at least 10 kHz resolution is available. The width and center frequency of the filter can be set in each Correlator FSP, for each sub-array, independently. Exactly 14880 spectral channels across the central 90% of the zoom filter bandpass are then correlated on the filtered output, producing spectral channels with widths as narrow as exactly 13440/64 = 210 Hz. Zoom and non-zoom spectral channels, when averaged to the same resolution, agree within +/-0.1% in amplitude and +/-0.001 radians in phase, to allow cross-continuum/spectral line justification.

In VLBI (beamformer) FSP Mode, the 220 MHz FS is digitally up-sampled to exactly 224 MHz such that subsequent beamforming processing produces real sampled data stream VDIF outputs of exactly 448 Ms/s, 256 Ms/s, …, 2 Ms/s to be compatible with "VLBI standard data rates" of 1 Ms/s x 2^n . The 448 Ms/s output is not directly at this rate, but sub-channels aligning with other VLBI stations' channels can easily be produced in a capable VLBI FX correlator F-part filterbank.

Clearly, the 448 Ms/s VLBI output is the entire Frequency Slice bandwidth with the central 200 MHz containing no transition-band roll-off, aliasing, or sensitivity losses. Lower rates, coming from VLBI FSP Mode post-beamforming ("beam-channel") tunable filters, can be placed anywhere within the FS. Each of these has a 5% transition band at either edge containing aliasing within it, which quickly washes out in the VLBI correlator due to earth-rotation fringe washing.

Each VLBI FSP beamforms two Frequency Slices, and for each one, 2 VLBI beams can be produced, each on a different delay center on the sky, each producing up to 4 tunable VLBI "beam-channels"[71], each one having a different tunable center frequency and bandwidth (sample rate) as mentioned. A "VLBI beam" is an independent delay center on the sky of whatever desired bandwidth across one or more Frequency Slices across one or more BBs; a "VLBI beam-channel" is a VDIF output sampled data stream spigot at one of the sample rates mentioned, derived from a beam within a Frequency Slice.

In VLBI FSP Mode, for each Frequency Slice and simultaneous with beamforming, 920 channels at exactly 218750 kHz each across the central FS are correlated. Internal processing also ensures these are linearly-spaced and contiguous across Frequency Slices and are normally used for deriving tied-array solutions for VLBI beamforming coherence, where such solutions are determined outside of the AT.CBF itself, and fed-back via updated delay and phase models. Of course, these channels could be used for imaging as well.

Many-bit processing is used throughout the AT.CBF and so there are no correlator or VLBI beamforming sensitivity losses of any significance.

Delay tracking and phase corrections (including earth-rotation phase, LO offset removal, and 90 deg de-Walshing) are virtually perfect using advanced high-fidelity techniques, requiring no post-correlation delay-dependent phase or amplitude corrections. Thus, it is highly recommended that with the AT.CBF in place, the existing antenna-based digitizer clock phase control for fractional delay be turned off.

The correlation processing described includes 90 deg de-Walshing for sideband suppression prior to correlation. An additional FSP Mode, "Correlator-SS", could be developed with sideband separation

[71] In addition to the native 448 Ms/s beam-channel.

correlator accumulation, to allow extraction of both sidebands. Likely this FSP Mode would not include zoom and may have a factor of 2 reduction in the number of channels, TBC.

To increase the bandwidth, either with X times the number of digitizers at the same digitized bandwidth as now, or X times faster digitizers[72], X copies of the described AT.CBF system can be deployed whilst retaining the architecture and existing FSPs. For example, if there X=2 more digitizers at the same digitized bandwidth as now, a carbon copy of the BLC-replacement AT.CBF system (estimated at 8 x 19" racks requiring up to 100 kW[73]) with no design changes, can be deployed. As another example, if the number of digitizers stays the same, but the digitized bandwidth of each goes up by X=2, then the FSPs in place can stay with no design changes, double the FSPs are added to process the double bandwidth, and the portion of the AT.CBF that produces the Frequency Slices is re-programmed and hardware added, to handle the doubling of digitized bandwidth.

[72] X need not be an integer. It is only necessary that a digitizer sample rate is chosen that is compatible with translation to the frequencies needed for the 10/9, 220/200 MHz oversampling coarse filterbank in AT.CBF.
[73] For 80 antennas and 24 FSPs. If the number of antennas is reduced to 66 and the FSPs to 20, power is reduced accordingly.

16 Appendix—CVs of Key NRC Personnel

Brent R. Carlson

Brent.Carlson@nrc-cnrc.gc.ca
Dominion Radio Astrophysical Observatory
Herzberg Astronomy and Astrophysics
National Research Council of Canada
P.O. Box 248, Penticton, BC, Canada, V2A 6J3

Summary:

Nearly 30 years of hardware and software design experience in radio astronomy instrumentation and systems engineering. This includes signal processing systems engineering, formal requirements definition, large system hardware and software architecture development, specification and development of digital boards with embedded processors and FPGAs, FPGA and ASIC design, implementation, and test using Verilog HDL, and digital signal processing algorithm development, in particular techniques for radio astronomy signal processing.

Key innovations include: incoherent clocking, currently in the research phase, as an all-COTS digital fiber, all-digital method for radio telescope clock and timing; the Sample Clock Frequency Offset (SCFO) scheme incorporated into the SKA1 Mid telescope design; the Frequency Slice Architecture (FSA), the signal processing architecture for the SKA1 Mid Correlator/Beamformer; and the 'WIDAR' technique for the (Expanded) Very Large Array (VLA) correlator.

Skills:

- The ability to envision novel solutions to solve complex problems or in areas where there are existing solutions with limitations.
- Formal systems engineering including requirements analysis, definition, allocation, and flow-down to lower levels.
- Complex system design from concept to completion and operations, including conceptualization at all levels for hardware and software partitioning.
- Development of novel signal processing, electrical/thermal/mechanical design, data handling, protocols, and methods as required for a particular project.
- Solid foundation in ADC fundamentals, digital signal processing, high-speed digital FPGA and ASIC design, as well as high-speed PCB design concepts for the latest generations of FPGAs' high-speed serial transceivers.
- Prolific and professional technical writing and technical product output.
- FPGA Verilog RTL design, simulation, test, as well as gate-level test, and device testing in target PCB environments.
- ASIC Verilog RTL design, simulation, and test. Verification of RTL design against gate-level Verilog netlist (.vo, .sdo.)

- Study and development of algorithms and mathematics of signal processing using custom 'C' code, MathCad, or other suitable tools as required.
- 'C' programming for embedded real-time applications and non-real-time applications.

Education:

- Over the years, several design tool courses, including Mentor Graphics FPGA Advantage, Xilinx advanced high-speed FPGA design, as well as project management training in managing technical personnel. Generally, I learn new design tools and concepts on the job as required, augmented as necessary with dedicated training.
- Qualification for Professional Engineering Status (previous P. Eng. status acquired in Alberta.)
- Practical Reliability Engineering. Two day course offered by the Electronics Test Center in Edmonton, May 1989.
- Electromagnetic Compatibility Engineering. Short course from the Center for Professional Advancement (Dallas, April 1988.)
- Bachelor of Science in Computer Engineering from the University of Alberta, 1987 (grad. Dec. 1986.)
- Grade 12 from Prince George Secondary School, 1981.

Work Experience:

November 2016 to present: Senior Designer/Design Engineer (RCO-5 level) for the National Research Council of Canada.

- October 2018 to present, "incoherent clocking" laboratory research project. This novel method, using all-COTS digital fiber optics and all-digital methods, aims to provide radio telescopes with cost-effective clock and timing by measuring antenna independent LOs and correcting the data accordingly. If successful, this method may completely obsolete existing methods for clock and timing distribution as well as enable "at feed" digitization where it is currently cost prohibitive or impractical.
- From November 2016 to October 2018, SKA1 CSP (Central Signal Processor) Systems Engineer and domain expert responsible for requirements analysis, allocation, flow-down, and definition. Additionally, SKA1 Mid.CBF and SKA1 CSP signal processing architect and domain expert, as well as led study and development of the ngVLA CSP reference design.

Sept/Oct 2016: Assistant Director NRAO Central Development Laboratory, Charlottesville Va.

April 1998 to August 2016: Senior Designer/Design Engineer for the National Research Council of Canada.

- From mid-2012 to mid-2016, domain expert and chief system engineer for the Canada-led SKA CSP consortium bid to lead the SKA CSP consortium. During this time developed the "PowerMX" platform concept/architecture concept applicable to all SKA signal processing. Spearheaded initiative for a "Digital Platform Study Group" to try to bring the community together to agree on a common platform for SKA signal processing. In a meeting at the SKA Project Office in January 2013, presented concept for "WIDAR" LO offset concept for self-interference suppression even in direct-digital sampling receivers.

- From early 2011 to 2012, provide development support for the "Kermode" ATCA high-performance multi-FPGA (Xilinx) card, including writing technical specifications/data sheet, developing and writing use-case studies, providing input/feedback on architecture, and researching various technical details including internal Xilinx FPGA architecture and connectivity restrictions. Develop and write User Manual, production and prototype test plans, exhaustive spreadsheet of FPGA pinouts and board connectivity for users, and participate in design reviews. Also during this time, continue to participate in the international SKA signal processing domain as a Canadian delegate/institute expert and continue to wrap-up EVLA documentation as well as provide technical support for the correlator as requested.
- From early 2010 to early 2011, develop new concepts and architectures for signal processing for the international Square Kilometer Array (SKA), write technical documents, and present concepts at the Conceptual Design Review in early April 2011. The SKA is an international effort to construct a cm-wave radio telescope, ~100X more powerful than the VLA, and Canada is a participant. These concepts included a novel mechanism for building a large 2D systolic array correlator, with nearest-neighbour printed wiring connections for low-cost, reliable operation; development of a specification for the "X421" ASIC, with facilities for "visibility-based addressing" for real-time image processing; and development of central phased-array/beamformer processing concepts. Also, develop straw-man concept for fully-integrated monolithic phased-array receiver, with concentration on electrical-physical layout, signal routing, and digital signal processing.
- From mid-2002 to early 2010, principle engineer and technical lead for the EVLA 'WIDAR' correlator project. The development team consisted of 1 project head, 1 project management assistant, 4 hardware design engineers, 1 software engineer, 2 technologists, and production staff in Canada, as well as 3 software engineers, and various numbers of liaison/test scientists in New Mexico. This was a $20 million project to build a wideband (16 GHz) cross-correlation spectrometer for the (Expanded) Very Large Array radio telescope in New Mexico U.S.A. Duties and responsibilities included system signal processing and architecture development; system design; Altera FPGA RTL design, implementation, and test; correlator ASIC RTL design, test, and qualification; low-level hardware test and debug using wideband Agilent Infinium DSO and other test equipment as appropriate.

  Several types of circuit board assemblies were designed in-house for this project, the largest of which was ~15" x 19", 28 layers, containing 64 F672 ASICs, 87 FPGAs (F256 to F672), memory, and an embedded PC/104+ CPU module. The main system clock speed was 256 MHz, but with most inter-board differential line rates at 1.024 Gbps, with some up to 3.125 Gbps (XAUI.) Built FPGA 1G and 10G Ethernet UDP/IP packet generator/handler for high-speed, processor independent data output.

  Additional duties included working with/guiding mechanical/thermo-electrical/electrical designers to meet system requirements; guide/manage set up of project web page; writing requirements and technical documents; writing RFP documents for formal contract bidding and tendering of major components for the Government of Canada; presenting at formal design reviews; participating in system testing and debugging, and managing set up of in-house production handling of circuit boards for final assembly, testing, and Q/A; system reliability study using the Relex Reliability software tool. The installed correlator system consists of 16, 24" x 7' racks, each rack containing 16, 15" x 19" circuit board assemblies, and dissipating up to 10 kW each.

- From mid-1999 to early 2002, develop and perform simulation testing of a novel (patented) concept for wideband correlator signal processing called "WIDAR". Develop detailed architecture for a "WIDAR" correlator for the U.S. Expanded Very Large Array. This was new for the time, and allowed for ~16X the capability in the correlator compared to what was thought possible with the technology of the day.
- From 1998 to mid-1999, work with industrial and university researchers to refine the technical specifications and design parameters for the Large Adaptive Reflector project, a novel telescope concept for the SKA. Develop and prepare presentation materials for visualization of the telescope. Develop and study straw-man photogrammetry system for telescope surface measurement.

February 1997 to April 1998: Operations manager for the Canadian Space VLBI Correlator – a VSOP mission element.

- Main Canadian representation for mission technical decisions involving Japanese and other international mission elements (ground radio telescopes, tracking stations, correlators.)
- Oversight of many of the Canadian operations matters for the VSOP mission. Communication/coordination with members of other mission elements during IOC (In Orbit Checkout) to help quantify problems/characteristics with the space radio telescope, NASA-DSN/NRAO/NAO tracking stations, ground radio telescopes, and recording systems.

August 1990 to February 1997: Group leader and senior project engineer for the Canadian Space VLBI Correlator Project, with primary funding from the Canadian Space Agency.

- Hardware and software system architecture design of digital correlator for Space Very Long Baseline Interferometry (Space VLBI.) Included system level hardware DSP design and design of system level software for UNIX client and embedded real-time VxWorks servers. With a small "diverse" team, and poorly funded and supported, this project successfully went from concept to full operations, and was a major component of the VSOP program, eventually processing several hundred observations over a period of ~5 years, many observations tapping into some of the unique capabilities of the system.
- Development of DSP (Digital Signal Processing) algorithms and simulation of radio astronomy signals for aperture synthesis (Gaussian noise simulation, FIR filters and SSB mixing for Doppler shift and delay of simulated astronomical data, autocorrelation, zero-insertion interpolation for multi-rate signal processing, delay and phase compensation, phase-cal tone extraction, complex cross-correlation) using MathCad and in-house developed behavioural simulator written in C.
- Design and implementation of digital logic for DSP functions using Xilinx 4000 series devices for 32 Msample/sec operation. Design and implementation of VME/VSB Station Module for station (antenna) based DSP with total aggregate bit rate of 512 Mbps. This was a 9U x 400mm PCB containing approximately 50 Xilinx FPGAs. Design of FIR filter in FPGA to provide enhanced high resolution spectral-line processing capability in the correlator.
- High level system software design for the correlator:

  -Complete system level software design including definition of functionality of embedded and host control computers using Data Flow Diagrams (DFDs), state diagrams, structure diagrams etc. This design was used as a foundation for the implementation of all host and embedded software.

-Design of batch control language and Graphical User Interface functions for controlling the operation of the correlator.

-Specification of requirements of batch compiler, GUI functionality, and graphics display functionality for implementation by external software contractor.

- Design and implementation of embedded real-time software in 'C' for antenna-based processing and VLBI tape recorder control using the VxWorks real-time OS.
- Provide group leadership and supervision on correlator implementation to team comprised of two computer scientists, one technologist, and one geophysicist working on the project. Interact with project Principle Investigator (astronomer-engineer) and geodicist to ensure that all required astronomical and geodetic processing capabilities are implemented in the correlator.
- Spend about 5-10% of total time on project management (budgets, forecasting using Microsoft Project, reporting on developer activities etc.). Specification of job descriptions and interviewing of co-op students to work on the correlator project. Write regular reports to the Canadian Space Agency program manager on the development of the correlator.
- Prepare and give technical presentations to technical and non-technical audiences of 10 to 100 people on the operation and implementation of the correlator. This includes two formal Canadian Space Agency design reviews and numerous internal and external presentations.

May 1986 to June 1990: Senior hardware and software design engineer with IDACOM Electronics Ltd. (purchased in July 1990 by Hewlett Packard.)

- Hardware development of ISDN Primary Rate Interface (PRI - T1/CEPT) on a 68020 CPU VME board (joint project with Siemens on which I was the project leader.) Provide direction to S/W developers and marketing on the board.
- Hardware development of ISDN Basic Rate Interface VME board with on-board 68000 processor.
- Maintenance and upgrade of proprietary embedded operating system 'C' code (for 1 year.) Written on Sun 3 and tested using a 68K emulator for debugging.
- Test and develop modifications to bring the IDACOM "PT" into compliance with FCC/VDE class B EMI requirements.

July 1981 to April 1986: Junior hardware engineer and test technologist with IDACOM while attending the University of Alberta.

- Re-package and improve design of a high power density and high reliability switching power supply for new product integration. Received an award and bonus for the design.
- Worked full and part time in the test department of IDACOM. Duties included testing and repair of switching power supplies, system testing using defined procedures, backplane testing etc.

Awards and Patents:

NRC-HAA 2017 Certificate of Excellence, Outstanding Team, for the SKA CSP Team.

Recipient of the Queen's Diamond Jubilee Medal for inventing WIDAR, January 2013.

NRC-HIA 2010 Internal Award, EVLA Correlator Team.

Patent: Parallel Correlator Architecture (WIDAR), Carlson and Dewdney, U.S. Patent No. 7,061,992 (expired), Canadian Patent No. 2,362,776.

Publications:

Journal Papers

Gunaratne, T., Carlson, B., Comoretto, G., Novel RFI Mitigation Methods in the Square Kilometre Array 1 Mid Correlator Beamformer, Journal of Astronomical Instrumentation, Vol. 8, No. 1 (2019) 1940011, DOI: 10.1142/S225117171719400117.

Carlson, B.R., Incoherent clocking in coherent radio interferometers, IEE Electronics Letters(2018), 54 (14):909. (https://goo.gl/hun6ni)

Carlson, B., Gunaratne, T., "Signal processing aspects of the sample clock frequency offset scheme for the SKA1 Mid telescope array", in 32nd URSI GASS, Montreal, August 19-26, 2017.

Carlson, B. [2016] "Sample Clock Frequency Offset (SCFO) Resolution Team 3 Investigation", SKA-CSP Memo-0021 (https://arxiv.org/abs/1812.06972)

The Expanded Very Large Array (invited paper)
Perley, R., Napier, P., etc., Carlson, B., Fort, D., Dewdney, P., et al, Proceedings of the IEEE, Vol. 97, No. 8, August 2009.

Efficient Wideband Digital Correlation
B. R. Carlson and P. E. Dewdney, Electronics Letters, IEE, Vol. 36 No. 11, p987, 25th May, 2000..

The Canadian S2 VLBI Correlator : A Correlator for Space VLBI and Geodetic Signal Processing
B. Carlson, P. Dewdney, T. Burgess, R. Casorso, W. T. Petrachenko, and W.H. Cannon, PASP, 111, 1025, pp 1025-1047, 1999.

David Alan Del Rizzo

Dave.DelRizzo@nrc-cnrc.gc.ca 104-4400 McLean Creek Road, Okanagan Falls BC V0H 1R6

Profile

An intuitive thinker, I enjoy being challenged by problems and working to apply novel techniques in an approach to excellent solutions. I am always learning.

Experience

RESEARCH COUNCIL OFFICER, RADIO SOFTWARE TEAM LEAD

NATIONAL RESEARCH COUNCIL CANADA / HAA / DRAO – 2000-PRESENT

Member of operations and software development team, specializing in task automation, data processing and visualization, database design and management, development of monitor & control tools and graphical user interface development.

At various times, a team member involved in:

- RFInd (Radio Frequency Interference Novelty Detection)
  Project management and software design & development for an in-house system to monitor and detect spurious Radio Frequency Interference at the DRAO site, using advanced machine learning algorithms and processing techniques.
- SKA Mid.CBF (Square Kilometre Array 'Mid' Correlator Beam Former)
- SKA DISH Digitizer
  Design and development of software used in the monitor and control of firmware deployed on the Talon-DX platform (an Intel Stratix10 FPGA-based board developed and built at NRC) that will service both the SKA Mid.CBF correlator and the SKA DISH Single Pixel Feed Receiver (digitizer). Development of software tools for the TANGO C++ monitor and control device server software workflow from design to implementation in support of teams on both projects.
- Kermode DSP Board
  Embedded software development used in firmware monitor and control.
- MITR (Module Instance Tracking & Reporting) Database
  Design and implementation of a flexible module tracking database with web-based front end, to assist in the organization and maintenance of processes, materials and modules during the build phase of the EVLA project at DRAO.
- WIDAR Correlator
  Contributed to the design and development of software-based monitor and control systems. In particular, Graphic User Interfaces (GUIs) used in system configuration, test data visualization and system diagnostics.
- Canadian Galactic Plane Survey
  Telescope Operator for the DRAO Synthesis Telescope (7 x 8m aperture synthesis radio interferometer) managing the day-to-day scheduling and data processing pipeline, automation of processing tasks, organization of archival data and the development of countless software tools used in the maintenance and ongoing operation of the telescope facility.

CORRELATOR OPERATIONS, UNIVERSITY OF CALGARY – 1997-2000

Member of a small team tasked with the management and operations of the Canadian Space Very Long Baseline Interferometry (SVLBI) correlator located at the DRAO in Penticton. The SVLBI correlator marked the Canadian contribution to the Japanese-led VLBI Space Orbital Programme (VSOP) project involving the HALCA orbital radio telescope. Software development included database design, data visualization and Graphical User Interface (GUI) development.

Education

York University (Toronto, Canada) – Honours BSc Physics & Astronomy, 1995

Skills

Background knowledge of Radio Astronomy, including radio telescope operations, techniques and principles

Experience with correlator design and implementation, particularly aspects of monitor and control

Data visualization • Database design • Scripting • Task automation • Data organization & management • Embedded software • Continuous integration • Code generation • Workflow implementation • Radio telescope operations

Project management & team leadership

Software design and development environments:
Python, Java, C/C++, Linux, MySQL, Postgres, PHP, Perl, IDL, HTML, XML, JSON

Software tools and systems:
TANGO Control System, Yocto Build System, Git, Gitlab, cmake, Google Mock/Google Test, Docker, OpenProject

Certified SAFe Practitioner (2019)

References

Brent Carlson - DRAO
Sean Dougherty - NRAO/ALMA
Andrew Gray - DRAO

THUSHARA KANCHANA GUNARATNE

Research Council Officer (RCO)
DSP / FPGA Engineer
National Science Infrastructure (NSI)
National Research Council (NRC) CANADA
Dominion Radio Astrophysical Observatory (DRAO)
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EDUCATION

BSc. Eng.	Electronics & Telecom: Engineering, University of Moratuwa, Sri Lanka	1998-2003
Engineering Council (UK) - Certificate		2000
MSc.	Electrical Engineering, University of Calgary	2004-2006
Thesis Title:	Beamforming of Temporally Broadband Bandpass Plane Waves using 2D FIR Trapezoidal Filters	
PhD.	Electrical Engineering, University of Calgary	2007-2011
Thesis Title	Beamforming of Broadband Bandpass Signals using Multidimensional FIR Filters	
Postdoc.	Multidimensional Signal Processing (MDSP) Group, University of Calgary	2011-2013
	International Center for Radio Astronomy Research (ICRAR), Curtin University, Australia	2013-2014

EXPERIENCE

Research Council Officer, Signal Processing — Feb. 2014– Present
Herzberg Astronomy and Astrophysics (HAA) - NRC Canada

Responsibilities: Design and implementation of state of the art signal processing modules for applications in radio astronomy

Relevant Research Projects:

- Design and implementation of firmware blocks for Talon Demonstrator Correlator (TDC)
- Modelling the signal chain of the SKA1 Mid Correlator Beamformer (CBF) using MATLAB
- Verification of Sample Clock Frequency Offset (SCFO) method for interference rejection
- Design and implementation of over-sampled and critically-sampled polyphase DFT filter-banks, ReSamplers, Digital Down Convertors and Up-Samplers

Postdoctoral Research Fellow — Jun. 2013-Jan.2014
ICRAR, Curtin University, Western Australia, Australia

Responsibilities: Verification of the SKA-Low Phased Array front-end

Postdoctoral Fellow — Oct. 2011-Apr. 2013
Department of Electrical & Computer Engineering, University of Calgary

Responsibilities: Conducting research, preparing internal-reports & manuscripts, mentoring fellow graduate students in the MDSP Group

Research Assistant Jun. 2004 – Sep. 2011

MDSP Group, Department of Electrical & Computer Engineering, University of Calgary

Responsibilities: Conducted research, prepared internal-reports & manuscripts, presented at symposia

PUBLICATIONS

- T. Gunaratne, B. Carlson, and G. Comoretto, "Novel RFI Mitigation Methods in the Square Kilometre Array 1 Mid Correlator Beamformer", J. Astron. Instrum., vol. 08, no. 01, Feb. 2019.
- T. Gunaratne and A. Peens-Hough, "Modeling of RFI and RFI Mitigation Techniques in SKA1 Mid Telescope," 2019 RFI Workshop - Coexisting with Radio Frequency Interference (RFI), Toulouse, France, 2019.
- T. K. Gunaratne, "Generation of Coherent Signals for the Verification of Signal Processing Algorithms in Radio Astronomy, " 2019 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing (PACRIM), Victoria, BC, Canada, 2019.
- B. Carlson and T. Gunaratne, "Signal processing aspects of the sample clock frequency offset scheme for the SKA1 mid telescope array", in 2017 XXXIInd General Assembly and Scientific Symposium of the International Union of Radio Science (URSI GASS), 2017.
- M. Pleasance, H. Zhang, B. Carlson, R. Webber, D. Chalmers, and T. Gunaratne, "High-performance hardware platform for the Square Kilomtre Array mid correlator amp; beamformer", in 2017 XXXIInd General Assembly and Scientific Symposium of the International Union of Radio Science (URSI GASS), 2017.
- A. Madanayake, C. Wijenayake, D. G. Dansereau, T. K. Gunaratne, L. T. Bruton and S. B. Williams, "Multidimensional (MD) Circuits and Systems for Emerging Applications Including Cognitive Radio, Radio Astronomy, Robot Vision and Imaging," in IEEE Circuits and Systems Magazine, vol. 13, no. 1, pp. 10-43, First-quarter 2013.
- Thushara K. Gunaratne, Len Bruton and Pan Agathoklis, "Broadband Beamforming of Focal Plane Array (FPA) Signals using Real-Time Spatio-Temporal 3D FIR Frustum Digital Filters", in IEEE Transactions on Antennas and Propagation, vol. 59, no. 6, pp. 2029-2040, 2011.
- Arjuna Madanayake, Thushara K. Gunaratne and Leonard T. Bruton, "Reducing the Multiplier-Complexity of Massively Parallel Polyphase 2D IIR Broadband Beam Filters", in Circuits, Systems, and Signal Processing. Published Online 22-11-2012.

COLLABORATORS

Gianni Comoretto (INAF), Adriaan Peens-Hough (SARAO), Mitch Mickaliger (U. Manchester), H.L.P.A. Madanayake (FIU), Ian Morrison (Curtin University), Len T Bruton (U. Calgary), Pan Agathoklis (U. Victoria, BC), Willem van Straten (ATU), David Wilson (ATU).

HONOURS & ACHIEVEMENTS

- Certificate of Excellence : Individual, National Research Council 2017

- Certificate of Excellence : SKA CSP Team, National Research Council 2017
- Meritorious Candidate, NSERC Postdoctoral Fellowship Competition 2012
- Graduate Student Productivity Award, Dept: of Elect: & Comp: Eng:, University of Calgary 2011
- First Author of one of the ten Honor Mentioned Student Papers – IEEE ISCAS 2007
- MICRONET Scholarship, MICRONET R&D, CANADA 2007-2008
- UNESCO Team Gold Medal for the Valedictorian
  Faculty of Engineering, University of Moratuwa, Sri Lanka 1998-2003

DR. STEPHEN T. HARRISON

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Work Experience

- **Adjunct Professor** July 2019–Present
  University of Victoria–Victoria, B.C.
  - Supervise graduate students and support collaborations between DRAO and UVic.

- **Digital Engineer** September 2016–Present
  Dominion Radio Astrophysical Observatory (NRC)–Penticton, B.C.
  - FPGA development lead: Square Kilometer Array (SKA) dish digitizer.
  - High-performance DSP solutions for radio astronomy applications using FPGAs.
  - Wideband spectrometers, polyphase filter banks, digital downconverters.
  - Hardware test automation and data analysis.

- **Firmware Engineer (Remote, Part Time)** September 2013–June 2016
  PMC-Sierra, Ltd./Microsemi Corp.–Burnaby, B.C.
  - Debug system-level issues through OS, embedded software, and digital design layers.
  - Develop automated hardware/software regression tests using C++ and Tcl.
  - Design, develop, and maintain internal automation tools.

- **VLSI Engineer** September 2009–June 2012
  PMC-Sierra, Ltd.–Burnaby, B.C.
  - Design and document telecommunications system blocks using Verilog and VHDL.
  - Verify system block designs using Verilog, VHDL, and Specman testbenches.
  - Implement technology standards including Ethernet, DDR2/3, EPON, and OTN.
  - Target designs for 65nm and 40nm TSMC processes, Altera and Xilinx FPGA devices.

- **Software Developer** June 2005–June 2006
  SaneWave–Vancouver, B.C.
  - Design and develop cross-platform desktop applications in C++.
  - Develop and debug embedded software for audio processing devices in C.
  - Develop, debug, and test USB audio drivers on Windows XP and MacOS X.

- **Software Developer/Product Technician** January 2004–May 2005
  Andian Technologies, Ltd.–Burnaby, B.C.
  - Maintain SolidTrack rail geometry measurement software.
  - Design and implement dynamic rules-based data analysis system.
  - Produce documentation including user manuals, mechanical, and electrical drawings.

Training

- Managing Projects (NRC, 2017)
- SystemVerilog for Verification (Hardent, 2019)
- Introduction to Universal Verification Methodology (Hardent, 2020)

Education

- **Doctor of Philosophy (Electrical Engineering)** September 2012–December 2016
  University of Victoria–Victoria, B.C.
  - **Dissertation:** Time Compression Overlap Add (TC-OLA) for Wireless Communications.
  - **Software-Defined Radio:** Wideband receivers, polyphase downconverters, SDR architectures, land mobile radio systems.
  - **Digital Signal Processing:** Broadband beamforming, adaptive predistortion, music information retrieval.

- **Bachelor of Engineering (Electrical)** January 2007–April 2009
  University of Victoria–Victoria, B.C.
  - Digital Signal Processing option, with distinction.
  - Andreas Antoniou Medal for Digital Signal Processing.
  - APEGBC Achievement Award.

- **Electrical Engineering Bridge** July 2006–December 2006
  Camosun College–Victoria, B.C.

- **Diploma of Technology (Electronics)** September 2001–April 2003
  British Columbia Institute of Technology–Burnaby, B.C.
  - Computer Control option, with honours.

Publications and Posters

- **S. Harrison**, R. Coles, T. Robishaw and D. Del Rizzo, "RFI Novelty Detection using Machine Learning Techniques," in *RFI2019: Coexisting with Radio Frequency Interference.*
- T. Robishaw, **S. Harrison**, D. Del Rizzo, R. Messing and B. Robert, "Bustin' Makes Me Feel Good: A Low-Cost Cell Buster for the 850 MHz Band," (Poster) in *RFI2019: Coexisting with Radio Frequency Interference.*
- N. Bruce, **S. Harrison**, P. F. Driessen, R. Herring, "Development of a Phased-Array Ionospheric Imaging System," in *Proc. 2019 IEEE Pacific Rim Conf. Commun., Comput. and Signal Process.*
- R. Coles, **S. Harrison**, D. Del Rizzo and T. Robishaw, "Discovering Radio Frequency Interference using Machine Learning Methods," (Poster) in *2019 McGill Physics and Artificial Intelligence Workshop.*

- **S. Harrison**, T. Robishaw and G. J. Hovey, "A Software-Defined Spectral Line Observing System for the DVA1 Telescope," in *Proc. 2018 2nd URSI Atlantic Radio Science Meeting*.
- **S. Harrison**, G. J. Hovey, B. Veidt, Z. Ljusic and T. Burgess, "A Digital Beamformer for the Advanced Focal Array Demonstrator (AFAD)," in *Proc. 2018 SPIE Astronomical Telescopes and Instrumentation*.
- **S. Harrison** and P. F. Driessen, "Robust TC-OLA Reception With Frequency Domain Equalization for Ultrawideband (UWB) Applications," *IEEE Communications Letters*, vol. 21, pp. 656–659, Mar. 2017.
- **S. Harrison** and P. F. Driessen, "Time-Compression Overlap-Add: Description and Implementation," in *Proc. 2015 IEEE Pacific Rim Conf. Commun., Comput. and Signal Process.*, pp. 64–69.
- **S. Harrison** and P. F. Driessen, "Novel UWB and Spread Spectrum System Using Time Compression and Overlap-Add Techniques," *IEEE Access*, vol. 2, pp. 1092–1105, Sep. 2014.
- I. Moazzen, **S. Harrison**, P. Agathoklis and P. F. Driessen, "A Nested Microphone Array for Broadband Audio Signal Processing," in *Proc. 2013 IEEE Pacific Rim Conf. on Commun., Comput. and Signal Process.*, pp. 377–382.
- V. K. Arora and **S. Harrison**, "Upscaling River Networks for use in Climate Models," *Geophysical Research Letters*, vol. 34.

Mentoring

- **As Course Instructor**
  - ECE 590 - DSP Applications in Radio Astronomy (University of Victoria, 2020).
- **As Academic Supervisor**
  - Nick Bruce, PhD (2022 Expected).
- **As Outside Committee Member**
  - Colter McQuay, MASc (2019), *License Free Communication using Digital Mobile Radio Standards and Spread Spectrum.*
  - Ahmed Youssef, PhD (2018), *Enhancement of Target Detection Using Software-Defined Radar.*
- **As Co-op Technical Supervisor**
  - Jean-Pierre Lavigne, *Polyphase Filterbank Updates for the DRAO RFI Monitor.*
  - Neil Brubacher, *Solar Telescope Upgrade using Software-Defined Radio.*
  - Rory Coles, *Novelty Detection in Radio Frequency Interference using Machine Learning.*
  - Aneet Lakhani, *Oversampled Polyphase Filterbank for the John A. Galt 26m Telescope.*

Patents

- **S. Harrison** and P. F. Driessen, "Spread spectrum method and apparatus," U.S. Patent 9 479 216 B2, Oct. 25, 2016.

Michael Pleasance

National Research Council of Canada

Michael.Pleasance@nrc-crnc.gc.ca

A systems engineer / project manager with fifteen years of experience in signal processing applications for Radio Astronomy and Airborne Imaging Radar systems. Areas of expertise include system design, real-time software engineering, FPGA design and project management.

Recent Key Professional Contributions:

- Successfully led the Mid.CBF Team through the SKA design phase by achieving a full pass at the Mid.CBF critical design review.
- Executed architectural design of the Mid.CBF Frequency Slice Architecture by mapping Brent Carlson's Frequency Slice Architecture concept onto the existing Mid.CBF hardware development path. This resulted in significant cost savings and risk reduction with minimal impact on the schedule to Mid.CBF CDR.
- Re-organized Mid.CBF development team to better distribute responsibility / ownership, resulting in clear areas of responsibility and an increase in team performance.
- Proposed design changes to the Mid.CBF PSS Beamformer which could reduce the number of FPGAs required by a factor of two, leading to significant cost and power savings.
- Proposed design changes to Mid.CBF to use passive fibre interconnect where possible rather than FPGA based switches, leading to cost and power savings.
- Designed and implemented a heterogeneous computing framework using Java and OpenCL to leverage the rapid development of Java with the processing power of OpenCL on multi-core CPUs and GPUs. This framework has been used as the basis for several projects at MDA.

Key Competencies

Project Management
- Work package breakdown
- Work package effort estimation
- Schedule / dependency management
- Resource allocation

System Engineering
- System architecture and decomposition
- Requirements and interface analysis
- Verification planning and execution

Tools:
- Intel Quartus (Stratix-10)
- Intel QSys/Platform Designer
- Mentor Graphics ModelSim
- Eclipse IDEs
- Microsoft Developer Studio

FPGA Design
- Part selection / resource estimation
- RTL Implementation of DSP algorithms
- Simulation and design verification
- FPGA power estimation

Software Engineering:
- Real-time DSP software design
- Object-oriented software design
- Complete software life-cycle

Languages:
- Verilog / SystemVerilog
- Java
- C / C++
- OpenCL
- Scripting languages (Perl, TCL, etc)

Education

2004 **UNIVERSITY OF BRITISH COLUMBIA** **VANCOUVER, BC, CANADA**

Bachelors Of Applied Science
Engineering Physics Major – Computer Science Specialization

Experience

2016 - Present **NATIONAL RESEARCH COUNCIL OF CANADA** **PENTICTON, BC, CANADA**

2016 – Present: SKA1-Mid Correlator / Beamformer Lead (Mid.CBF)

- Sub-element lead responsible for system architecture, prototyping activities, construction costing and preparation for sub-element CDR.
- Manage fifteen person, internationally distributed engineering team
- Manage Mid.CBF risks and technical performance measures
- Interface with vendors and other members of the SKA community
- Manage / supervise Digital Signal Processing group at DRAO

2004 - 2016 **MACDONALD, DETTWILER AND ASSOCIATES LTD.** **RICHMOND, B.C., CANADA**

2015 – 2016: Project Engineer, : SKA1-Mid Correlator / Beamformer Lead (Mid.CBF)

- MDA technical lead, working closely with NRC technical lead to design Mid.CBF architecture
- Manage Mid.CBF prototyping plan and schedule for fifteen person, internationally distributed team
- Manage Mid.CBF risks and technical performance measures
- Interface with other members of the Central Signal Processing consortium and SKA Office
- Contribute to Mid.CBF construction costing and development plan

2014 – 2016: System Engineer, SKA-Mid Central Beam Former

- Design FPGA based system for performing beamforming for pulsar search and timing functions of SKA Mid radio telescope targeting Altera Stratix-10 FPGAs.
- Develop interface specifications for communication with internal and external sub-systems
- Assist with requirements analysis for PSS/PST Beamformer
- Working closely with NRC group based at Dominion Radio Astrophysical Observatory
- Gaining experience with FPGA design flow and Altera and ARM development tools

2004 – 2014: System/Software Engineer, Imaging Radar Systems

- Signal processing / post processing lead for SIVAM Ground SAR Processor upgrade
- Prototyped new hardware for CP140 Extension Project
- Developed and implemented improved Doppler Centroid Estimation algorithm for CP140 GMTI processor using Matlab for algorithm design and C++ for real-time implementation.
- Performed customer witnessed factory and on-site acceptance tests for GRPF
- SAR Processor and Integration/Test Team Lead for GRPF system
- Write and perform formal system sell off procedures
- Operate Radar and analyze data for Contractor Flight Tests
- Integrate system at subcontractor lab
- Design, implement and test Control and Ingest components for Airborne radar system gaining expertise in VxWorks and MCOS operating systems.

Michael Smith — Curriculum Vitae

EDUCATION AND PROFESSIONAL LICENSURE

Licensed Professional Engineer (P.Eng.) Engineers and Geoscientists BC, Canada

Bachelor of Science, Computer Engineering Queen's University, Ontario, Canada (2004)

WORK EXPERIENCE

Dominion Radio Astrophysical Observatory, National Research Council of Canada, Penticton, British Columbia, Canada

Telescope Computer Engineer, September 2016 to present

- Design and implementation of distributed control software for the Observatory's telescopes using C++, Python, and GoogleTest/GoogleMock for unit testing
- Maintaining the Observatory's Gitlab source code repository as well as continuous integration using Gitlab-CI
- Project manager for the integration of new software systems as well as mechanical upgrades to the Observatory's largest single-dish telescope

Viion Systems Inc., Victoria, British Columbia, Canada

Hardware and Software Engineer, April 2015 to August 2016

- Maintaining the embedded Linux build environment and automation scripts for deploying over-the-air updates to the company's live cameras in the field
- Design and simulation of FPGA firmware for real-time processing of video data over MIPI bus and interfacing to image sensors and lens controllers over I2C/SPI
- Analysed technical specifications of digital imaging sensors and evaluated emerging digital imaging technologies

Contech Enterprises Inc., Victoria, British Columbia, Canada

Multidisciplinary Hardware/Software Engineer, September 2012 to April 2015

- Implemented firmware for very lost-cost/low-power retail products in C/assembly on Freescale RS08 microcontroller with 256 bytes of RAM
- Transferred product designs to overseas contract manufacturers and regularly solved technical issues to ensure production and shipping dates were met

Redlen Technologies, Victoria, British Columbia, Canada

Senior Engineer, March 2012 to September 2012

- Extended in-house test fixtures and software to function as customer evaluation platforms and provided one-on-one training to customers
- Performed failure mode analysis on radiation detector products, created Python scripts to aggregate and extract statistics from large volumes of test result data

Test Systems Engineer, June 2010 to March 2012

- Responsible for designing and implementing robust test fixtures and software for characterizing radiation detectors and analog charge amplifier ASIC
- Created software libraries and tools in Python/LabView for characterizing radiation detectors and reporting experimental test results to scientists

Engineering Seismology Group (ESG) Solutions, Kingston, Ontario, Canada

Engineering Projects Manager, July 2009 to May 2010

- Provided engineering support for seismic data-acquisition projects, including interfacing with internal salespeople and external clients

Senior Electronics Designer, March 2008 to July 2009

- Designed and prototyped various rugged time synchronization electronic products for use in industrial applications and transferred designs to production
- Authored technical manuals, test procedures, and quality control documentation in an ISO 9001 quality environment

Hardware Designer, September 2004 to March 2008

- Schematic capture and circuit board layout of low-noise analog data acquisition products and sensors for mining and oil applications
- Traveled to domestic and international client sites to problem-solve and conduct the installation of sensors and supporting infrastructure

PROFESSIONAL DEVELOPMENT

Managing Projects – Three day course

Twenty Eighty Strategy Execution, Ottawa, ON, Canada (October 2017)

Developing Software for an ARM-based SoC – Two day course

Intel Programmable Solutions Group, Penticton, BC, Canada (November 2016)

Statistical Analysis using JMP 9 – Three day course

Predictum Training and Education, Victoria, BC, Canada (January 2012)

Texas Instruments OMAP ARM Processor Integration Workshop using Linux

Texas Instruments, Waltham, MA, USA (July 2009)

Heng Zhang

Office phone number: 1-250-4972352

Email: Heng.Zhang@nrc-cnrc.gc.ca

I am working as a digital design engineer at NRC Herzberg Institute of Astrophysics (NRC-HIA) in Penticton, where my responsibilities include high-speed PCB design, FPGA design, schematic capturing, testing and verification, signal integrity and timing analysis, design for manufacture and testability, design specification and documentation, project planning and budget forecasting. I have extensive experience with Mentor Graphics, Xilinx and Altera tool flows.

EMPLOYMENT

2002 – now National Research Council Canada Canada

Digital Design Engineer, Research Council Officer

I have been working on several projects since I jointed NRC in 2002. In EVLA project, I have successfully completed several PCB designs and FPGA designs. The PCB designs that I have finished for the EVLA projects are: Baseline Board, PC104 Monitor/Control Mezzanine Card (PCMC), Station Data Fanout Board (SDFB), Crossbar Board, Patch Board, Common Backplane, Rack Power Monitor/Control Interface Board (RPMIB), Correlator Chip Test Board and TimeCode Generator Board. Among these PCB designs, the Baseline Board is the most complex PCB. It is a 12Ux15.75inch board with 28 layers, double-sided high-speed PCB with BGAs on both sides. It has 183 BGA devices, 64 DDR SDRAMs, 32 DP-SRAMs, 96 1Gbps high-speed LVDS fanout buffers, 64 point-of-load switching regulators and 11 quarter-brick switching power supplies. It is designed with blind via and through-hole via technology, controlled impedance, both single-ended and differential high-speed traces with minimum trace width and space of 3.5mil. For the FPGA designs, I have completed PCMC FPGA, Station Board Timing FPGA, TimeCode Generator FPGA and 4 Baseline Board MCB/Configuration Fanout FPGAs designs. The PCMC FPGA is implemented as a PCI device. It is acting as a bridge between the PCI bus and local MCB bus. It is also in charge of configuring the FPGAs on the Baseline Boards/Station Boards and monitoring the temperatures/voltages on the Baseline Boards/Station Boards. All the PCB designs and FPGA designs have been successfully tested, installed and in operation at EVLA site. During the testing and verification phase of the EVLA project, I have successfully debugged and fixed about 20 Baseline Boards with manufacturing and component faults.

In the TMT adaptive optics Real-Time-Control (RTC) project, I successfully implemented Deformable Mirror (DM) fitting algorithm in Xilinx XC4VLX40-12FFG1148CS2 device. The sparse matrix and vector multiplications are implemented with Column-Wise multipliers. DM fitting process is implemented with 4 iterations of Conjugate Gradient algorithm. Both Column-Wise multipliers and 4 iterations of Conjugate Gradient implementations are successfully

developed, verified and tested with Station Board FPGAs. I also did an investigation and time analysis on tomography implementation of Block-Gauss-Seidel (BGS) with 20 iterations of Conjugate Gradient algorithm. From the investigation, the BGS-CG20 algorithm for the tomography process can be implemented on a single multi-function FPGA board with significant time improving (by factor of 2). The implementation of BGS-CG20 algorithm is expandable with more hardware as the RTC system grows.

In the Kermode project, I have successfully designed and tested the 8-FPGA High-Speed digital signal processing board. The Kermode board is in standard ATCA form factor. It contains 8 Virtex 6 LX35 FPGAs, 16 DDR3 SODIMM modules and 4 FMC cards. I am responsible of library parts creation, schematic capturing, PCB layout, pre-layout and post-layout simulations, generating manufacturing package, hardware/firmware test and verification, and design/manufacture documentations. This board contains 6.5Gbps transmission lines and DDR3 memory interfaces. The Kermode board has been used for the verification of DVA-1 antenna and the PAF beamforming applications.

I designed and tested the DVA-1 spectrometer for the DVA-1 antenna verification application. The DVA-1 spectrometer is a 2048-channel correlator with maximum 50MHz processing bandwidth. The sampled data from dish are correlated in the FPGA and the results are saved into the DDR3 memory. The host computer can read the results from the DDR3 memory through 1GbE link. Delay on the data samples can be adjusted with the FPGA internal block memory. The spectrometer is implemented with a single Xilinx Vritex 6 LX35 FPGA on the Kermode board. The DVA-1 spectrometer allows us to verify the performance of the DVA-1 antenna.

In the SKA1 CSP Mid.CBF project, I have designed 2 boards: the PowerMX motherboard and the TALON-DX board. The PowerMX motherboard is a High-Speed digital board that can host up to 4 processing daughter cards and 8 IO daughter cards. It provides the power, clocks and monitor/control functions to the daughter cards. The high-speed 26Gbps links are provided between the processing cards, and between the processing cards and the IO cards. I was responsible of design specification, PCB development, test and verification, and documentations. The 26Gbps links were fully verified and the performance meets the design specification.

The TALON-DX board is a single FPGA DSP board. It contains a single 64x26G SERDES Intel Stratix-10 SX HPS device P/N 1SX210HU2F50E2VG, as well as surrounding/supporting 4xDDR4 DIMM banks and 5xFCI LEAP Mid-Board Optical (MBO) modules. The FPGA device/package is pin-compatible across the range of the 1SX165 to the 1SX280. I have been leading the hardware development of the TALON-DX board. The 3 major challenges of this design are: 64 SERDES channels that operate at 26Gbps speed, 4 DDR4 DIMM modules that operate at 2400MT/s, and the high-current power distribution networks for the FPGA core voltage. To ensure the SERDES performance, 3D SI simulations are conducted for the 26Gbps SERDES channels. In order to achieve the 2400MT/s DDR4 performance, all DDR4 traces are length-matched within 2ps tolerance. Multiple copper layers are used for the FPGA core voltage distribution to ensure that the 0.85V power quality meets the FPGA requirements. The PCB design has been completed. The 2 prototype boards are fabricated and received. Right now we are conducting the prototype bring-up test. We have verified that all power rails, all clock signals are correct. We are able to program the FPGA successfully. In the meantime, I implemented the FPGA design to conduct the SERDES verification and the DDR4 verification. These tests will be performed through Intel System Console tool.

- High-speed digital design, signal integrity analysis, synchronization on circuit boards and between sub-systems, FPGA design and digital simulation.
- Circuit design and printed circuits incorporating the latest components, high-speed communication I/Os, memory interface and backplane architectures.
- Experience with development tools such as Mentor Graphics DesignView, ExpeditionPCB, SignalVision, ICX, HyperLynx, ModelSim, Xilinx ISE Design Suite and Altera Quartus II. Experience with high-speed design techniques, high-speed differential and single-ended routings, high-speed simulation, design for test, manufacture and diagnosis.
- Working knowledge of multi-rate digital signal processing, poly-phase FIR filtering and filter banks, complex digital signal mixing, correlation, decimation, interpolation, convolution and fast Fourier transforms.
- Demonstrated ability to communicate effectively through clear technical writing and presentations. For example, writing design specifications, test and verification plans, interface control documents, protocol specifications, manufacturing and assembly instructions, technical memorandums and presentations in EVLA project and TMT adaptive optics RTC project. Lately I wrote a memo for Tomography Implementation with BGS-CG20.
- Project planning, electronics components pricing and cost/schedule control.
- Demonstrated ability to interpret, analyze and capture project requirements. For example in EVLA project, successfully interpreted, analyzed and captured project requirements for the PCB and FPGA designs. In TMT adaptive optics RTC project, successfully interpreted, analyzed and captured project requirements for DM fitting implementation in Xilinx XC4VLX40-12FFG1148CS2 device.
- Responsible of complex, high-speed data processing system design
- High-Speed DSP algorithm, design, implementation and verification.
- HDL coding, functional simulation, FPGA placement and routing, static timing analysis, gate-level simulation. Familiar with Xilinx ISE Foundation/Altera Quartus II placement and routing tools, ModelSim simulation and verification.
- Schematic capturing and PCB layout design. Experience with high-speed, controlled-impedance, single-ended/differential trace design. Experience with 12U, 28-layer high-speed high density board designs. Familiar with Mentor Graphics Design Capturing and ExpeditionPCB tools.
- PCB board level simulation. Familiar with Mentor HyperLynx, Signal Vision and ICX simulation tools.
- Prototype testing and verification. Strong ability of problem solving, FPGA code optimization, and board level trouble-shooting.
- Design experience with Giga bit Ethernet, 10 Giga bit Ethernet interfaces, PCI bus and I2C bus.
- Familiar with test equipments such as: logic analyzer, digital oscilloscope, network analyzer, Signal generator, Spectral analyzer.

1997 – 2001 Aiwa Singapore Ltd. Singapore

Senior Electrical Engineer (Research and Development Department)

I was responsible of audio and video product designs from conception to mass production.

- Successfully designed 8 models within 4 years in Aiwa Singapore Ltd. with zero defects.
- As a main electrical engineer designed model LCX-133 which won Aiwa President Award in 2000.
- New project cost control, design schedule control, project planning and budget forecasting.
- Digital and analog circuit design, PLL/VCO, ADC/DAC, amplifier, signal conditioning, power supply designs, simulation and verification.
- Schematic capture, PCB layout design, high-speed simulations and verifications.
- RF designs for FM and AM receivers.
- Debugging and troubleshooting digital and analog circuits with test equipments.
- Electronics system testing such as: design verification, reliability test, temperature test, safety test based on UL or IEC standards, AC noise test, flicker test, ESD test and EMC test.
- Production engineering support, design documentations, manufacturing packages, assembly instructions and ECOs.
- Experience of microprocessor applications with C language.
- Familiar with MPEG1 and MPEG2 standards.

1991 – 1997 Anjing Science and Technology Company Tianjin, P.R. China

Electrical Engineer

I was responsible of electrical designs for industrial automation machines, control and monitor equipments such as: automatic packing machines, water treatment systems, car battery assembly lines, power station monitoring systems and electric motor auto-testing systems.

- Electrical control circuit designs, simulations and verifications.
- Schematic capturing, PCB designs and design documentations.
- Hydraulic and pneumatic systems design.
- Project planning and budget forecasting, schedule and cost control.
- Debugging and troubleshooting circuit boards with test equipments.
- System installation, testing and maintenance.
- PLC (Programmable Logic Controller) program developments, testing and verifications.
- Software development with C language.
- Maintenance and upgrading of the electrical control systems.
- Experience with power station and power transmission system maintenance (10KV).

EDUCATION

1987 – 1991 Shanghai Jiaotong University Shanghai, P.R. China

Degree of Engineering

Bachelor's degree, Electrical Engineering Department.

Excellent score on my final year project (designed a position detection sensor used on satellite).