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A SOLID-STATE RADIOMETER

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Work is now being done at NRAO that will lead to a completely solid-state standard receiver that will eventually replace the standard vacuum tube version now seeing wide use at the Observatory. So far, the work has progressed very well although relatively small effort has been applied in this direction, but a solid-state receiver is well within the realm of possibility. The major objective is to insure that the radiometer is noise limited instead of stability limited. As with any system development, some design constants should be chosen that are common to all components. The radiometer system consists of a number of sub systems, such as the gain modulator, intermediate frequency amplifier, audio amplifier, switch driver, and phase detector.

First, the selection of transistors becomes very important. Such factors as frequency cut-off, power dissipation, collector ratings, small signal current gain, and cost must be considered. On the basis of these considerations, the Philco 2N1742 MADT (micro alloy diffused-base transistor) was selected for all radio frequency circuits. The audio and phase detector circuits are not so demanding, and there are a number of transistors that can be used. The primary voltage to be used is of considerable practical importance. Since the 2N1742 collector rating is -20 V DC, a voltage of -18 volts was chosen. This voltage is slightly higher than was desired, because the transistor is very sensitive to over voltage. The -18 volts was selected because it is a multiple of 6 (used in digital circuits), and it is high enough to allow nominal power output without a heavy collector current. A voltage of 12 or 15 volts would be better if the 2N1742 was the only component using the primary power. A bandwidth of 80-100 megacycles, centered on 50 megacycles, is being attempted up to the diode detector. Since this is a post-amplifier, noise figure is of secondary importance, and no attempt will be made to keep the noise figure less than 7 or 8 db.

I. Switch Driver

A solid-state switch has been designed and tested that will deliver more than enough 400 cycle power to drive the entire receiver. In fact, it is intended that the 400 cycle unit will be capable of driving at least two standard receivers. The 400 cycle switch is simply a triggered multivibrator running at 400 cycles/sec. It is possible to construct a free running multivibrator, but the frequency stability is dependent on the R-C feedback

loop, and the free running unit tends to drift about ± 5 cycles. With a narrow 400 cycles filter in the audio circuit, this drift cannot be tolerated. Therefore, the synchronizing trigger seems advisable at this time. The multivibrator circuit is inherently very inefficient, because of the large feed-back power required to switch the opposite transistor on or off, as the case may be. There are two ways to achieve the desired power from the multivibrator. One way is to use large components and high power and use only a small portion of the dissipated power. This is a very inefficient method. The second method is to use small components and low power, and feed the vibrator output into a high impedance amplifier, and amplify the signal by conventional means. This method requires more components, but the circuit is more efficient. Another factor to consider with switch drivers is the possibility of operation at more than one frequency. For instance, the AIL maser system is switched at 20 cycles/second, whereas the standard receiver is switched at 400 cycles/second. If a monostable or bistable circuit is used, it can be triggered at any frequency from a fraction of a cycle/second to more than one megacycle. If an astable circuit is used, it will run at only the design frequency. In this system the bistable circuit was chosen. This circuit can be modified quickly to astable operation if the need should arise. The general circuit is shown in Figure 2.

The theory of operation is straightforward. The transistor Q_1 is used in the emitter follower configuration in order to present a high impedance to the reference source. In some cases the transistor may not be necessary, depending on the internal impedance of the reference oscillator. Transistors Q_1 and Q_2 are connected in the conventional bistable multivibrator circuit, using 2N242 transistors. This is a relatively inefficient circuit, and can be improved upon. The transistor Q_4 is used as a Class A power amplifier, capable of approximately 4 watts output power. Improvements in the circuit could be made by reducing the size of the transistors Q_2 and Q_3 in the multivibrator, thereby increasing circuit efficiency. This will be done in the finished circuit.

One problem not immediately seen is AC coupling at low frequencies (such as 20 cycles/second) and low impedance. A future project will be to design and test a hybrid circuit using analog and digital techniques, which should avoid the AC coupling difficulties.

II. Gain Modulator

The gain modulator designed for the solid-state receiver has been tested with positive results. This unit is the first RF circuit in the standard system, and uses 2N1742 transistors throughout (see Figure 3). Transistor Q_1 serves two purposes. First, it serves as a constant current source for the transistor switches, Q_1 and Q_2, and second, it provides a means of inserting the RF signal into the switches. Transistors Q_2 and Q_3 are emitter coupled, and transistor Q_1 is driven by the 400 cycles/second square wave alternately into saturation and to cut-off. Q_2 follows Q_1 exactly 180° out of phase. Therefore, the signal is effectively switched from one attenuator to another. These attenuators can be adjusted to provide radiometer balance. After the signal passes through the attenuators the two channels are recombined in a summing circuit and fed on to the intermediate amplifier. The problems encountered in the gain modulator have been limited to the attenuators, and to bandwidth. The attenuator problem has been of a physical nature; simply, the attenuators have been approximately 2 or 3 times as large as the remainder of the circuit. Some consideration has been given to this problem, and on the final configuration it will have been eliminated.

Since we are attempting to maintain a bandwidth of about 100 Mc/s through the system, the gain modulator must be capable of this bandwidth. The limiting factor now is the coupling transformers between the switching transistors and their associated attenuators. In the final design, the circuit will use the wide-band transmission line transformers. These transformers will be discussed more fully under the IF amplifier. The gain modulator as shown in Figure 3 has a 3 db bandwidth of 15 Mc/s, and co-channel separation of about 40 db. This can probably be improved by a different layout and better RF shielding. Also shown in Figure 3 is the DC biasing circuit, and the switch locking network, providing a method to lock the gain modulator in either the signal or comparison position. There are other means by which gain modulation can be accomplished, such as a voltage controlled stage in the IF strip, the gain changing in synchronization with a drive voltage. The radiometer would be balanced by changing the amplitude of the drive voltage. A system such as this, while theoretically possible, introduces a number of variables into the system that must be controlled very closely. As for now, the circuit of Figure 3 works well, and has been used in the prototype radiometers.

III. Intermediate Frequency Amplifier

The intermediate frequency (IF) amplifier in the solid-state receiver should have an overall gain of about 60 db, a bandwidth of about 100 Mc/s, and a power output of approximately 50 mw. Noise figure is not so important, and 7 or 8 db would be adequate. Figure 4 shows the preliminary design of the unit as built and tested in the laboratory. As in the gain modulator, the transmission line transformers are the deciding factor in gain and bandwidth. The transformers that have been built did not meet design specifications and, consequently, the IF amplifier did not approach the desired specifications. As shown in Figure 4, the gain was only about 15 db, and 3 db bandwidth was 40 Mc, with about 6 to 8 db ripple. These difficulties have been attributed to the transformer, and specifically to the toroid core material. Since the prototype circuit was built and tested, no further circuit design has been done. Further investigation has been made into the transmission line transformers, and we are now in the process of obtaining new core material to be used in the next bread-board prototype.

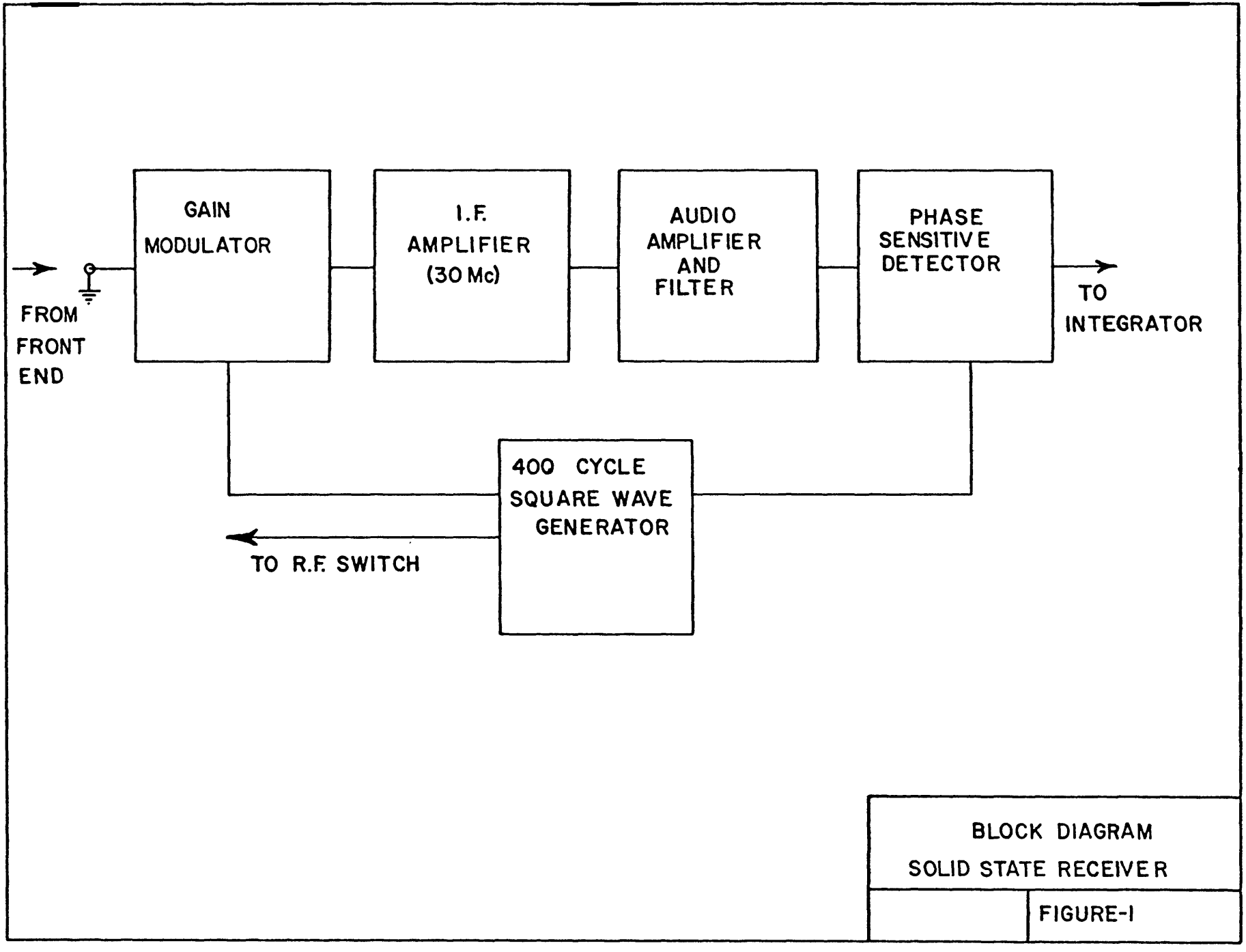
If the interstage transformers can be considered as ideal, the design is relatively simple and straightforward. Transistor Q_1 is used in the input impedance matching circuit, and in conjunction with resistor R_1 provides a nominal input impedance of 50 ohms. Capacitor Q_1 is used as a peaking capacitor for frequency adjustment. Resistor R_2 and transformer T_1 make up the interstage coupling network. R_2 is used for the same reason as capacitor C_1, to boost the high frequency response of the circuit. The following stages are identical up to the output stage which is designed as a power amplifier. Theoretically, the current gain per stage should be 6 db, obtained across the transformer. Practically, the gain that can be obtained is limited by the biasing circuit and stray L and C. Actual gain per stage approaches 5 db. There are minor adjustments that can be made to enhance frequency response, such as increasing bias current or adding a variable inductance in the transistor base lead. A new amplifier will be built in the near future using a new type of core material for the toroidal transformers. In the bread-board test set-up, a commercial IF amplifier was used. The bandwidth of this amplifier was approximately 90 Mc/s.

IV. Narrow Band Audio Amplifier

The 400 cycle signal from the detector must be filtered and amplified. This is accomplished by the circuit configuration as shown in Figure 5. Any good quality audio transistor can be used, and the circuit constants can be adjusted accordingly. The circuit as shown will deliver about 20 db gain, but it is a simple matter to add stages to increase this figure. The circuit is a narrow bandwidth, twin-tee feed-back amplifier, tuned to the switch frequency of 400 cycles per second. The transistors are used as straight cascaded audio amplifiers, and the bandpass characteristics are determined by the twin tee feed-back loop. The theory of operation is simply this: The twin-tee presents a low impedance to all frequencies except 400 cycles, and thus gives almost 100 percent feed-back. The remaining amplifier signal is the 400 cycle sine wave that is desired. By this means, the low power 400 cycle square wave signal is converted to a higher power sine wave signal that maintains phase relation with the 400 cycle driving signal, and the phase detector is protected from overload by noise on the 400 cycle signal.

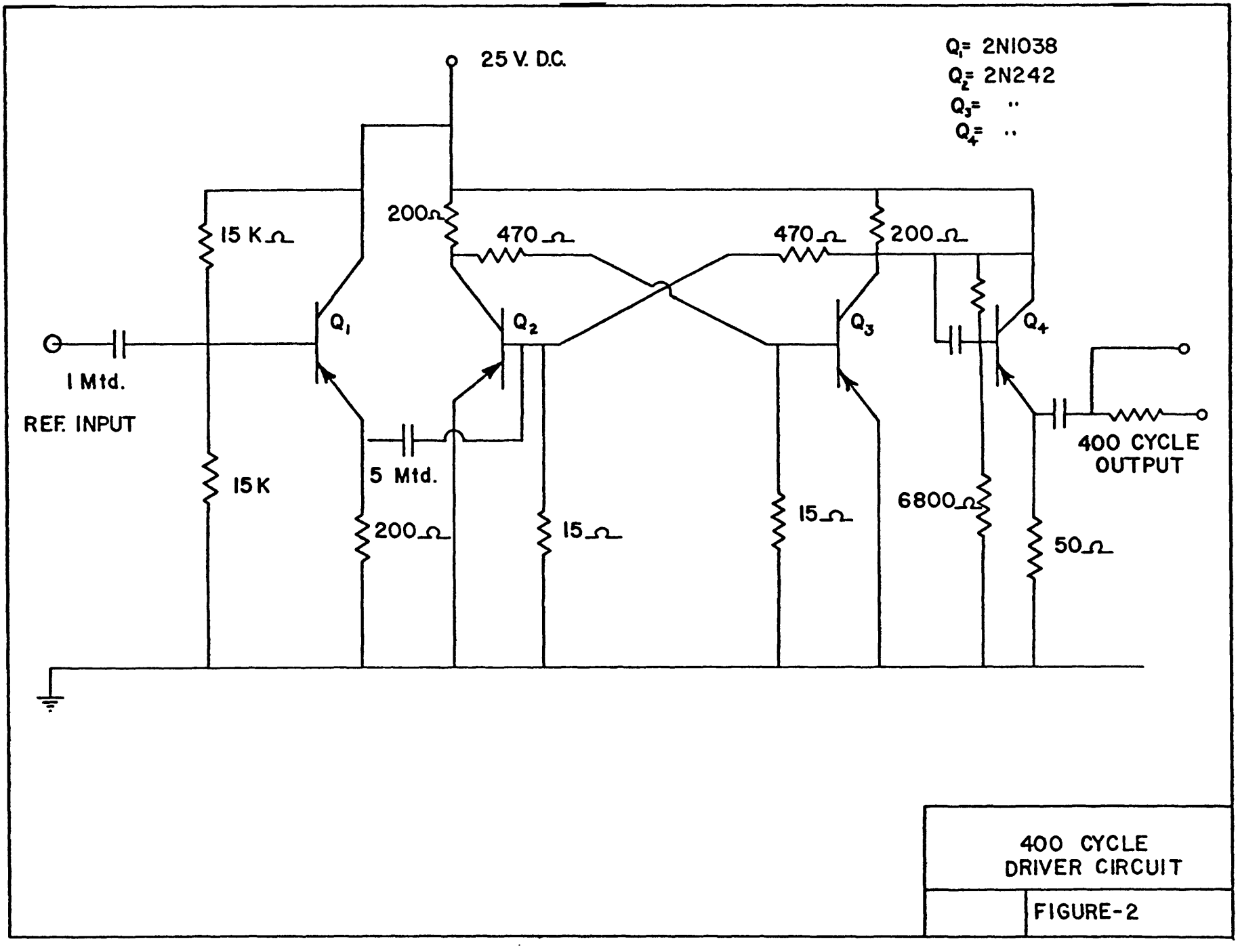
V. Phase Sensitive Detector

In order to separate the desired signal from the undesired random signal, some sort of phase sensitive device is required. The circuit used in the prototype receiver is shown in Figure 6. Circuit operation is as follows: The 400 cycle signal is introduced by means of transformer T_1. Q_1 and Q_2 are solid-state choppers built specifically to obtain low offset voltage. The offset voltage from the integrated choppers is extremely low, usually less than 50 μV. These solid-state devices are used in this case as switches, driven alternately on and off by the 400 cycle switching signal. The result is a simple, effective phase sensitive detector. The output signal can be used directly, or if the level is too low, it can be amplified by means of a DC amplifier. From this point on, the signal can be handled by digital means. Physical size is secondary in most cases but it is worth noting that a system built along these lines would occupy about 30 inches of standard 19-inch panel. Since the transistor is a low power device, heat problems would be minimized and thermal instability would be less than that for vacuum tubes. The transistor is also insensitive to microphonics. Although the standard tube receiver has shown good results, it is believed that the solid-state receiver will eventually make the tube version obsolete.



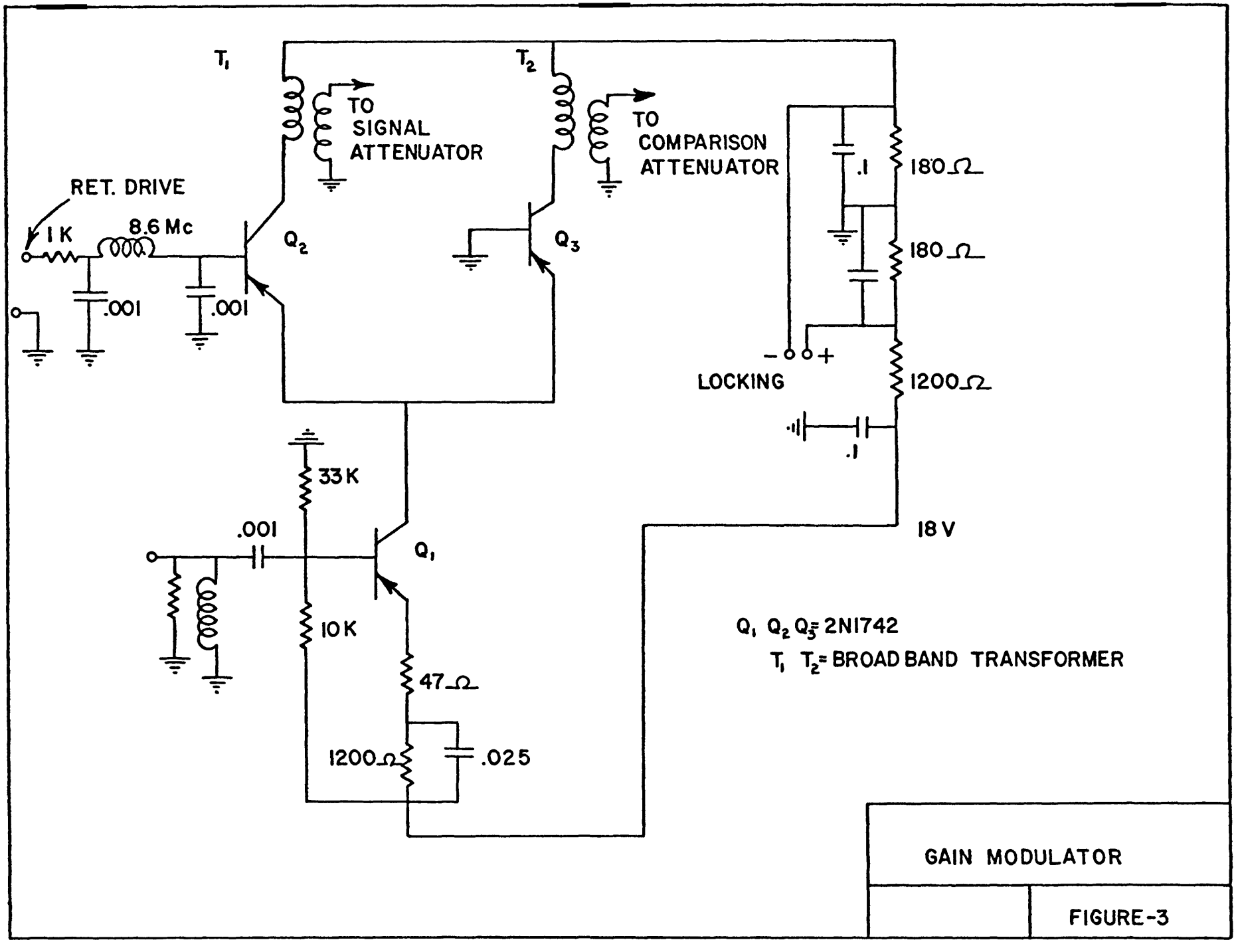
BLOCK DIAGRAM
SOLID STATE RECEIVER

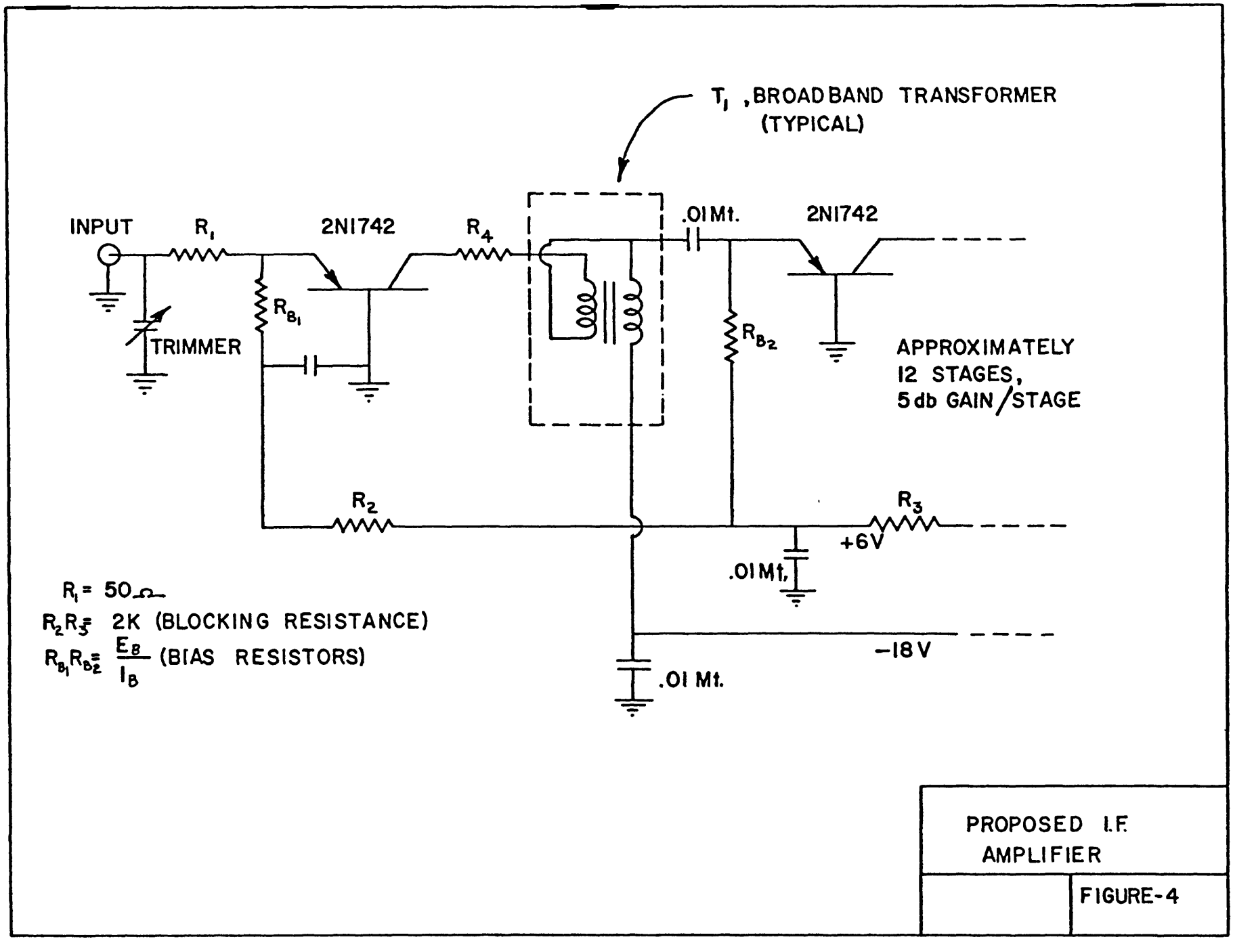
FIGURE-1

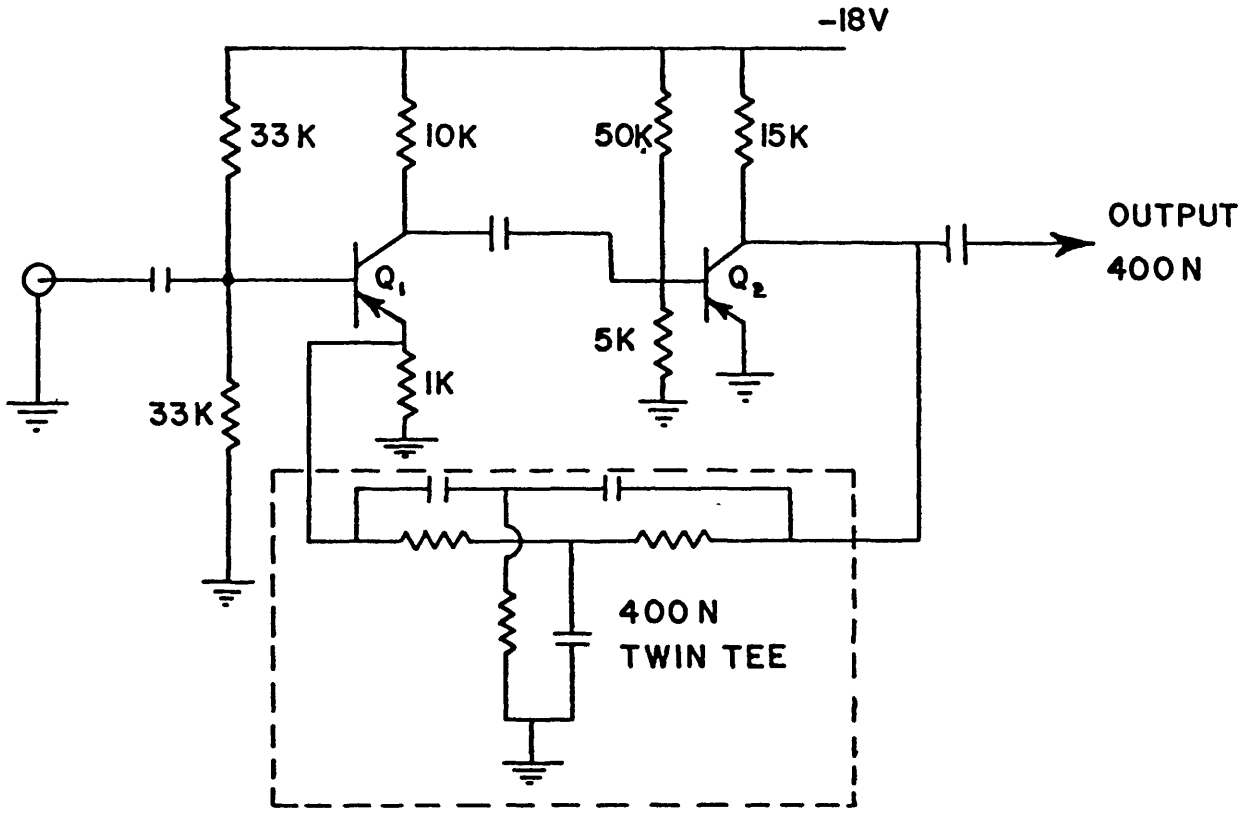


400 CYCLE
DRIVER CIRCUIT

FIGURE-2


T1
T2
TO SIGNAL ATTENUATOR
TO COMPARISON ATTENUATOR
RET. DRIVE
1K
8.6 Mc
Q2
Q3
.001
.001
.1
180Ω
180Ω
LOCKING
1200Ω
.1
18 V
33K
.001
Q1
10K
47Ω
1200Ω
.025
Q1 Q2 Q3 = 2N1742
T1 T2 = BROAD BAND TRANSFORMER
GAIN MODULATOR
FIGURE-3

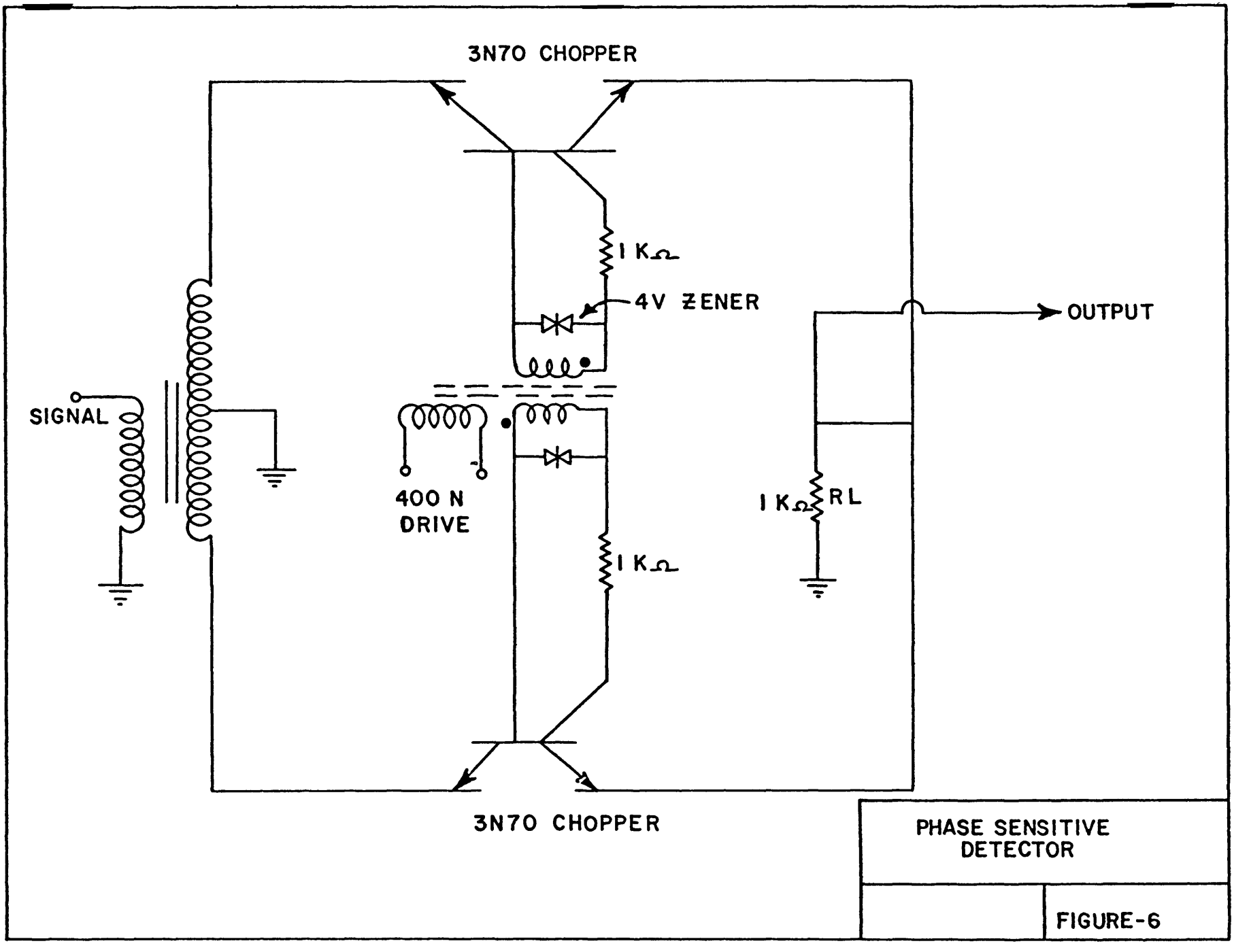

T1 , BROADBAND TRANSFORMER
(TYPICAL)
INPUT
R1
2N1742
R4
.01Mf.
2N1742
TRIMMER
RB1
RB2
APPROXIMATELY
12 STAGES,
5db GAIN/STAGE
R2
R3
+6V
.01Mf.
-18V
.01 Mf.
R1 = 50Ω
R2R3 = 2K (BLOCKING RESISTANCE)
RB1RB2 = EB/IB (BIAS RESISTORS)
PROPOSED I.F.
AMPLIFIER
FIGURE-4



Q_1, Q_2= 2N223 or EQUIVALENT

NARROW BAND
AUDIO AMPLIFIER

FIGURE-5



PHASE SENSITIVE DETECTOR

FIGURE-6