NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

Electronics Division Internal Report No. 66

VLB CONTROL II

Claude C. Bare

DECEMBER 1967

NUMBER OF COPIES: 100

VLB CONTROL II

Claude C. Bare

General:

The VLB (digital) Control (unit) II performs the following functions:

(1) Time Keeping — The 5 MHz signal from the atomic frequency standard is divided down to 20-second intervals. It is also capable of changing an atomic frequency input to UTC time.

(2) TM12211 Control — The control signals necessary for the operation of the TM12211 Ampex tape unit are provided. Parity error signals from the tape unit are stored and each track playback signal is available for scope viewing.

(3) Sample Clock — The 5 MHz clock is divided by 6 17/18 to provide the 720 kHz sample rate.

(4) Assemble Data — Six samples along with parity are assembled into a character for writing on tape in a computer-compatible format.

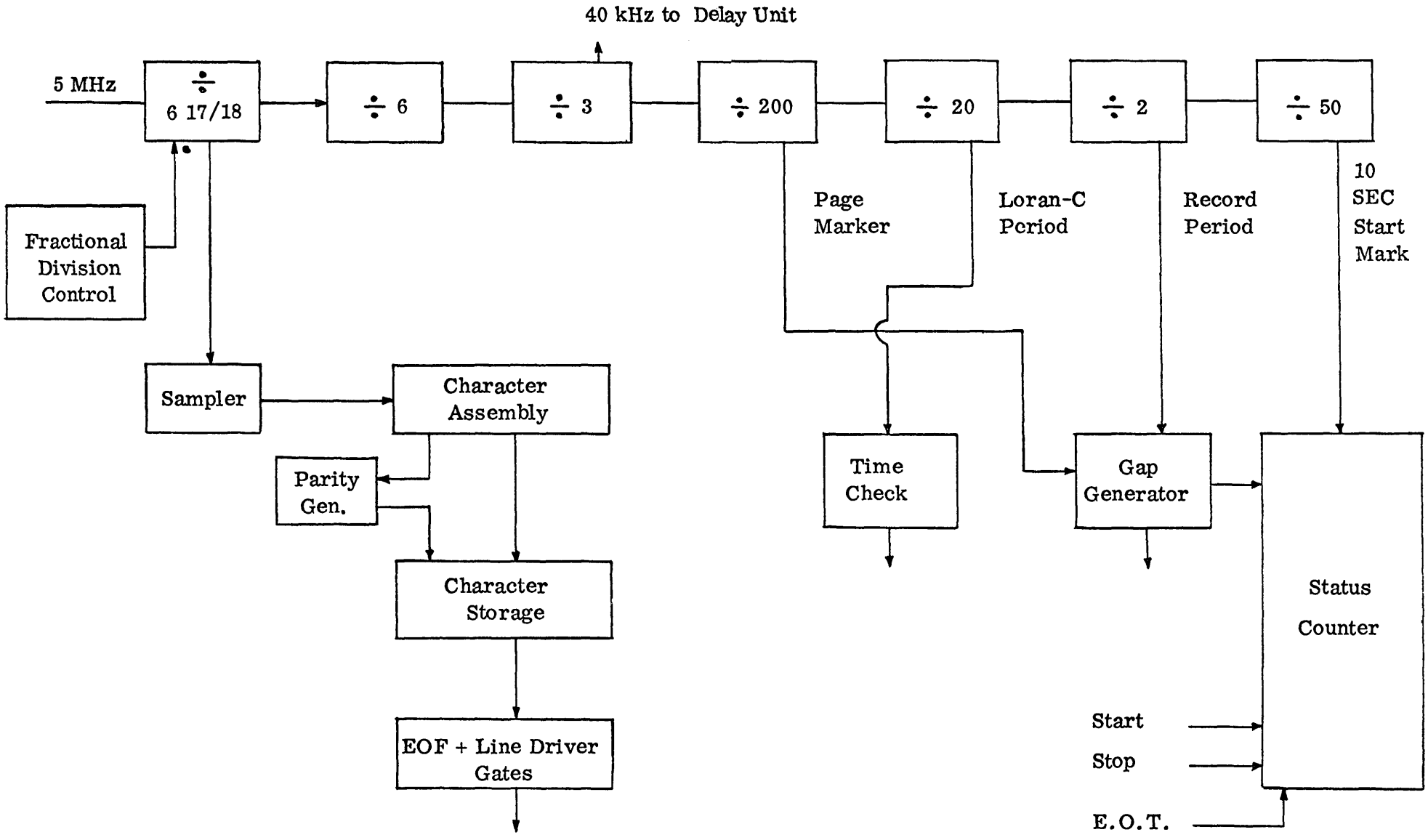
Block Diagram:

A block diagram is shown on the next page to aid in the following discussion of the VLB Control. The general layout of the block diagram is the same as drawing DS-3275.

Logic:

The VLB Control Logic is shown in DS-3275. A reduced copy is included as a fold-out page at the end of this report.

The 5 MHz input signal is converted to a near square wave by a circuit on a special card. A schematic of the circuit is shown on DS-3280, a reduced copy of which is included at the end of the report.



VLB CONTROL

BLOCK DIAGRAM

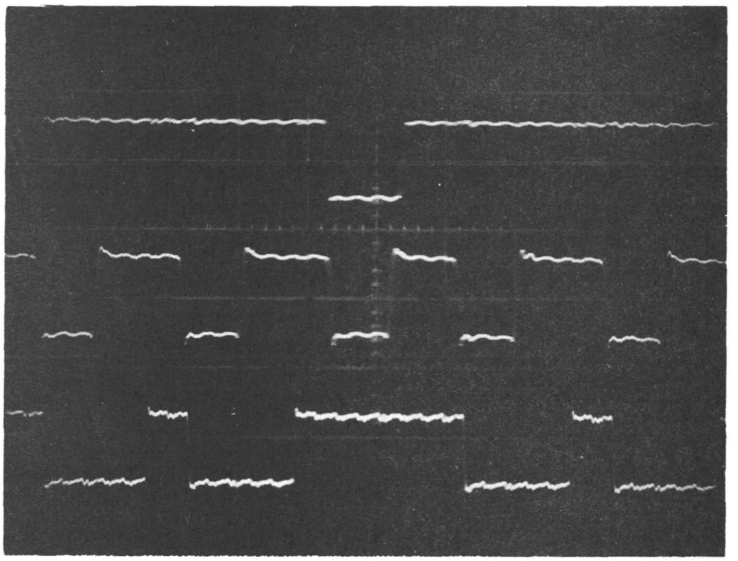
The 5 MHz (TP1) square wave is divided by 6 17/19 to provide 720 kHz in the fractional division logic. This 720 kHz signal provides the Sample and Shift clock (P1, TP5) for the incoming data from the clipper. Pictures showing relative timing of fractional division signals (F3, F4, and P1) are reproduced on the next page. F10, F11, and F12 divide by 6 and F3 (TP2) causes a pulse to be lost 17 out of 18 times. The signal F31A triggers F4 (TP3) which inhibits dropping of a pulse by F3 every 18th cycle. The atomic to UTC Control Logic causes the divider to divide by 7 instead of 6 three extra times every 20 seconds. This slows the time-keeping and sampling process by 300 parts in 10^{10}. The wire from 4-30 to 6-30 must be removed if a UTC standard oscillator is used.

The 720 kHz signal is divided by 6 to provide STORE and WRITE clocks called B1A and WRITE STROBE. The dividers also provide a 200 Hz signal called a page marker. This period of the page marker specifies the inter-record-gap (P3, TP7) length of 5 milliseconds. A 5 Hz signal (F71) triggers the gap five times per second. Every second 39 pages with 600 characters per page are recorded.

The Loran-C timing logic uses a 10 Hz signal to provide the pattern rate. The 10 Hz signal triggers a delay-multi which gates 8 cycles of 1 kHz to the scope sync driver to generate the LCR sync signal. The dividers also provide the 1/20 Hz for status control and 1/10 and 1/20 Hz for atomic to UTC time conversion.

The STATUS COUNTER is the control center of the VLB digital system. The following table explains the sequence of operations:

Input	F5	F6	F7	F8	Status
	0	0	0	0	Stopped
Start Switch					
	1	0	0	0	Wait
10 SEC (F104)					
	1	1	0	0	
Begin Gap (P3A)					
	1	1	1	0	Tape accelerating and recording one record or 30 inches of blank tape.
Begin Gap (P3A)					
	1	1	1	1	Recording data (inhibited during gaps).
Stop or EOT					
	0	1	1	1	Recording data (inhibited during gaps).
Begin Gap (P3A)					
	0	0	1	1	EOF
Begin Gap (P3A)					
	0	0	0	1	Stopped
Begin Gap (P3A)					
	0	0	0	0	Stopped

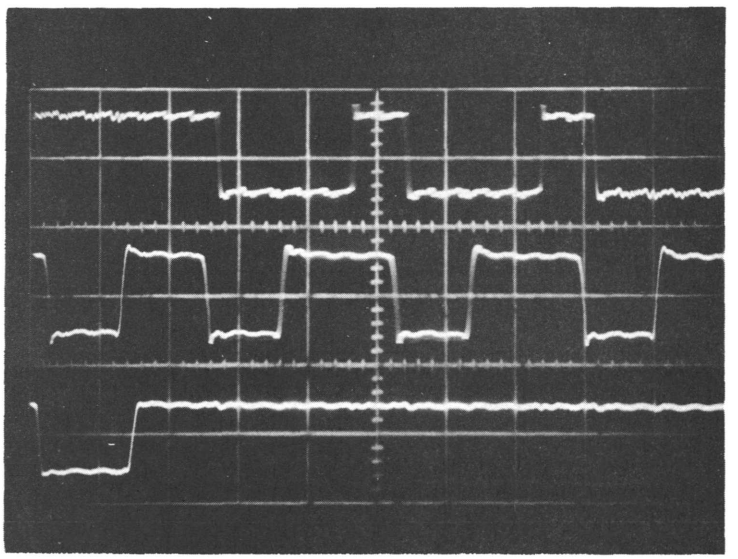


F4 (TP3)

P1 (TP5)

F3 (TP2)

≈ 0.7 μsec/cm



F3 (TP2)

P1 (TP5)

F4 (TP3)

0.5 μsec/cm

FRACTIONAL DIVISION WAVEFORMS

The tape drive starts only after the correct signals in the proper sequence. The RUN signal to the tape drive goes true ≈ 105 milliseconds after 10 SEC (F104) goes false (positive) or after the 10 second scope sync goes true (negative).

The data from the BACK END goes to the CLIPPER via a test switch. The switch provides test signals for recording all ONES, all ZEROS and a pattern of three characters of ONES and three characters of ZEROS (some tracks may record 4 and 2 or 2 and 4). The clipper is composed of two stages of current switching amplifiers and a grounded emitter output stage. The gain through the clipper is approximately 60 dB. The rise time is much less than the sample interval of 1.2 microseconds. The clipper is shown in S2.500.1 (see end of report).

An adjustment is provided to balance the clipper input circuit. The pot is moved to obtain approximately an equal number of ONES and ZEROS at the sampler output (TP6). This adjustment can be done most accurately with only a small signal into the clipper.

The clipper drives the control inputs to the sampler. The sampler can change states only at clock times. The synchronous output of the sampler drives the Character Assembly register and the Parity Generator. The data is shifted to the character storage register and is gated to the tape unit except when writing the End Of File character. Data continues to be sent to the tape unit during the inter-record gaps but the WRITE STROBE is inhibited during the gap. A WRITE-RESET is generated 25 microseconds after the gap begins to reset the write flip-flops. This operation produces on tape the character called LONGITUDINAL PARITY.

Vertical parity is checked in the tape unit read circuits. The parity error information is stored in a flip-flop (F19) which drives an indicator light. Since the longitudinal parity character has incorrect (even) vertical parity, the parity check circuits are inhibited during the time this character is read.

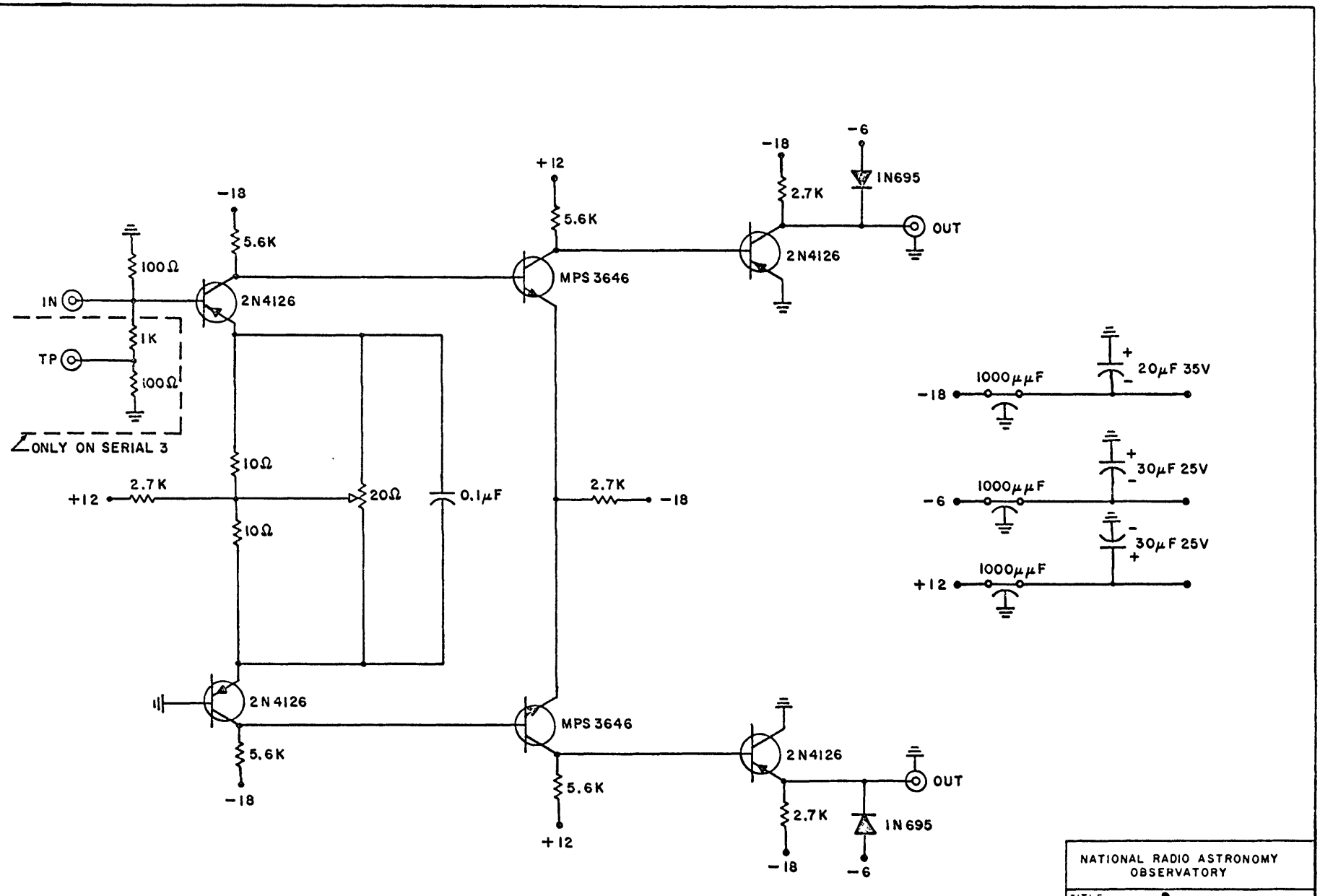
Timing:

- The operation of the VLB not only requires stable oscillators but also accurately known starting time of the two systems. Of course, the ultimate question is: When was the first bit that was recorded on tape sampled? This exact question can be replaced by a question that is easier to answer when only NRAO

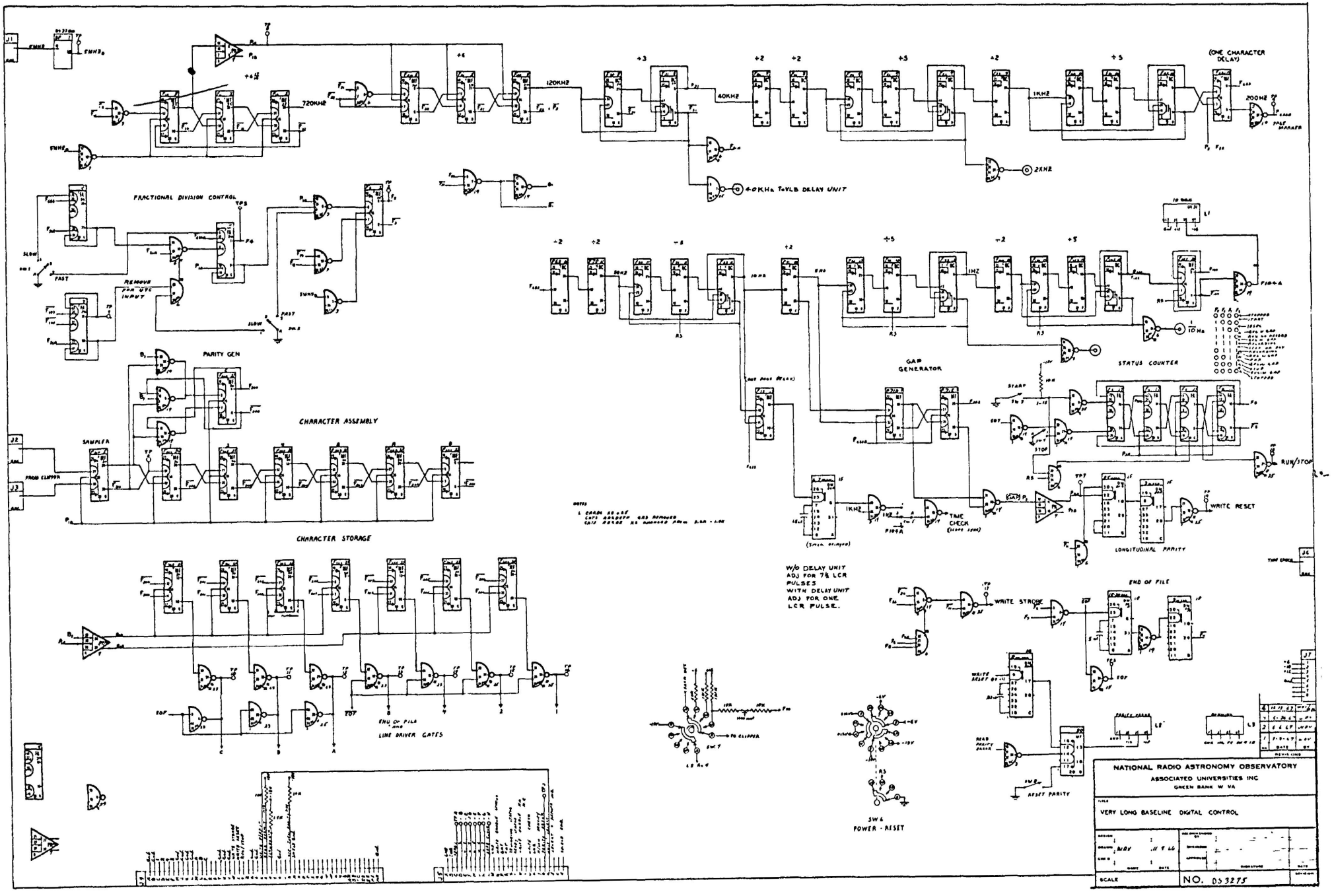
designed VLB equipment is used. With the VLB equipment, is it sufficient to measure the difference between some periodic VLB timing signal and UTC at each site? In the past this timing signal has been LCR. With the addition of a portable clock to our equipment, I recommend that the 1 Hz ($\overline{0.8\ SEC}$) signal be used. The $\overline{0.8\ SEC}$ signal precedes LCR by 5,490 microseconds.

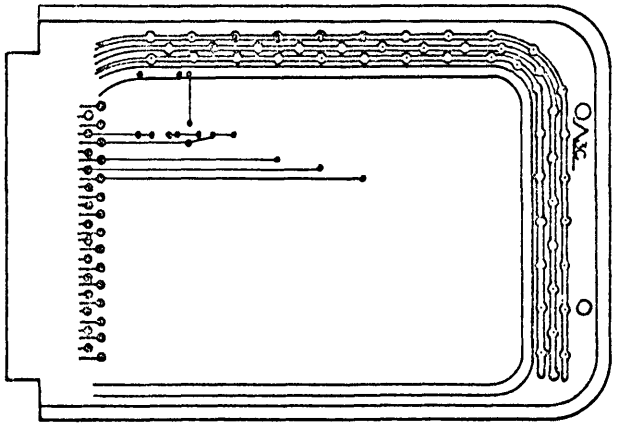
The VLB Control is synchronized by first resetting the dividers with the power switch reset. The switch is then moved to ON as the tone return on WWV or some other UTC minute mark. Sync the scope on the negative edge of the $\overline{0.8\ SEC}$ signal. Move the time of the sync signal with the fast and slow switches (located behind the hinged front panel) to place the WWV tick within 20 millisec after the $\overline{0.8\ SEC}$ sync signal. With the one second output from the portable clock on the scope, move the sync time with the fast and slow switches to bring the negative edge of $\overline{0.8\ SEC}$ within a convenient amount of the portable clock tick. This difference along with the predicted portable clock error provides the estimated offset from UTC. Check again to insure that an error of one or more seconds has not been made. The TONE RETURNS as the 10 SEC light extinguishes.

The synchronization with Loran-C will be discussed in another report concerning the VLB Delay Unit.

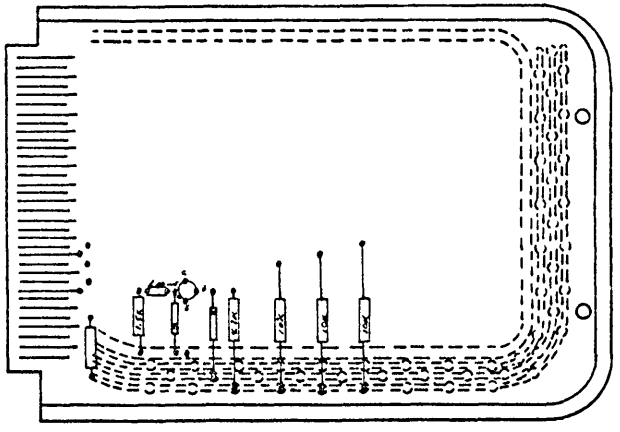


NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: VLB CLIPPER	
DSGN BY C. BARE	DATE: 12-13-67
APPD. BY:	DR. BY A.J. MIANO
DWG. NO S 2-500-1	

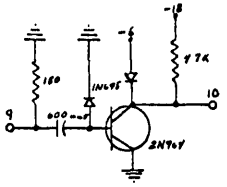

FRACTIONAL DIVISION CONTROL
PARITY GEN
CHARACTER ASSEMBLY
SAMPLER
CHARACTER STORAGE
LINE DRIVER GATES
GAP GENERATOR
STATUS COUNTER
TIME CHECK
LONGITUDINAL PARITY
WRITE RESET
WRITE STROBE
END OF FILE
RUN/STOP
W/O DELAY UNIT ADJ FOR 7½ LCR PULSES
WITH DELAY UNIT ADJ FOR ONE LCR PULSE.
SW6
POWER - RESET
NATIONAL RADIO ASTRONOMY OBSERVATORY
ASSOCIATED UNIVERSITIES INC
GREEN BANK W VA
VERY LONG BASELINE DIGITAL CONTROL
NO. 053275

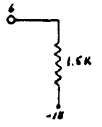


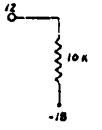
TOP

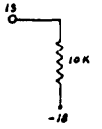


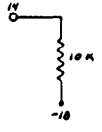
BOTTOM











NO.	DATE	BY
REVISIONS		

NATIONAL RADIO ASTRONOMY OBSERVATORY
ASSOCIATED UNIVERSITIES INC.
GREEN BANK, W. VA.

TITLE

V. L.B. DIGITAL CONTROL

BUFFER CARD

DESIGN			RECOMMENDED BY		
DRAWN	W.B.K.	11-11-66	ENGINEER		
CHK'D			APPROVED		
	NAME	DATE		SIGNATURE	DATE
SCALE			NO. 053280		REVISION