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THE 108-CHANNEL MULTIPLEXER FOR USE WITH THE HONEYWELL 316 SPECTRAL LINE PROCESSOR

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1.0 Introduction

This report describes the interface between the existing filter receivers and the Honeywell 316 computer as used in the recently developed spectral line processor for use at the 36-foot telescope.

The interface may accommodate up to 108 inputs. These will usually be two filter receivers (probably a 40-channel and a 50-channel or two 50-channels). Eight spare data channels are provided and are accessible via isolated BNC connectors.

Each channel consists of an input buffer amplifier, an integrator, and a switch. After a specific integration period the outputs of the channels are sequentially converted to a 12-bit binary number and read into the computer.

A reference generator provides timing signals to the multiplexer and computer, and provides LO or front-end switching signals.

2.0 Mode of Operation

The operating waveforms and block diagram of the multiplexer are shown in Figure 1.

The reference generator provides a 1 μs pulse every 50 ms. Previous to this pulse the integrators have been in the "hold" mode, storing the information from the last integration period which is approximately 46 ms.

The 1 μs pulse does three things: (1) sets the 7-bit address counter to channel zero, (2) triggers a 2 ms one shot that controls the readout cycle, and (3) initiates a conversion on the A/D converter. The result of this first conversion is meaningless and is discarded by the computer.

When the conversion is complete the A/D converter gives a "status ready" signal which results in (1) advancing the 7-bit address counter to channel 1 and (2) generating a DROPN pulse to the 316. On receipt of the DROPN pulse the computer reads the A/D output and when the read-in is complete the 316 generates a CHRDY pulse which initiates conversion of channel 1. When the conversion is complete the "status ready" output of the A/D converter advances the counter to channel 2. This sequence continues until all 108 channels are read. The time needed to readout all channels is less than the 2 ms set by the readout one shot.

At the end of the 2 ms period a 1 ms one shot resets all the integrators to zero. The end of the 1 ms period initiates a one shot with a period of approximately 46 ms which controls the integrate/hold cycle of the integrators. At the end of the 46 ms period the integrators go into the "hold" mode and at the next signal/reference transition the readout sequence is begun once again.

The length of the integration period is adjustable by a pot on card 16.

3.0 Description of Multiplexer

3.1 Card Locations — See page 3.

3.2 Power Supplies

The power requirements for the various circuits in the multiplexer are as follows:

1) Multiplexer Cards — +15 V + 2.8 V
-15 V +10 V

These voltages are derived from the +22 V and -22 V outputs of the Redcor power supply, model 103348, via card 1 (Figure 2). This card uses a SG3501 dual ± 15 integrated circuit voltage regulator and two simple operational amplifier circuits to generate the necessary voltages.

2) A/D Converter

The A/D converter requires a precision ± 10 V supply and a normal +5 V. The ± 10 V is generated directly on the A/D card by a small precision power supply supplied from the ± 22 V and the +5 V comes directly from the Redcor model 103348.

3) Logic Circuits

The logic circuitry is provided with +5 V from a standard Analog Devices power supply.

4) Bulb Circuits

To avoid ground problems and current spikes through bulb switching, a separate +5 V power supply is used for the bulb circuits and their associated drivers.

3.1 Printed Circuit Board Locations

Numbered from right, looking at front panel:

1	Power Supply Board	1	2	3	4	5	6	7	8	9	10
2	Integrate + Multiplex Channels	1	12	23	34	45	56	67	78	89	100
3	" " "	2	13	24	35	46	57	68	79	90	101
4	" " "	3	14	25	36	47	58	69	80	91	102
5	" " "	4	15	26	37	48	59	70	81	92	103
6	" " "	5	16	27	38	49	60	71	82	93	104
7	" " "	6	17	28	39	50	61	72	83	94	105
8	" " "	7	18	29	40	51	62	73	84	95	106
9	" " "	8	19	30	41	52	63	74	85	96	107
10	" " "	9	20	31	42	53	64	75	86	97	108
11	" " "	10	21	32	43	54	65	76	87	98	Spare
12	" " "	11	22	33	44	55	66	77	88	99	Spare

13 Decoder Board Channels 0-39 (0 not used)
14 " " " 40-79
15 " " " 80-119 (only 80-108 used)
16 Counter and Waveform Generator
17 A/D Converter
18 A/D Buffer
19 Line Receiver + Line Driver
20 Bulb Driver

3.3 Integrator and Multiplexer Card

Each integrator and multiplexer card has 10 channels. One channel is shown in Figure 3. The input amplifier is differentially connected to give good, common-mode rejection. The output of this first amplifier is fed to the integrator via a 2N4393 FET switch which serves as the sample/hold element. The integrator has an RC of 50 ms; the operational amplifier used has a sufficiently low input current to insure negligible error buildup during the hold part of the cycle. The integrator is reset by discharging the 0.1 μF capacitor through a 390 Ω resistor using a 2N4393 FET.

The output of each channel is switched into the A/D buffer via an FET switch. To make the unit compact we used the Siliconix G115BK and G123BK which have 6 and 4 FET switches per chip. To convert the 0, +5 V logic levels from the decoders to suitable levels for driving the FET switches, G125BK level shifters are used. Each chip has 6 level shifters and two chips per card are used, ten level shifters for the ten channels, the other two for the reset and sample/hold FET's. Data sheets on all these components are given at the end of the report.

The offset of each channel has been trimmed by adjusting the offset adjust of the input amplifier to give a total offset of less than $\pm$ 10 mV.

3.4 Counter and Waveform Generator (Figure 6)

This circuit is fairly self-explanatory. Extensive use is made of the N8162A, an integrated circuit monostable, to generate the various pulses. Two DM 8563 binary counters are combined to make the 7-bit counter. The hold/integrate one shot circuit was made from discrete components as a short recovery time is required. This is obtained by charging the 2 μF capacitor via an emitter/follower.

Outputs from the 7-bit counter are displayed on the front panel and a facility is provided for manual sequencing.

Two octal decoders are situated on this board. The rest of the decoding is done with three decoder boards in card positions 13-15.

3.5 Buffer Card

The outputs from the 11 integrate/multiplex cards are summed together in the A/D buffer card (Figure 8, card 18). The gain of the amplifier (nominally unity) may be increased by the addition of the usual resistors. Offset is provided to insure that the voltage supplied to the A/D converter is always positive.

3.6 A/D Converter Card

This card consists of a precision power supply, an analog module, a digital module, and 12 line drivers. The line drivers were added to the board in anticipation of driving the circuitry in the 316 computer with a differential output. This proved to be not possible for various reasons, so we converted the line driver outputs to single ended with an adjacent circuit card using line receivers.

3.7 Bulb Driver Card

This card accepts the outputs from the A/D converter card and the counter card to drive indicator bulbs on the front panel. These bulbs display the counter address and the A/D converter output.

4.0 Interface with 316

The interface with the 316 consists of the following connections:

1) 12 data lines
2) CHRDY line
3) DROPN line

} from multiplexer

4) 5 ms clock
5) Signal/reference edge

} from reference generator

6) Calibration signal
7) Zero check
8) Sonar alert (signifies beginning and end of integration period)

} to reference generator from 316

To generate interrupt signals within the computer from the 5 ms clock and the signal/reference edge, the circuitry in locations E34, E35, and E36 was added as shown in Figure 10. Connection is made to the multiplexer from the 316 via one cable with the following connections:

E34	Computer	Function	Multiplexer ELCO
	01		Gnd
	02	CHRDY	W
	03		Gnd
	04	Bit 1	A
	05	Bit 2	C
	06		Gnd
	07		Gnd
	08	Bit 3	E
	09	Bit 4	J
	10		Open
	11		Open
	12	Bit 5	
	13	Bit 6	
	14		Open
	15		Open
	16	Bit 7	
	17	Bit 8	
	18		Open
	19		Open
	20	Bit 9	k
	21	Bit 10	m
	22		Open
	23	DROPN	Y
	24	Bit 11	a
	25	Bit 12	C
	26		Open
	27		Open
	28		Gnd
	29		Gnd
	30		Open
	31		Open
	32		Gnd

Connection to the reference generator from the 316 is made via one cable with the following connections:

E38	Computer	Function	Reference Gen. ELCO
	01	5 ms clock	E
	02	Cal	C
	03	S/R edge	H
	04	Zero check	M
	05	S/R square wave	E
	06	Sonalert	A
	08	Spare	S

5.0 Reference Generator

A block diagram of the reference generator is shown in Figure 11. A 5 ms sidereal clock is provided to the computer by dividing down a crystal oscillator. A further divide by ten gives the 50 ms pulses needed for the internal sync mode. These 50 ms pulses provide a sync signal to the multiplexer and also supply the frequency divide unit. The output of the frequency divide unit gives a signal/reference square wave to the computer and, after level shifting, also supplies the LO or front-end switch, etc. The reference generator may be synchronized to an external 10 Hz signal.

The reference generator also accepts the cal and zero check from the computer and level converts them to 3C logic levels.

A circuit diagram of the reference generator is shown in Figure 12.

INDUSTRIAL SERIES
to +85°C

6.0 Component Data Sheets

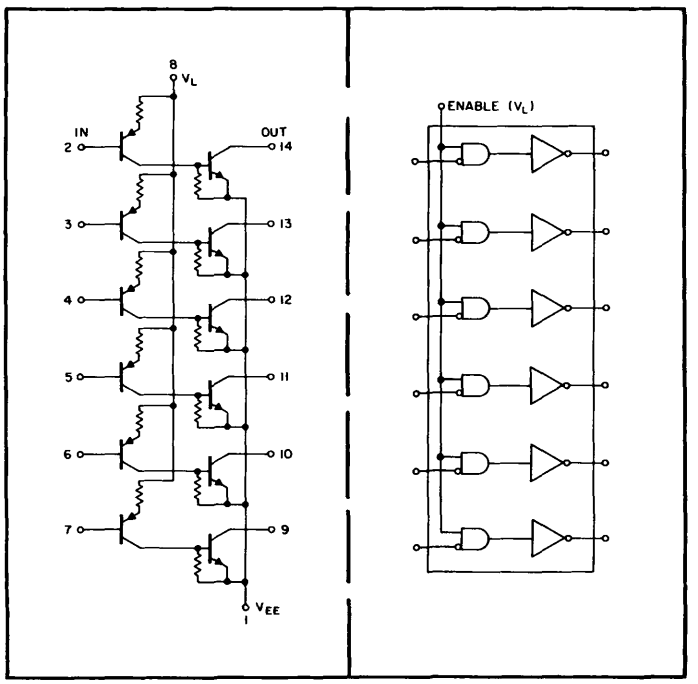
6-CHANNEL FET-SWITCH DRIVERS

D125BK

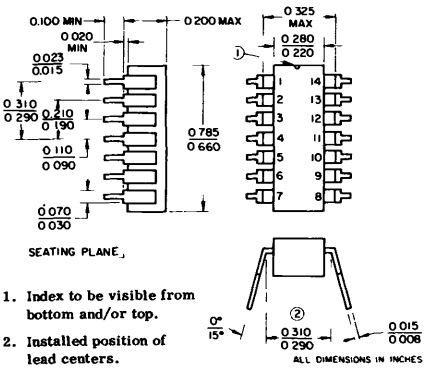
Siliconix incorporated

MONOLITHIC INTEGRATED CIRCUITS FOR DRIVING FET ANALOG SWITCHES

- Performs amplification and d-c level shifting required between low-level logic and MOS or junction FET switches
- Direct interface with TTL, DTL and RTL (V_L = 2.8 V)
- External pull-up elements required
- Compatible with G115 and G123 series multichannel MOS FET switches which include current-limiter pull-up FETs



MECHANICAL DATA



TO-116 Ceramic DIP
Tin Plated Kovar Leads

PRODUCT CONDITIONING

Units receive the following processing before final electrical test.

Temperature Cycle
-65 to +150°C, 5 Cycles

Hermeticity
Fluorocarbon Gross Leak, 100%
Helium Fine Leak, 2% AQL

ABSOLUTE MAXIMUM RATINGS

V_{IN} - V_{EE} ..... 30 V
V_O - V_{EE} ..... 36 V
V_L - V_{EE} ..... 30 V
V_{IN} - V_L ..... ±6 V
Maximum Dissipation ..... 500 mW
Current (Any Terminal) ..... 30 mA
Storage Temperature ... -65 to +150°C
Operating Temperature .. -20 to +85°C

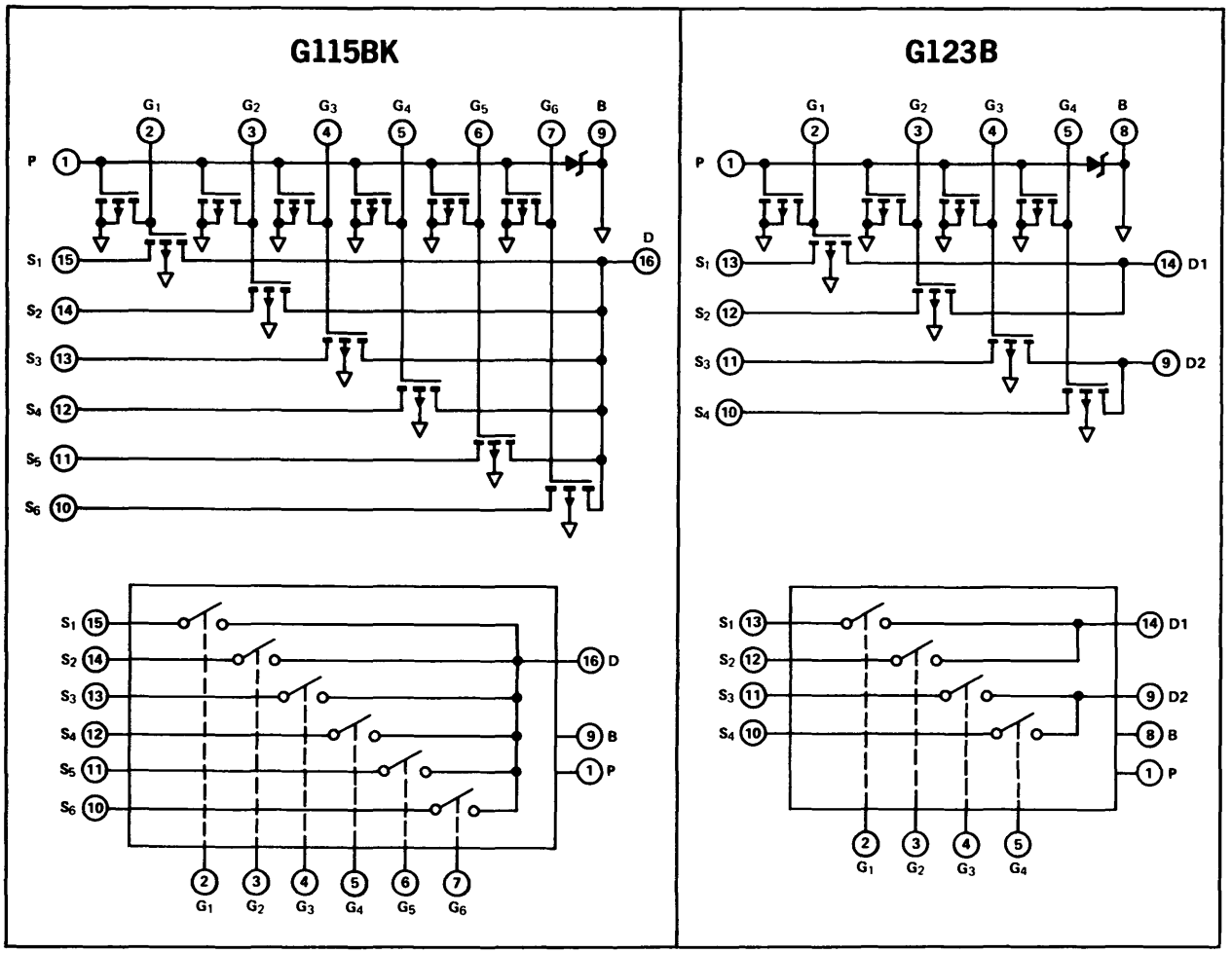
INDUSTRIAL SERIES
-20 TO 85°C

4 AND 6-CHANNEL ENHANCEMENT TYPE MOS FET SWITCHES

6.0 Component Data Sheets (cont.)

P-CHANNEL NORMALLY-OFF, TYPE C MOS FETS FOR SWITCHING APPLICATIONS

- Integrated FET current limiter pull-up elements supply collector current to buffer/drivers
- Integrated Zener-clamp gate protection
- Interface directly with D125B and D129B drivers



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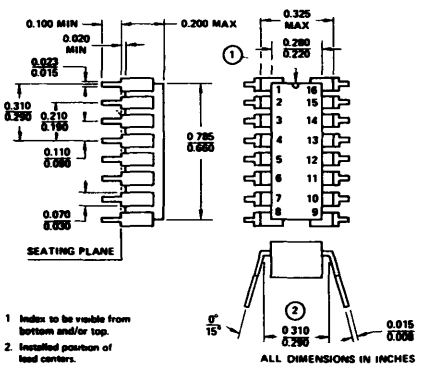
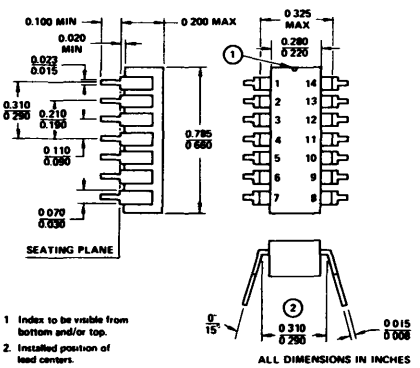
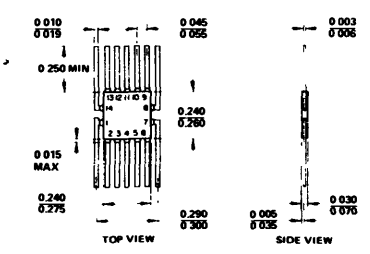


16-Pin Ceramic DIP
Tin-Plated Kovar Leads
G115BK

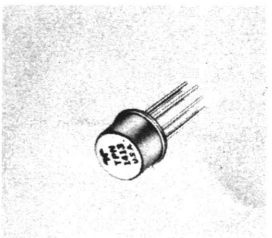


TO-116 Ceramic DIP
Tin-Plated Kovar Leads
G123BK



TO-86
G123BL

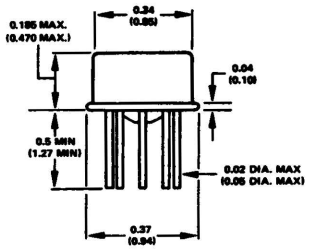
Siliconix incorporated

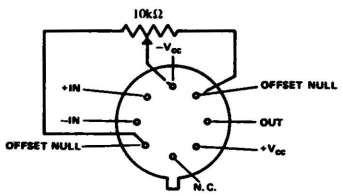


model 1413

precision microcircuit operational amplifier

6.0 Component Data Sheets (contd.)





MATING SOCKET
*MF-03-98

NOTE: ALL DIMENSIONS IN PARENTHESIS ARE EXPRESSED IN CENTIMETERS

* This socket not supplied by Teledyne Philbrick Nexus. Available from Barnes Corp. Lansdowne, Pa., 19050

** CAUTION: Avoid shorts to case. Case is connected internally to −15V power supply at Pin 4.

FEATURES:

- Low Bias Current 2nA
- High Differential Input Impedance 10MΩ
- 2mV Initial Offset Voltage
- 20,000 CMRR
- 40,000 Open Loop Gain

DESCRIPTION:

Model 1413 combines the above features with high common mode voltages and internal stabilization to eliminate the need of special external components for frequency compensation.

Packaging: TO-99 case with a pin configuration compatible with the 709 operational amplifier.

Applications: The low bias current of Model 1413 minimizes circuit or current error, making it ideal for use as: high impedance circuits, sample-and-hold amplifiers, integrators, fast summing amplifiers, and low current amplifiers.

SPECIFICATIONS

Characteristics (Typical at 25°C, nominal supply voltage unless otherwise indicated)

		Symbol	Typ.	Guaranteed
OUTPUT RANGE				
Voltage (peak)	min.	E_o	±12.5V	±11V
Current	min.	I_o	±15mA	±5mA
VOLTAGE GAIN (dc, open loop)				
Rated load	min.	A_o	40,000	15,000
10K load	min.	–	60,000	
FREQUENCY RESPONSE (inverting)				
Small signal (unity gain, open loop)	min.	f_t	0.5MHz	
Large signal: full output (undistorted)	min.	f_s		–
full output (peak-to-peak)	min.	f_p		10kHz
Slew rate		sr	0.6V/μsec	
Settling time to ±0.1% (step input)		ts	20μsec	
Overload recovery time (step input)		τ_{OL}	30μsec	
Max. cap. loading w/o causing instability		C_L	300pF	
INPUT VOLTAGE RANGE				
Common mode: dc linear operation	min.	E_{CM}	±13V	±12V
fault	abs. max.	–		
Differential (between inputs)	abs. max.	E_D		
Common mode rejection ratio		CMRR	20,000	4,000
INPUT VOLTAGE OFFSET				
Initial (without external trim) @25°C		E_{os}	±2mV	
Zero adjustment		R_{os}	10kΩ pot.	
Vs. temperature (avg. -25°C to +85°C)	max.	$E_{os}TC$	±20μV/°C	
Vs. time (per 24 hrs.)		$\Delta E_{os}/\Delta t$		–
Vs. power supply		PSRR		–
INPUT BIAS CURRENT				
Initial @25°C	max.	I_B	±2nA	±10nA
Vs. temperature (avg. -25°C to +85°C)	max.	$\pm I_B TC$		0.3nA/°C
Vs. power supply		$\Delta I_B/\Delta Vcc$		–
Vs. time (per 24 hrs.)		$\Delta I_B/\Delta t$		–
Difference (tracking)		I_D	±0.5nA	
INPUT IMPEDANCE @dc				
Differential		Z_D	10MΩ‖5pF	
Common mode (either input to common)		Z_{CM}	100MΩ‖5pF	
OUTPUT IMPEDANCE (open loop) at 5Hz		Z_o		–
NOISE (Referred to input)				
Flicker (0.016 to 1.6Hz)				
Voltage p-p		e_n	5μV	
Current p-p		i_n		–
Midband (1.6 to 160Hz)				
Voltage rms		e_n		–
Current rms		i_n		–
Broadband (160Hz to 16 kHz)				
Voltage rms		e_n	15μV	
Current rms		i_n		–
POWER REQUIREMENTS				
Nominal supply voltage		$\pm V_{cc}$	±15V	
Voltage range		–	±(3 to 18)V	
Current: quiescent	max.	$\pm I_{cc}$	±1.5mA	±3mA
full load	max.	$I_{cc}+I_o$		±8mA
TEMPERATURE RANGE (degrees C)				
Operating: rated		T_o		-25°C to +85°C
derated		–		
Storage		T_s		-55°C to +125°C

Prices and data subject to change without notice.

Teledyne Philbrick Nexus makes no representation that use of its modules in the circuits described herein or use of other technical information contained herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of licenses to make, use, or sell equipment constructed in accordance therewith.

EEM FILE 1100

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ALLIED DRIVE AT ROUTE 128, DEDHAM, MASSACHUSETTS 02026
TEL: (617) 329-1600 • TWX: (710) 348-6726 • TELEX: 92-4439

7.0 Multiplexer Wiring List

Channel Number	Connector	Pin No.	Function
1	J2	EE	Sig
		FF	Ret
2	J2	HH	Sig
		JJ	Ret
3	J1	A	Sig
		B	Ret
4	J1	C	Sig
		D	Ret
5	J1	E	Sig
		F	Ret
6	J1	H	Sig
		J	Ret
7	J1	K	Sig
		L	Ret
8	J1	M	Sig
		N	Ret
9	J1	P	Sig
		R	Ret
10	J1	S	Sig
		T	Ret
11	J1	U	Sig
		V	Ret
12	J1	W	Sig
		X	Ret
13	J1	Y	Sig
		Z	Ret
14	J1	a	Sig
		b	Ret
15	J1	c	Sig
		d	Ret
16	J1	e	Sig
		f	Ret
17	J1	h	Sig
		j	Ret
18	J1	k	Sig
		l	Ret
19	J1	m	Sig
		n	Ret
20	J1	p	Sig
		r	Ret
21	J1	s	Sig
		t	Ret
22	J1	u	Sig
		v	Ret
23	J1	w	Sig
		x	Ret
24	J1	y	Sig
		z	Ret
25	J1	AA	Sig
		BB	Ret
26	J1	CC	Sig
		DD	Ret
27	J2	A	Sig
		B	Ret
28	J2	C	Sig
		D	Ret
29	J2	E	Sig
		F	Ret
30	J2	H	Sig
		J	Ret
31	J2	K	Sig
		L	Ret
32	J2	M	Sig
		N	Ret
33	J2	P	Sig
		R	Ret
34	J2	S	Sig
		T	Ret
35	J2	U	Sig
		V	Ret
36	J2	W	Sig
		X	Ret
37	J2	Y	Sig
		Z	Ret
38	J2	a	Sig
		b	Ret
39	J2	c	Sig
		d	Ret
40	J2	e	Sig
		f	Ret
41	J2	h	Sig
		j	Ret
42	J2	k	Sig
		l	Ret

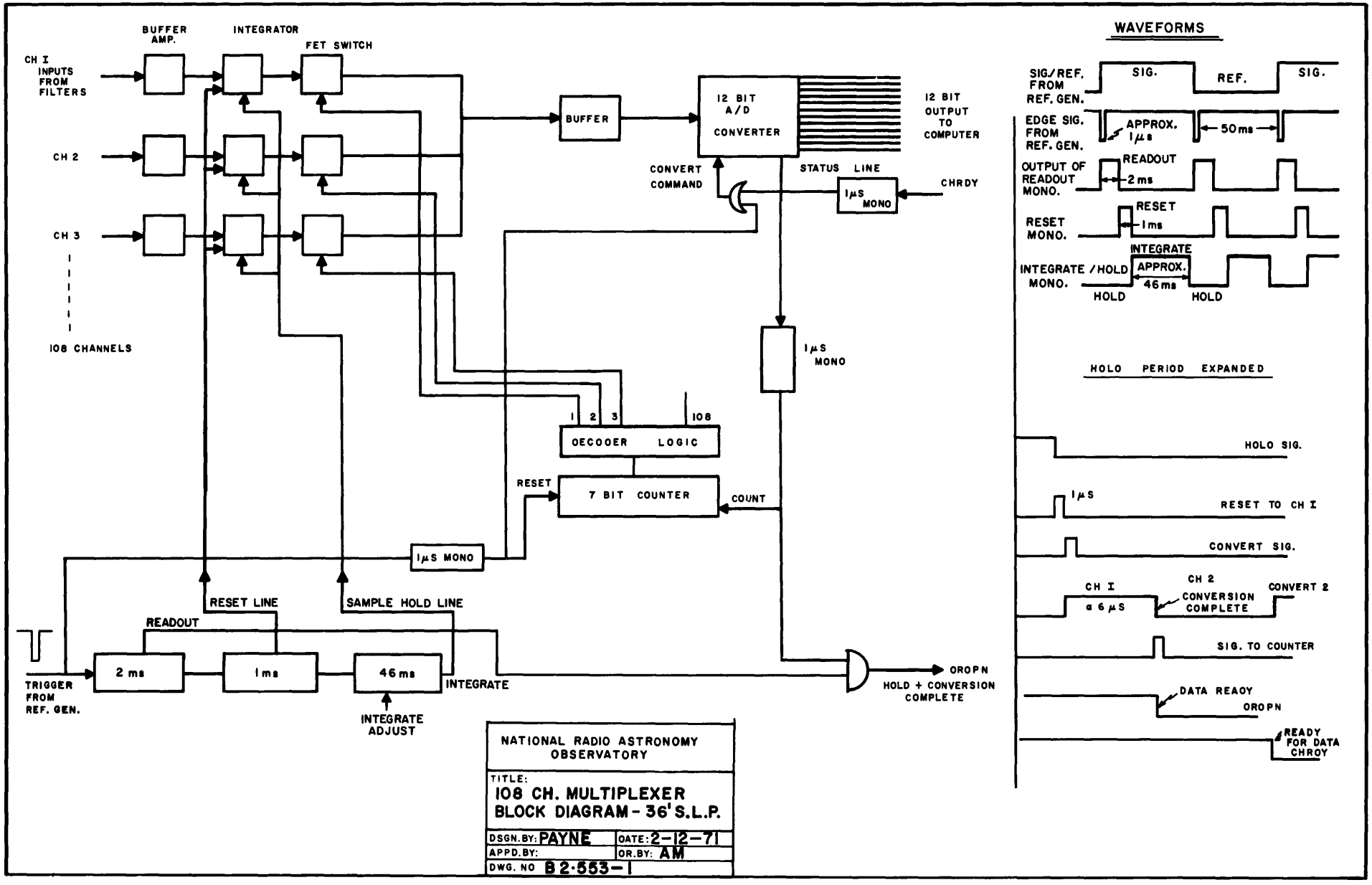
7.0 Multiplexer Wiring List (continued):

Channel Number	Connector	Pin No.	Function
43	J2	m	Sig
		n	Ret
44	J2	p	Sig
		r	Ret
45	J2	s	Sig
		t	Ret
46	J2	u	Sig
		v	Ret
47	J2	w	Sig
		u	Ret
48	J2	y	Sig
		z	Ret
49	J2	AA	Sig
		BB	Ret
50	J2	CC	Sig
		DD	Ret
51	J4	EE	Sig
		FF	Ret
52	J4	HH	Sig
		JJ	Ret
53	J3	A	Sig
		B	Ret
54	J3	C	Sig
		D	Ret
55	J3	E	Sig
		F	Ret
56	J3	H	Sig
		J	Ret
57	J3	K	Sig
		L	Ret
58	J3	M	Sig
		N	Ret
59	J3	P	Sig
		R	Ret
60	J3	S	Sig
		T	Ret
61	J3	U	Sig
		V	Ret
62	J3	W	Sig
		X	Ret
63	J3	Y	Sig
		Z	Ret

Channel Number	Connector	Pin No.	Function
64	J3	a	Sig
		b	Ret
65	J3	c	Sig
		d	Ret
66	J3	e	Sig
		f	Ret
67	J3	h	Sig
		j	Ret
68	J3	k	Sig
		l	Ret
69	J3	m	Sig
		n	Ret
70	J3	p	Sig
		r	Ret
71	J3	s	Sig
		t	Ret
72	J3	u	Sig
		v	Ret
73	J3	w	Sig
		u	Ret
74	J3	y	Sig
		z	Ret
75	J3	AA	Sig
		BB	Ret
76	J3	CC	Sig
		DD	Ret
77	J4	A	Sig
		B	Ret
78	J4	C	Sig
		D	Ret
79	J4	E	Sig
		F	Ret
80	J4	H	Sig
		J	Ret
81	J4	K	Sig
		L	Ret
82	J4	M	Sig
		N	Ret
83	J4	P	Sig
		R	Ret
84	J4	S	Sig
		T	Ret

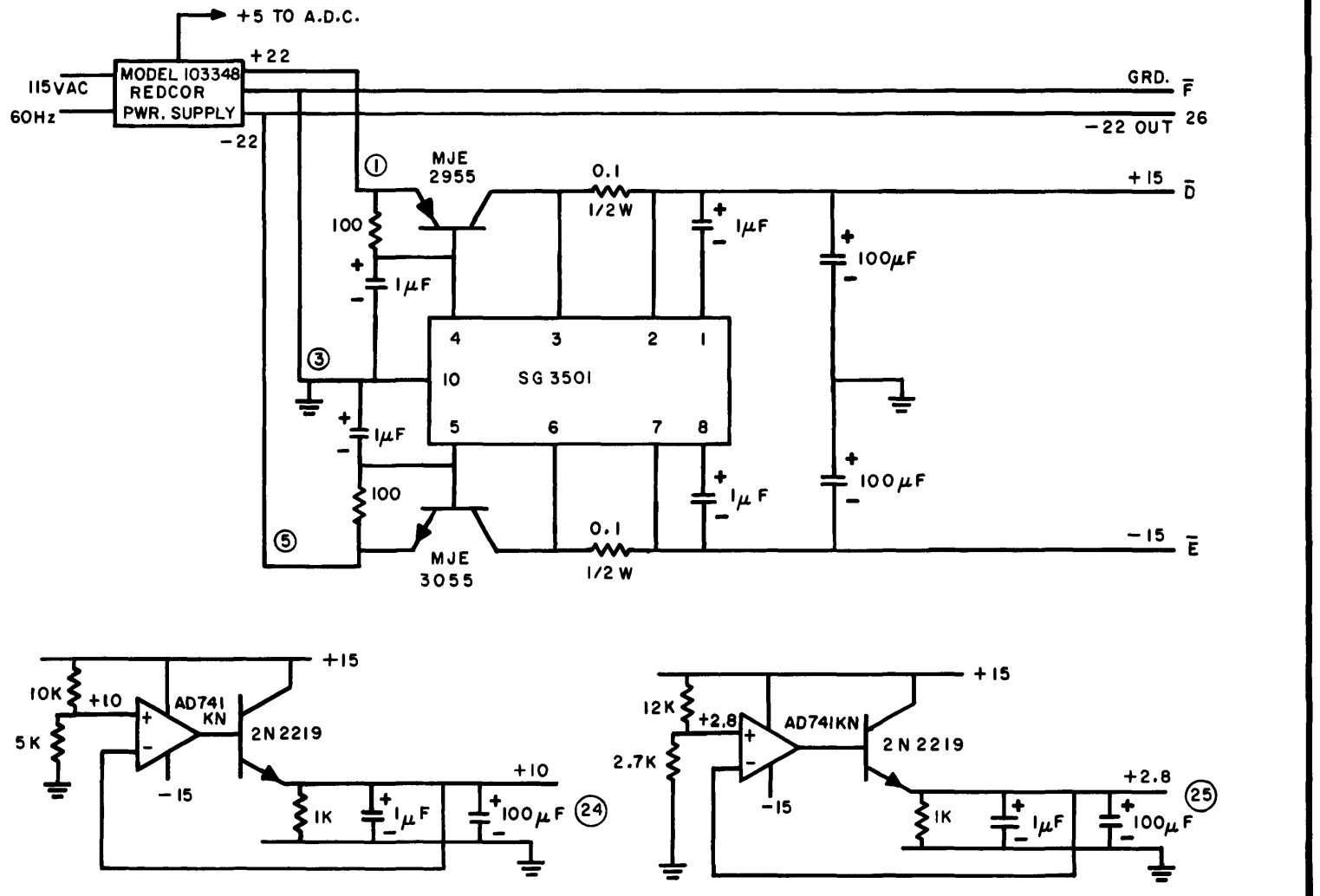
7.0 Multiplexer Wiring List (continued):

Channel Number	Connector	Pin No.	Function
85	J4	U	Sig
		V	Ret
86	J4	W	Sig
		X	Ret
87	J4	Y	Sig
		Z	Ret
88	J4	a	Sig
		b	Ret
89	J4	c	Sig
		d	Ret
90	J4	e	Sig
		f	Ret
91	J4	h	Sig
		j	Ret
92	J4	r	Sig
		l	Ret
93	J4	m	Sig
		n	Ret
94	J4	p	Sig
		r	Ret
95	J4	s	Sig
		t	Ref
96	J4	u	Sig
		v	Ret
97	J4	w	Sig
		u	Ret
98	J4	y	Sig
		z	Ret
99	J4	AA	Sig
		BB	Ret
100	J4	CC	Sig
		DD	Ret



NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: 108 CH. MULTIPLEXER BLOCK DIAGRAM - 36' S.L.P.	
DSGN. BY: PAYNE	DATE: 2-12-71
APPD. BY:	DR. BY: AM
DWG. NO B2-553-1	

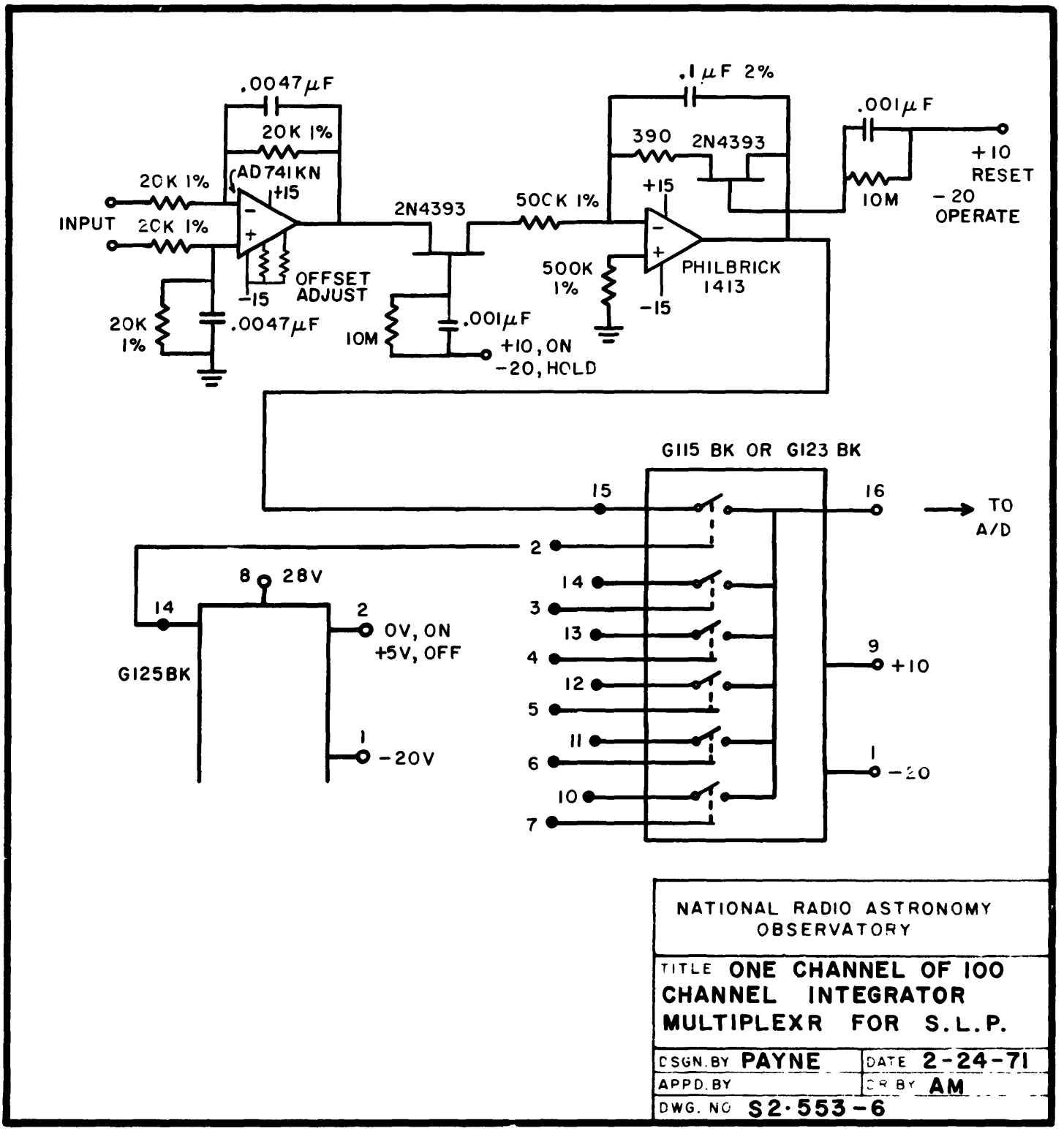
FIG. 1



CARD 1

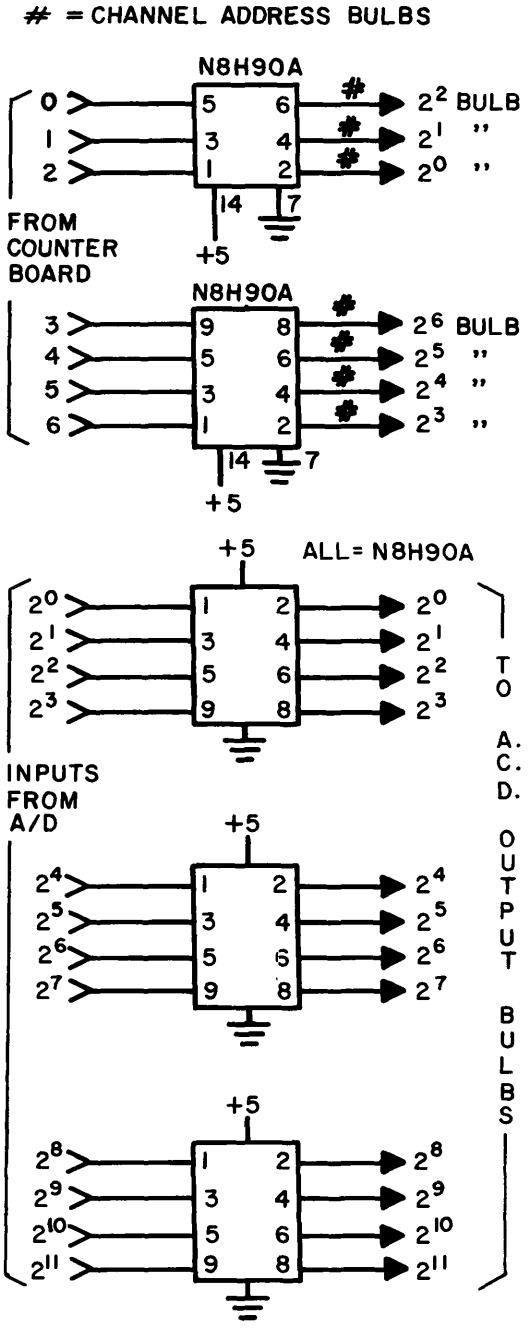
NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MULTIPLEXER POWER SUPPLY FOR S.L.P.	
DSGN. BY: PAYNE	DATE: 2-19-71
APP'D. BY:	DR. BY: AM
DWG. NO. S2-553-3	

FIG. 2



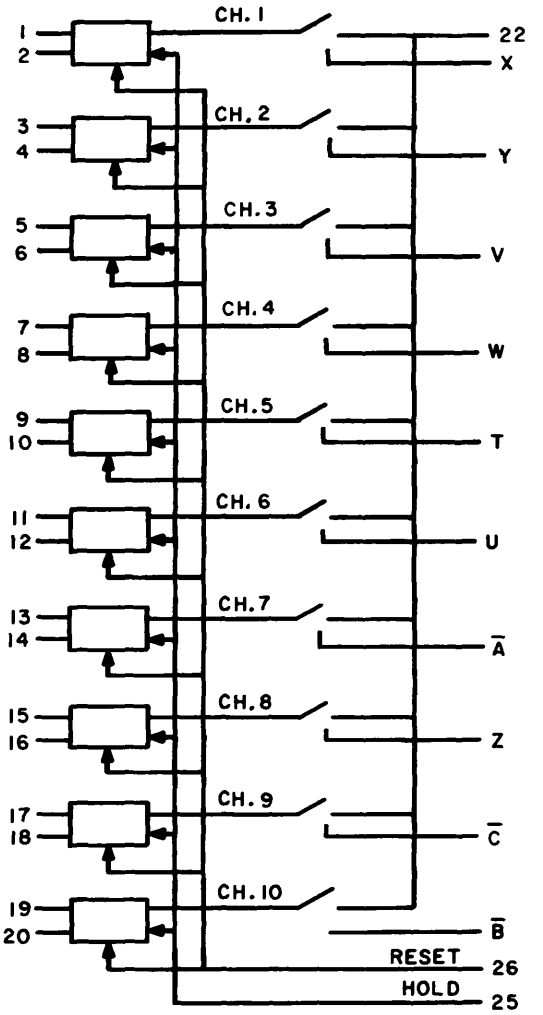
NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE ONE CHANNEL OF 100 CHANNEL INTEGRATOR MULTIPLEXR FOR S.L.P.	
DSGN. BY PAYNE	DATE 2-24-71
APPD. BY	DR BY AM
DWG. NO S2-553-6	

FIG. 3



BULB DRIVER BOARD

FIG. 9



PIN	
+15 –	D
GRD –	F
−15 –	E
−22 –	21
+10 –	23
+28 –	24

GRD – CH. SELECT
+5 – RESET
GRD – HOLD

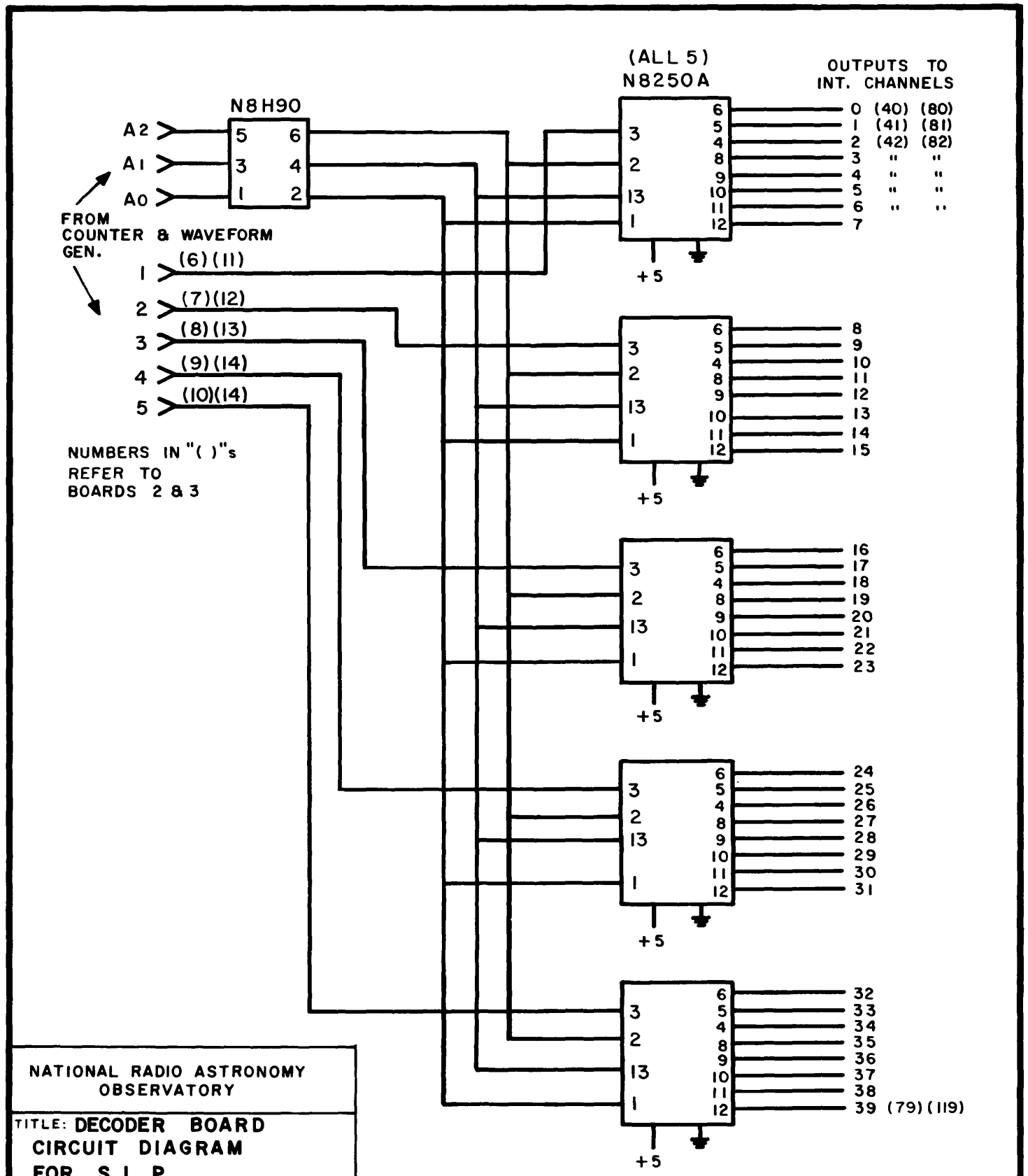
BLOCK DIAGRAM – INTEGRATOR & MULTIPLEXER CARD

CARD 2–12

FIG. 4

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: BULB DRIVER BOARD AND INTEGRATOR/MULTIPLEXER CARD FOR S.L.P.	
DSGN. BY: PAYNE	DATE: 2-19-71
APPD. BY:	DR. BY: AM
DWG. NO. B 2-553-3	

FIG. 4 & 9



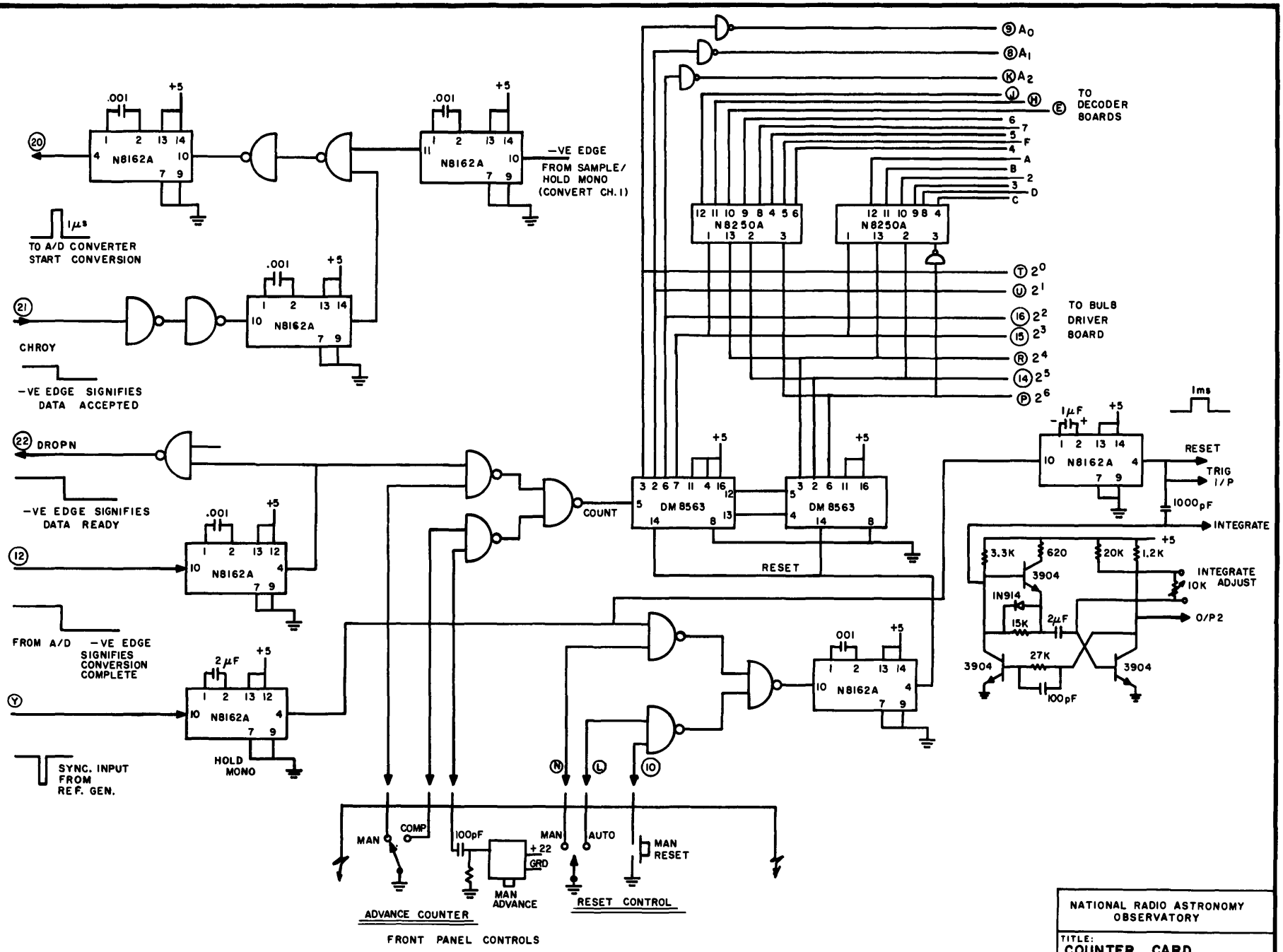
NATIONAL RADIO ASTRONOMY OBSERVATORY

TITLE: DECODER BOARD CIRCUIT DIAGRAM FOR S.L.P.

DSGN. BY: PAYNE	DATE: 2-19-71
APP'D. BY:	DR. BY: AM
DWG. NO. S2·553-4	

CARD 13 — 15

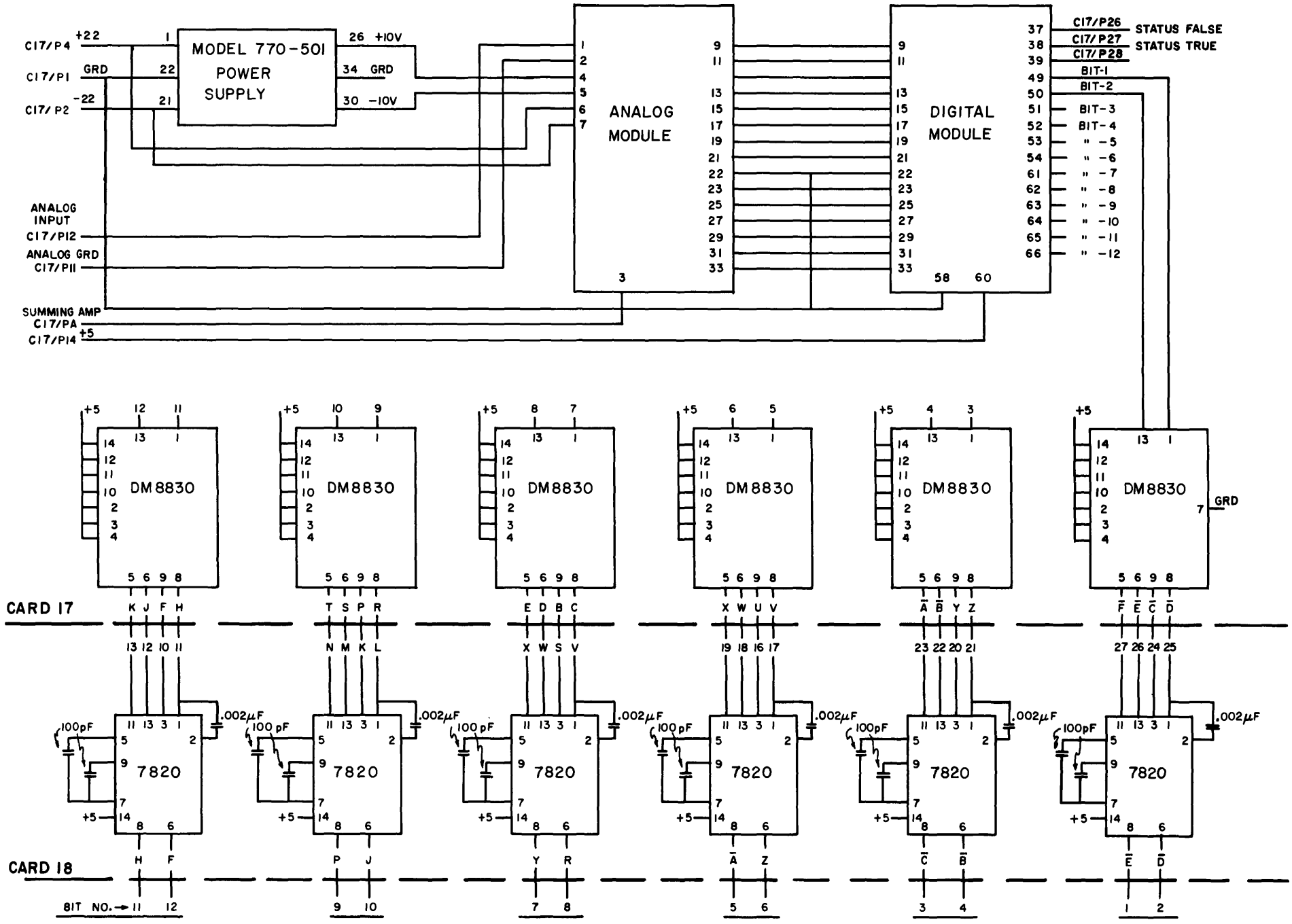
FIG. 5



NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: COUNTER CARD 36' S.L.P.	
DSGN. BY: PAYNE	DATE: 2-16-71
APP'D. BY	DR. BY A. M.
DWG. NO S2.553-2	

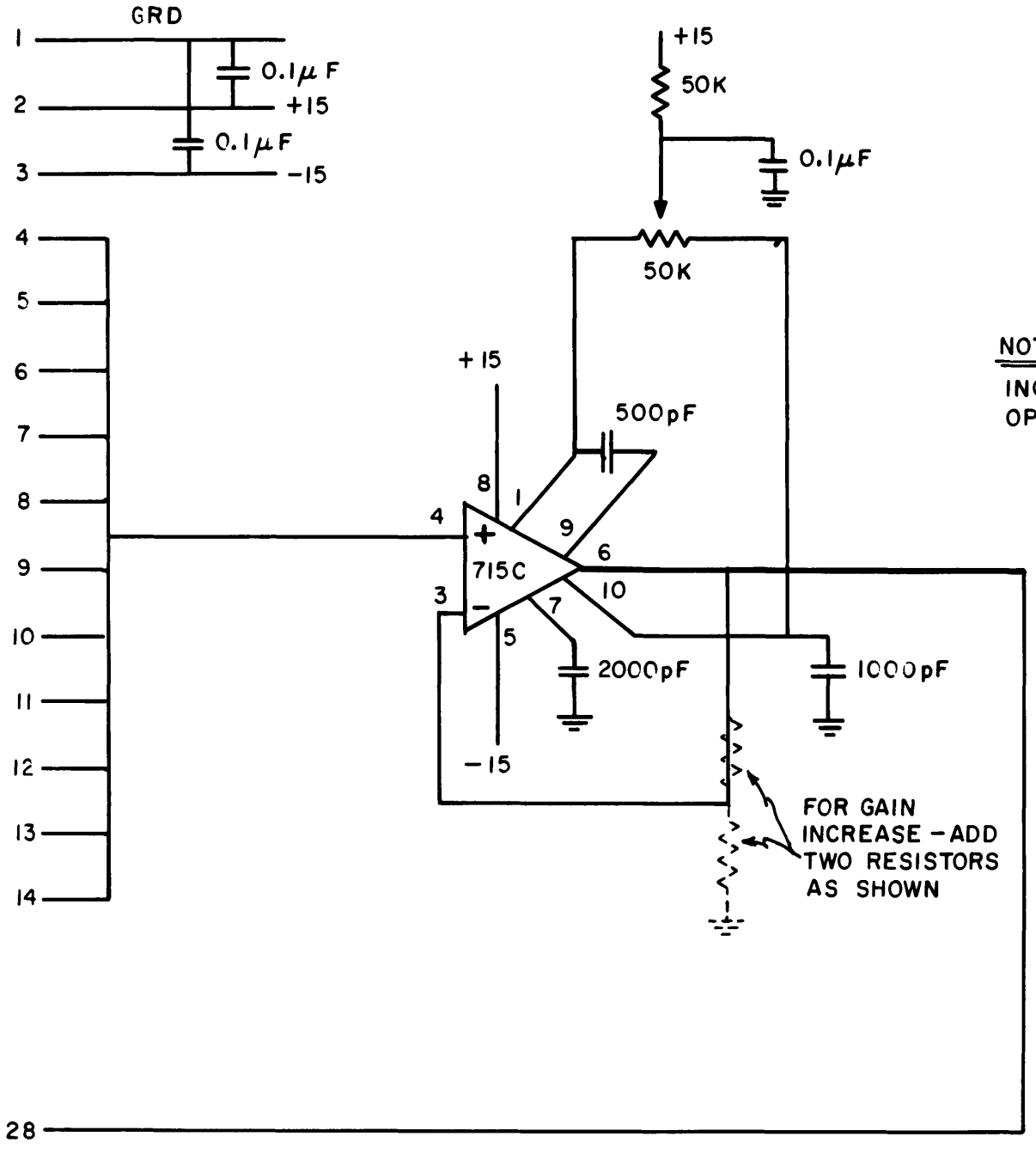
CARD 16

FIG. 6



A/D CONVERTER – CARD 17 & LINE RECEIVERS — CARD 18

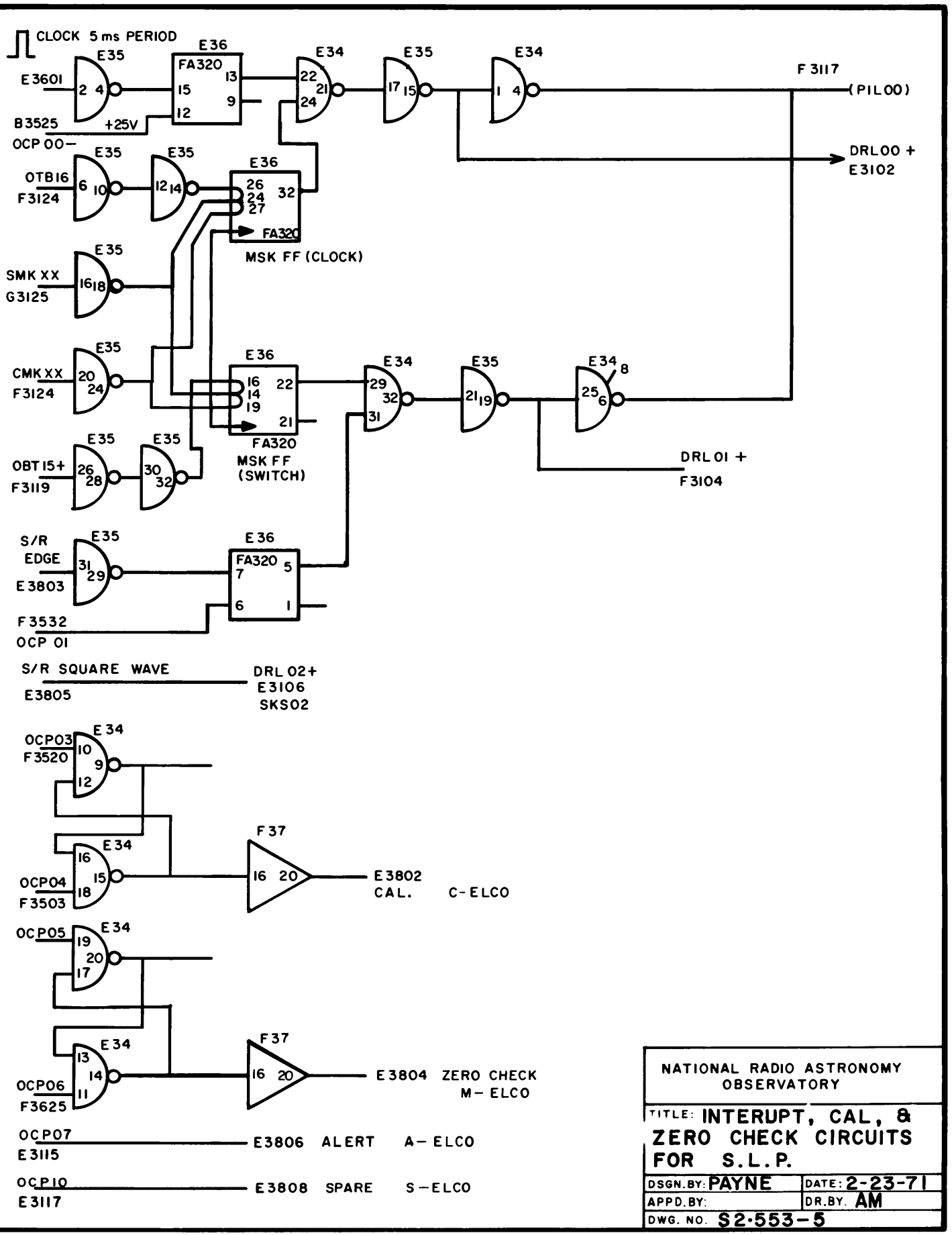
FIG. 7



NOTE: ADDITIONAL AMPLIFIER INCLUDED ON BOARD TO ACCOMODATE OPPOSITE POLARITY INPUTS.

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: A/D BUFFER	
DSGN. BY: PAYNE	DATE: 4-28-71
APPD. BY:	DR. BY: AM
DWG. NO. S2·553-9	

CARD 18
FIG. 8



NATIONAL RADIO ASTRONOMY OBSERVATORY

TITLE: INTERUPT, CAL, & ZERO CHECK CIRCUITS FOR S.L.P.

DSGN.BY: PAYNE	DATE: 2-23-71
APPD.BY:	DR.BY. AM
DWG. NO. S2·553-5	

FIG. 10

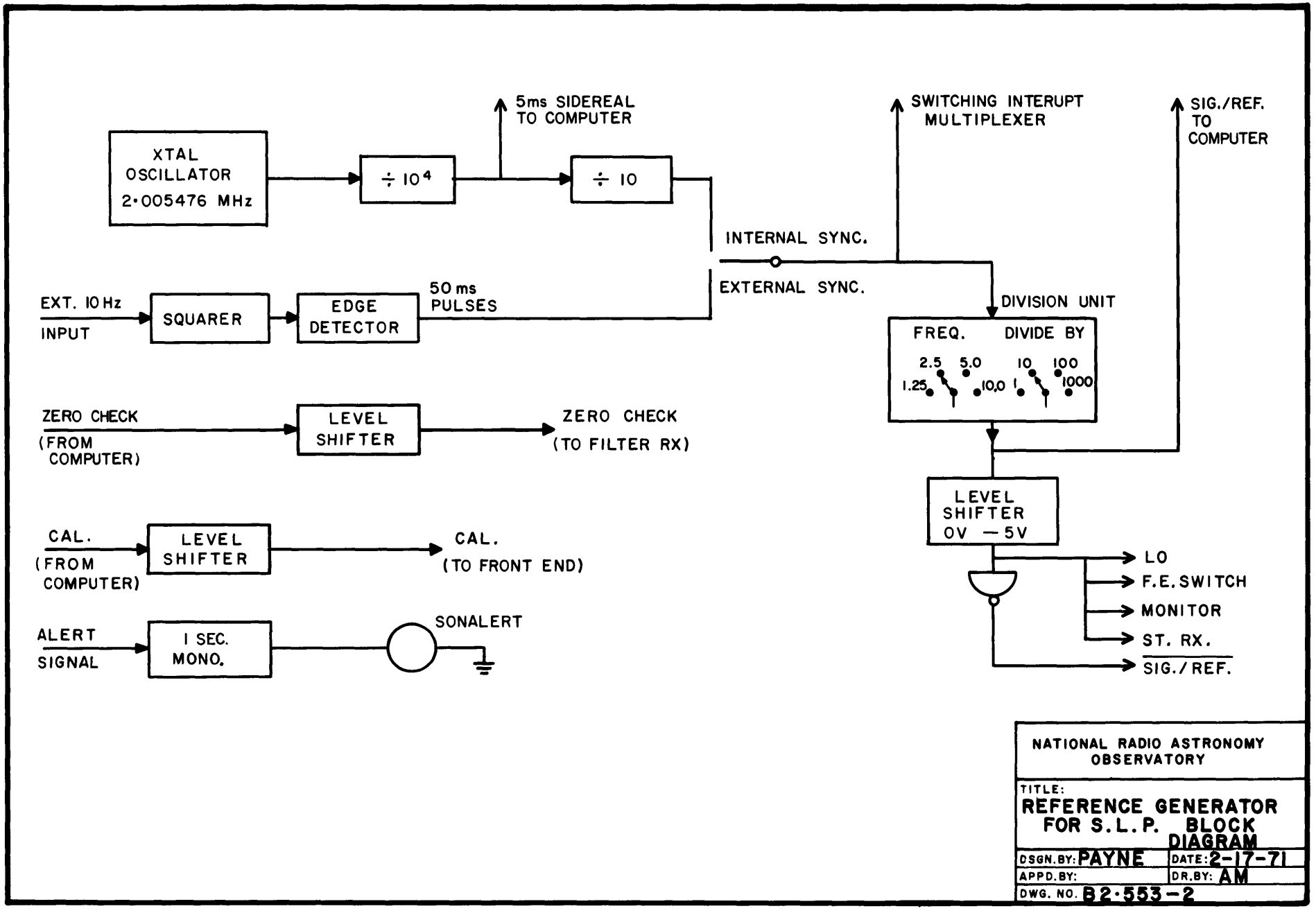
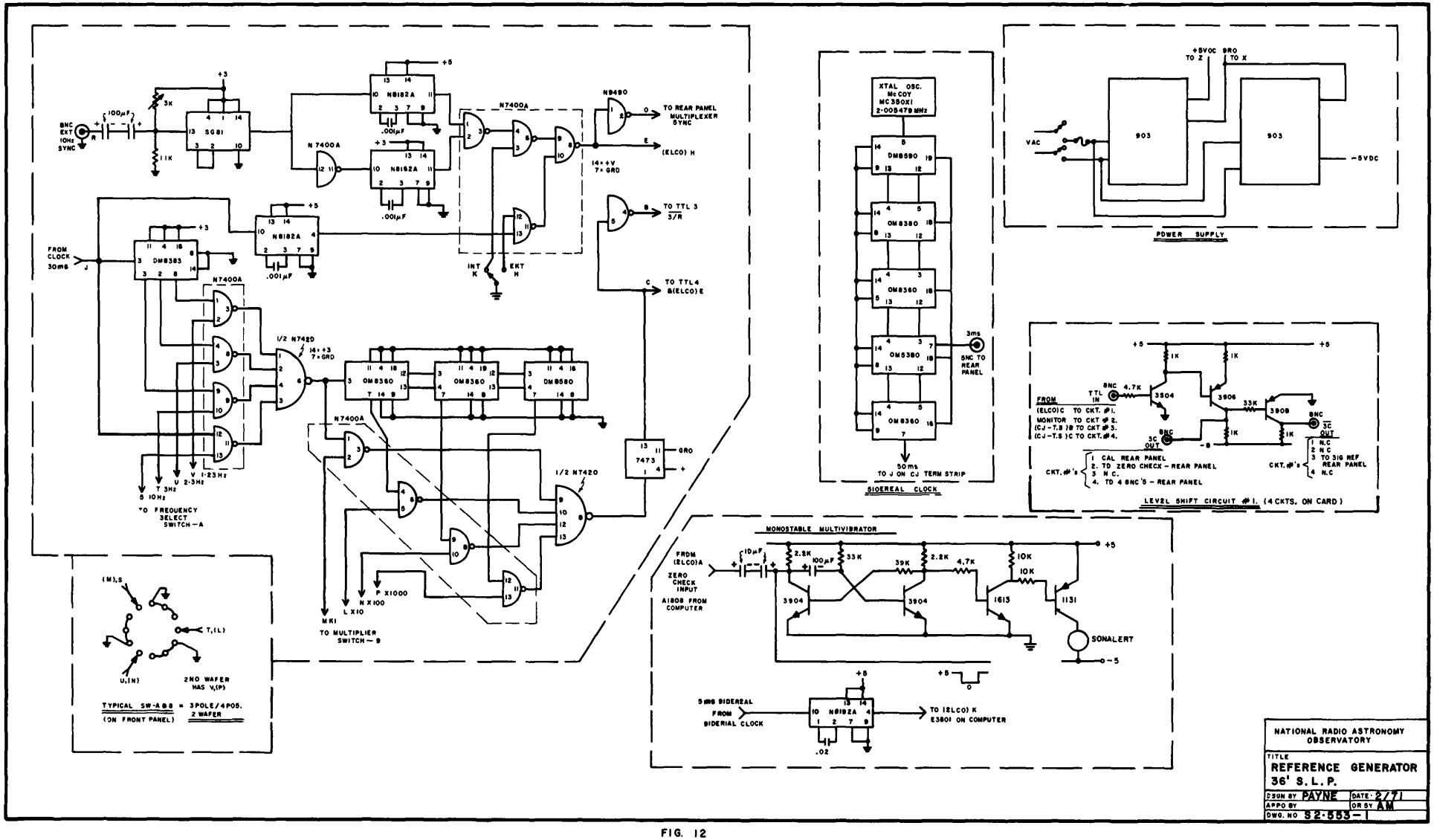

XTAL OSCILLATOR 2·005476 MHz
÷ 10⁴
5ms SIDEREAL TO COMPUTER
÷ 10
INTERNAL SYNC.
EXTERNAL SYNC.
SWITCHING INTERUPT MULTIPLEXER
SIG./REF. TO COMPUTER
DIVISION UNIT
FREQ. DIVIDE BY
2.5 5.0 10 100
1.25 10.0 1 1000
EXT. 10 Hz INPUT
SQUARER
EDGE DETECTOR
50 ms PULSES
ZERO CHECK (FROM COMPUTER)
LEVEL SHIFTER
ZERO CHECK (TO FILTER RX)
LEVEL SHIFTER 0V — 5V
CAL. (FROM COMPUTER)
LEVEL SHIFTER
CAL. (TO FRONT END)
LO
F.E. SWITCH
MONITOR
ST. RX.
SIG./REF.
ALERT SIGNAL
1 SEC. MONO.
SONALERT
NATIONAL RADIO ASTRONOMY OBSERVATORY
TITLE:
REFERENCE GENERATOR FOR S.L.P. BLOCK DIAGRAM
DSGN. BY: PAYNE
DATE: 2-17-71
APPD. BY:
DR. BY: AM
DWG. NO. B2·553-2

FIG. 11



NATIONAL RADIO ASTRONOMY OBSERVATORY

TITLE
REFERENCE GENERATOR
36' S. L. P.

DSGN BY PAYNE	DATE 2/71
APPD BY	DR BY AM
DWG. NO S2-553-	

FIG. 12