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NRAO 36-FOOT TELESCOPE POSITION CONTROL SERVO ADDITIONS:

1. Baldwin Position Encoder
2. Interface Box for Encoder
3. Electronic Tachometer System
4. Coarse Position Readout Converter

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1. ABSTRACT

A new optical position encoder has been installed and several older ones have been modified providing improved position readout for the NRAO 36-foot telescope at Tucson. Further, a new tachometer system has been developed and coupled to the new position encoding system providing an all electronic means of providing the rate feedback signal to the telescope drive servo. Finally, a novel 12-bit position readout coupled to the position encoders, providing telescope position readout independent of the control computer, has been installed.

NRAO 36-FOOT TELESCOPE
POSITION CONTROL SERVO ADDITIONS

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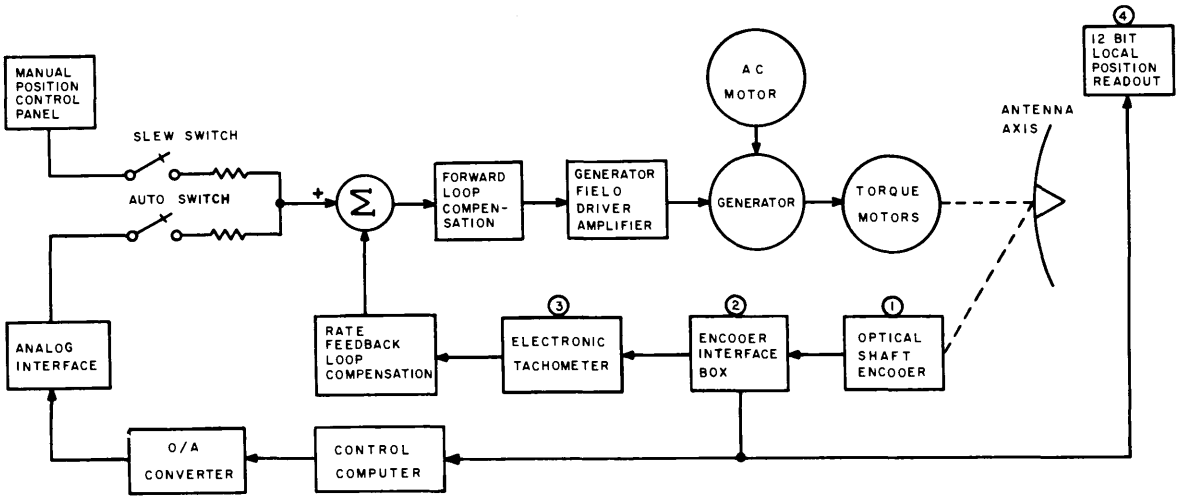
2. INTRODUCTION

The following report is intended to completely describe the new additions to the NRAO 36-foot telescope position control servo. The new additions include:

1. Optical shaft encoder - Baldwin model 694 BDL-1.
2. The new interface box for the Baldwin encoder.
3. Electronic tachometer system.
4. Local position readout system.

All information that is required to build, use, and repair the above systems is contained herein. There are other new additions to the servo which may be found in forthcoming reports by other personnel associated with these additions.



SIMPLIFIED BLOCK DIAGRAM OF POSITION CONTROL SYSTEM

FIG. 1

Figure 1 depicts the major parts of the position control system. Blocks 1, 2, 3, and 4 are the new additions described in this report.

There was no deviation from the prior art in the development of the position encoder interface box. New theory was employed in the synthesis of the seven least significant bits of the position encoder output, the technique used to generate the rate feedback signal provided by the electronic tach system, and the binary to angular degrees converter employed in the 12-bit local position readout system.

Several of the least significant bits in high resolution optical shaft encoders are synthesized from sine and cosine tracks on the outside edge of the code disk. These two tracks operate similar to the sine and cosine output windings of a conventional resolver except that the output carrier of the latter is usually 60, 400, or 10 kHz, while the encoder sine and cosine outputs employ a DC carrier. Hence, the encoder is referred to as an optical resolver with sin/cos output voltages following trigonometric values as a function of shaft angle according to the following definitions:

$$(1) \qquad \begin{aligned} \text{Sine Output} &= K \sin \alpha = X \\ \text{Cosine Output} &= K \cos \alpha = Y \end{aligned}$$

where K is the constant of proportionality and α = the angle through which the input shaft is positioned from reference. Now, if we modulate the sine and cosine outputs with equal modulation frequencies but 90 degrees phase difference, accordingly the following results:

$$(2) \qquad \begin{aligned} X_1 &= K \sin \alpha \cdot \cos \omega t \\ Y_1 &= K \cos \alpha \cdot \sin \omega t \end{aligned}$$

where ωt = modulation frequency.

Adding X_1 and Y_1 according to a well known trigonometric identity we obtain:

$$(3) \qquad X_1 + Y_1 = K (\sin \alpha \cdot \cos \omega t + \cos \alpha \cdot \sin \omega t) = K \sin (\alpha + \omega t)$$

So, as may be seen, if we turn the encoder shaft at a constant rate, frequency modulation of carrier (ωt) by a constant frequency αt results (constantly changing phase). But, if we rotate the shaft a fixed angle α , the phase of $X_1 + Y_1$ relative to the reference ωt will change by a constant phase angle. This principle allows the position of the encoder shaft

to be read out as a function of the phase difference between the phase variable signal (PVS) and reference (REF) with REF and PVS defined as,

$$(4) \qquad \begin{aligned} REF &= K \sin \omega t \\ PVS &= K \sin (\omega t + \alpha) \end{aligned}$$

Baldwin Electronics employs this technique in the new optical shaft encoder to synthesize the seven least significant bits by first band pass filtering K sin $(\omega t + \alpha)$ at the carrier frequency and then slicing the filter output producing the square wave PVS. The PVS is then phase compared to the REF in a 7-bit digital phase comparator, thus producing the seven LSB's. The REF + PVS are also made available by special order to the electronic tachometer producing the rate feedback to the telescope drive servo.

A simplified form of the Baldwin technique is employed in the new W/G to B/E modulator card newly installed in the Wayne George encoders producing the REF and PVS to the electronic tach system, where an analog phase comparator is coupled to an analog differentiator providing the rate feedback signal to the telescope servo.

A novel technique producing a binary to angular position conversion in the new 12-bit local position readout is employed allowing utilization of "off-the-shelf" building blocks to construct the local readout.

The basic problem is to convert a binary count A to a decimal count B. The count limits are:

Binary count (both)	$0.0 \leq A < 4096$
Decimal count (azimuth)	$0.0 \leq B < 360.0$
Decimal count (elevation)	$0.0 \leq B < 180.00$

A ratio or divider of some kind is needed. For example:

$$\text{Azimuth Ratio} = \frac{B}{A}$$

$$= \frac{3600}{4096}$$

$$= \frac{225}{256} \qquad \text{digital ratio}$$

$$= .8798\ 625 \qquad \text{analog ratio}$$

The analog ratio scheme was selected since only a digital panel meter, D/A converter, and resistor voltage divider are required as shown in Figure 2.

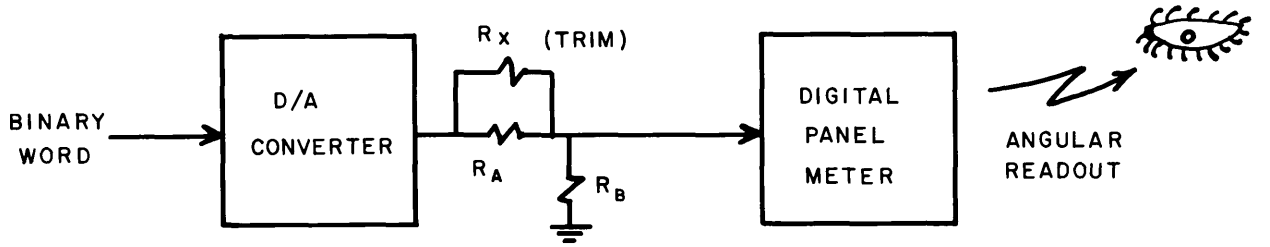


FIG. 2

The following computations are required:

$$\frac{\text{DPM}}{\text{DAC}} = \frac{0.36 \text{ volts}}{10.0 \text{ volts}}$$

$$= .036$$

$$= \frac{R_B}{R_A + R_B}$$

$$R_A = 26.8\ R_B$$

choose

$$R_A = 26.7 \text{ K } \Omega$$

$$R_B = 1.0 \text{ K } \Omega$$

$$R_X = 15 \text{ meg } \Omega$$

For elevation,

$$\frac{DPM}{DAC} = \frac{1.8 \text{ volts}}{10 \text{ volts}}$$

$$= 0.18$$

$$= \frac{R_B}{R_A + R_B}$$

$$R_A = 4.56\ R_B$$

choose

$$R_A = 4.64\ K\ \Omega$$

$$R_B = 1.0\ K\ \Omega$$

$$R_X = 680\ K\ \Omega$$

Thus, a simple, inexpensive and accurate local readout is afforded by this analog scheme in three steps:

1. Convert digital to analog.
2. Perform ratiometric conversion.
3. Convert analog to digital.

To build the same piece of gear using a digital scheme would require the use of highly specialized components and circuits that are more difficult to maintain.

Special meters have been produced at NRAO by a special drafting/photographic process. An ordinary panel meter is obtained, a special face is drafted over size, which is photographically reduced and reproduced on single weight, dull finish paper, and finally the meter face is removed while the photo-reproduction is cemented with pliobond cement to the back side. The meter face may be finished by filing around the edges carefully which produces a finished face that is hard to tell from a mass manufactured one. Examples of this technique may be seen on the encoder temperature indicator on the coarse position readout, all the meters on the electronic tachometer (see pictures in this report) and the lobe rotator phase indicators (picture in NRAO/EDIR 100).

3. SPECIFICATIONS

A. Encoder Interface Box

Input J-1: Interfaces directly with encoder supplying +5 and -5.5 V DC and TTL compatible input/output signals.

Computer Outputs J-2: Compatible with 3-C logic — 0, -6 V, current source to ground.

Lamp Display Outputs J-5: 0, -12 V with logic 1 = -12 V, current sinking to -12 V.

Modulator Outputs J-3: 32 kHz, differential, 50 Ω to ground, frequency modulated.

Power Supplies to Encoder: +5 V DC, 4 A max.
-5.5 V DC, 2 A max.

Power Supplies to Interface: -12 V DC, 1 A max.

Power Requirements: 115 V AC, 1 A max.

B. Electronic Tachometer

Number of Channels: 2 active
1 spare

Input Requirements: 32 kHz, differential 50 Ω to ground, frequency modulated ± 11 Hz.

Rate Output: ± 10 V, 5 mA max.

Rise Time: 4 milliseconds (τ < 2 milliseconds)

Scale Factor: Adjustable, approximately equal to $\frac{5 \text{ millivolts}}{\text{arc sec/sec}}$

Rate Indicator: 3 ranges switch selectable
Low — 30°/sec full scale
Med — 3°/min " "
High — 30°/min " "

Rate System Error: 0.1%.

B-1. Tachometer as Very Narrow Band FM Detector

Scale Factor: Adjustable to 1 volt/Hz.

Bandwidth: 80 Hertz.

Power Requirements: 115 V AC, 1 A.

C. Local Position Readout

Resolution:		12 bits binary both axis
Range:	Azimuth:	000.0° to 359.9°
	Elevation:	000.00° to 179.96°
Error:	Azimuth:	± .1°
	Elevation:	± .05°
Analog Output:		Linear within the limits for
	Azimuth:	0° = 0 V, 359.9° = 10 V
	Elevation:	0° = 0 V, 179.96° = 10 V
Input Requirements:		12 bits binary compatible with 3-C logic (0, -6 V)
Refresh Rate:		Adjustable from 1 Hz to 30 Hz via internal straps on DPM.

Encoder Temperature

Resolution:	20° 120° Coarse - Cold/Normal/Hot
Range:	0 - 150 °F
Error:	± 5 °F
Input Requirements:	0-5 mA via remote display cable from thermistor circuit.
Thermistor Type:	Fenwal No. GB 31 P2
Thermistor Location:	Baldwin Optical Unit Wayne George Electronics Unit
Power Requirements:	115 V AC, 1 A max.

4. PHYSICAL DESCRIPTION AND LOCATION

Most equipment associated with the telescope drive servo additions are located in easily accessible areas. The encoders and associated electronics and interface boxes are situated near the encoders at the ends of the telescope axis. The signal cables routed to the console and computer are multiconductor except for the special cable associated with the electronic tachometer located in the console. This special cable consists of two runs each axis of twin-ax 100 ohm differential, twisted-pair, shielded cable. There is one run each for the reference and phase variable signals from the Baldwin encoder interface box and from the special W/G to B/E modulator card located in slot 423 of the Wayne George encoder electronics box. The electronic tachometer output connects to the servo amplifier in the console via a "BNC" jumper cable.

The 12-bit local position readout is located in the console and is connected to the encoders via J-5, the remote lamp display cable by special jumper from the cable to the local readout chassis and back to the lamp display. Pictures of the equipment may be referred to in section 10. The local readout displays the telescope position on digital panel meters which may be calibrated from the front panel using the toggle switches and corresponding screw adjustments. This simple procedure is described in more detail in section 7. Also located in the center of the readout chassis is an indicator showing encoder temperature and a toggle for selecting the azimuth or elevation encoder thermistor. The thermistor is in the electronics unit of the Wayne George encoders and in the optical unit of the Baldwin system. The center-off position of the toggle turns off the entire temperature monitoring system including the local indicator in the Baldwin interface box.

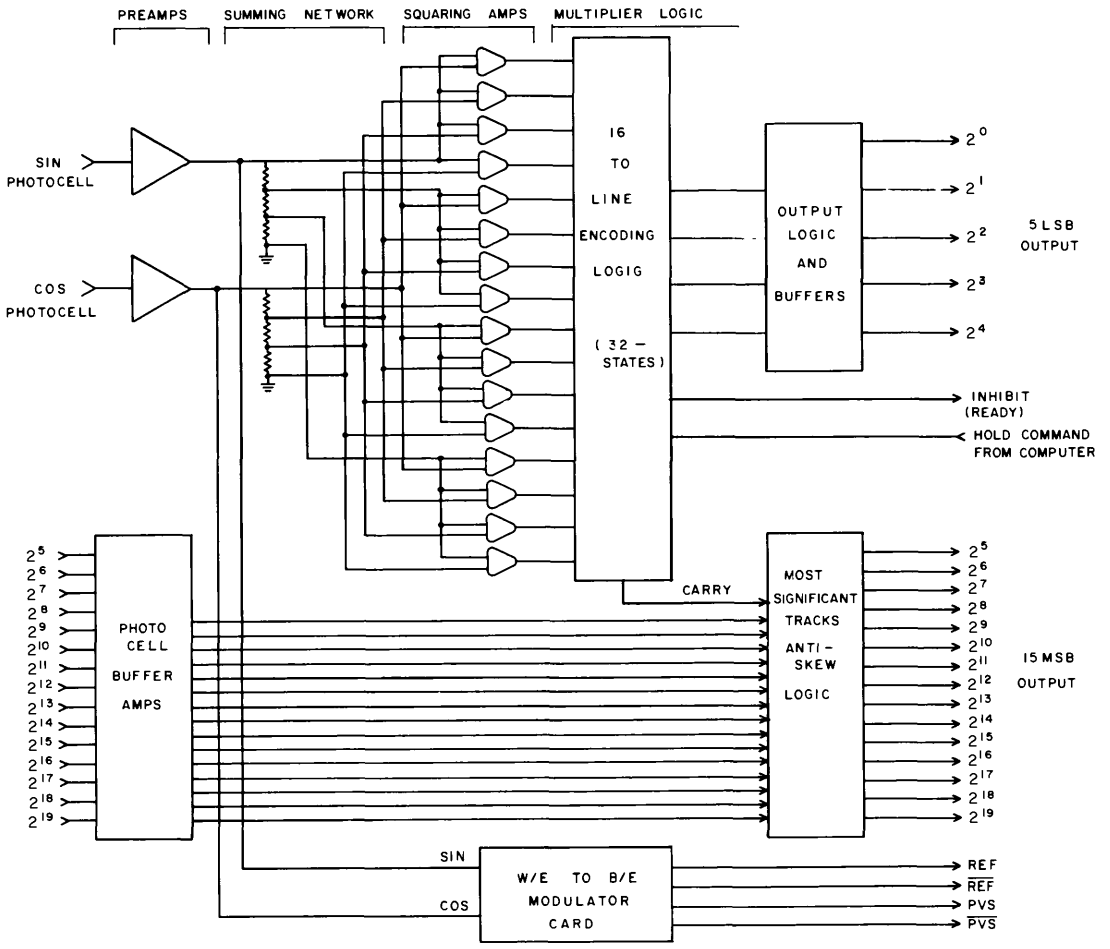
The electronic tachometer chassis contains various indicators showing normal system performance. Associated with each of two channels are two position indicators showing the condition of the phase detectors, a rate indicator meter showing telescope velocity switch selectable to one of three ranges, and lamp indicators for the channel switch, REF, and PVS status. Also in the center of the chassis is a selector switch allowing a spare channel to be switched in if there is a failure of the internal system.

5. SIMPLIFIED ELECTRONIC DESCRIPTION

The servo system additions comprising the Baldwin encoder and interface box, modifications to the Wayne George encoders, electronic tach, independent readout system, and computer modifications are all interconnected, making it necessary to discuss the entire system in one report. So, the following electronic discussions will consider the various circuits in a logical order, hopefully allowing the most understandable explanation to evolve. Block diagrams will be included; pictures are in section 10 and schematics are in section 11. The schematics are explained in detail in section 6. The index lists other sections that may be helpful in the following discussions.

In this system all telescope position and velocity information is produced by the optical shaft encoders. A simplified block diagram of the position control system is presented in Figure 1, section 2.

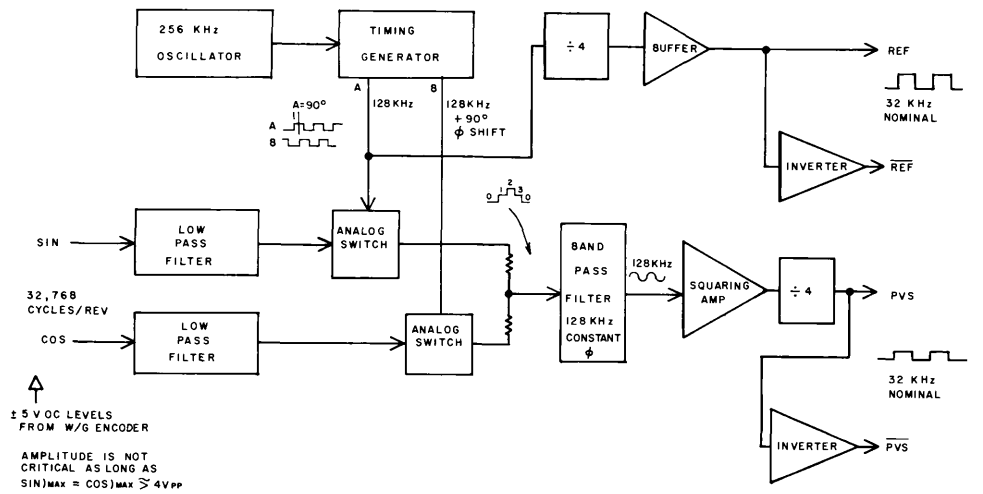
A block diagram of the Wayne George encoder is presented in Figure 3, showing modifications consisting of the W/E to B/E modulator card and associated wiring.



WAYNE GEORGE MODEL BD100 ENCODER BLOCK DIAGRAM
FIG. 3

This card which replaced the old 400 Hz resolver format modulator operates on the sine and cosine signals present at the sin/cos photocell preamps. Also operating from these preamps are the resistor networks providing scaled sine and cosine voltage inputs to the differential squaring amplifiers producing 16 lines that are encoded to 5 line binary data comprising the 5 least significant bits (LSB) of the encoder output. The 15 most significant bits (MSB) are produced by 30 photocells coupled to the buffer amplifiers. The anti-skew logic selects, as a function of shaft direction, which of the two photocells, laging or leading associated with each bit, is coupled to the output. Thus, the LSB's control all binary output code transitions in ripple down fashion from LSB to MSB. A more detailed discussion of the operation is found in the Wayne George encoder repair manual.

A block diagram of the W/E to B/E modulator card is presented in Figure 4.

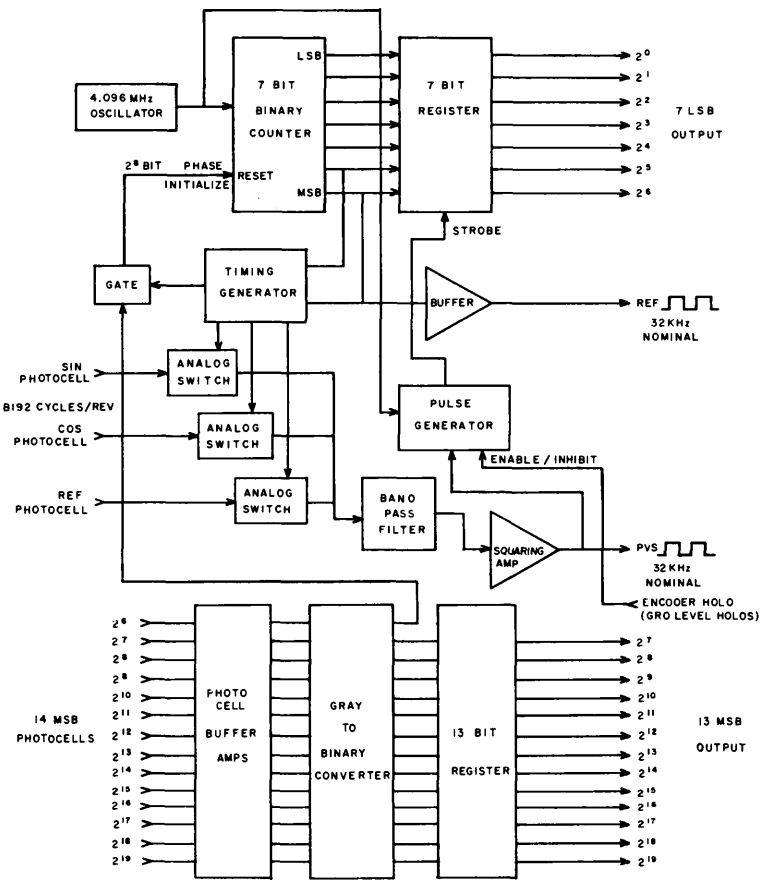


W/G TO BALDWIN FORMAT CONVERTER CARD

FIG. 4

The resolver type sine and cosine signals are present at the low-pass filters. The low-pass filters prevent switching transients produced by the analog switches from getting out into the encoder circuits. The analog switches sample the sin/cos signals in phase quadrature when operated from the timing generator. The differential signals REF and $\overline{\text{REF}}$ are buffered and transmitted to the electronic tach system. The analog switch sampled signals are summed at resistor summing networks coupled to the 128 kHz constant phase bandpass filter thus producing a sinusoidal output coupled to the squaring buffer amplifiers providing the PVS and $\overline{\text{PVS}}$ signals to the electronic tach system. The PVS signals are phase variable with respect to the REF signals since sine and cosine modulated signals (of varying magnitude) are summed into the bandpass filter. (See principle as explained in section 2.)

The Baldwin encoder uses an improved scheme of synthesizing the LSB's which is employed to produce 7 LSB's compared to the 5 LSB's produced in the Wayne George method. A functional block diagram of the Baldwin encoder is shown in Figure 5.



BALDWIN MODEL 694BL ENCODER BLOCK DIAGRAM

FIG. 5

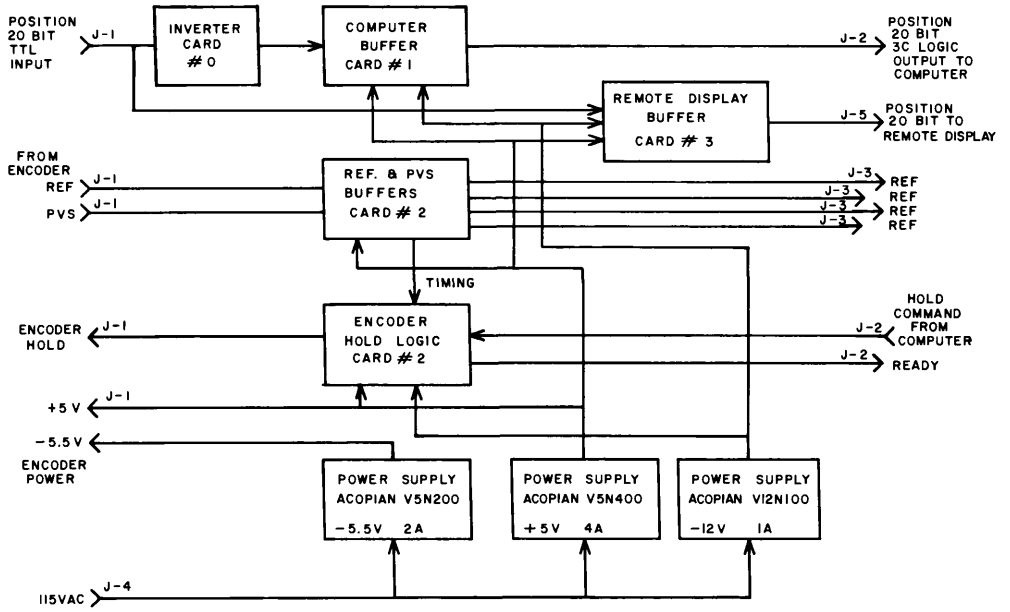
The LSB synthesis operates on the principle of phase comparison of a reference (REF) and phase variable signal (PVS). This is done by means of a 7-bit digital phase comparator comprising a binary counter whose output is strobed to an output register after the PVS undergoes a rising transition as seen at PIN 31 of the encoder connector. The 7-bit output register then contains a count that represents the phase between the REF and PVS signals.

The PVS is produced by sampling the sine and cosine photocell signals and a reference photocell signal providing a DC reference. The sampled outputs are summed and filtered similar to the method just described for the W/G to B/E modulator card. The REF and PVS signals are buffered in the encoder interface box and made available to the electronic tach providing rate data. The analog switches are operated by a special three-state timing generator. The encoder hold line inhibits the strobe to the encoder output registers.

The 14 MSB's in the Baldwin encoder are developed from 14 gray-encoded tracks. The photocells are amplified and coupled to a gray-to-binary converter (add one logic) and finally strobed into an output register synchronously with the LSB transitions.

The Baldwin encoder is made compatible with the existing Wayne George encoder system by circuits contained in the Baldwin encoder interface box. Figure 6 is a block diagram of the interface box.

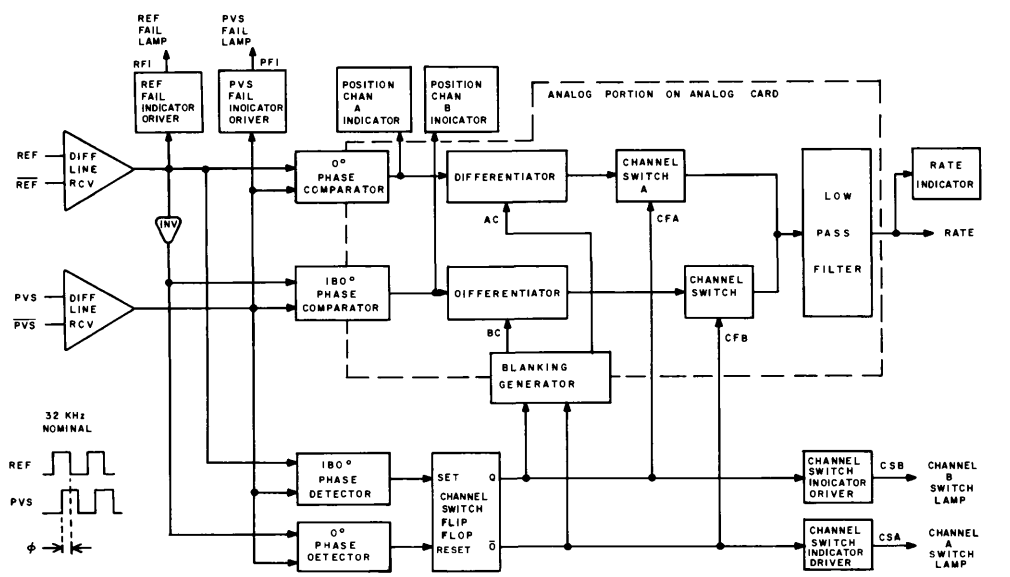
The interface box contains 3 power supplies providing power to the encoder and interface. All interface circuits are simple buffers except for the encoder hold logic on card 2. Here a hold command from the computer is synthronized with the PVS and then applied to the encoder. A return (ready) signal is then generated, informing the computer that the encoder output is frozen and ready to be strobed into the computer.



BALDWIN MODEL 694BL ENCODER INTERFACE BOX BLOCK DIAGRAM

FIG. 6

A functional block diagram of the electronic tachometer is shown in Figure 7.

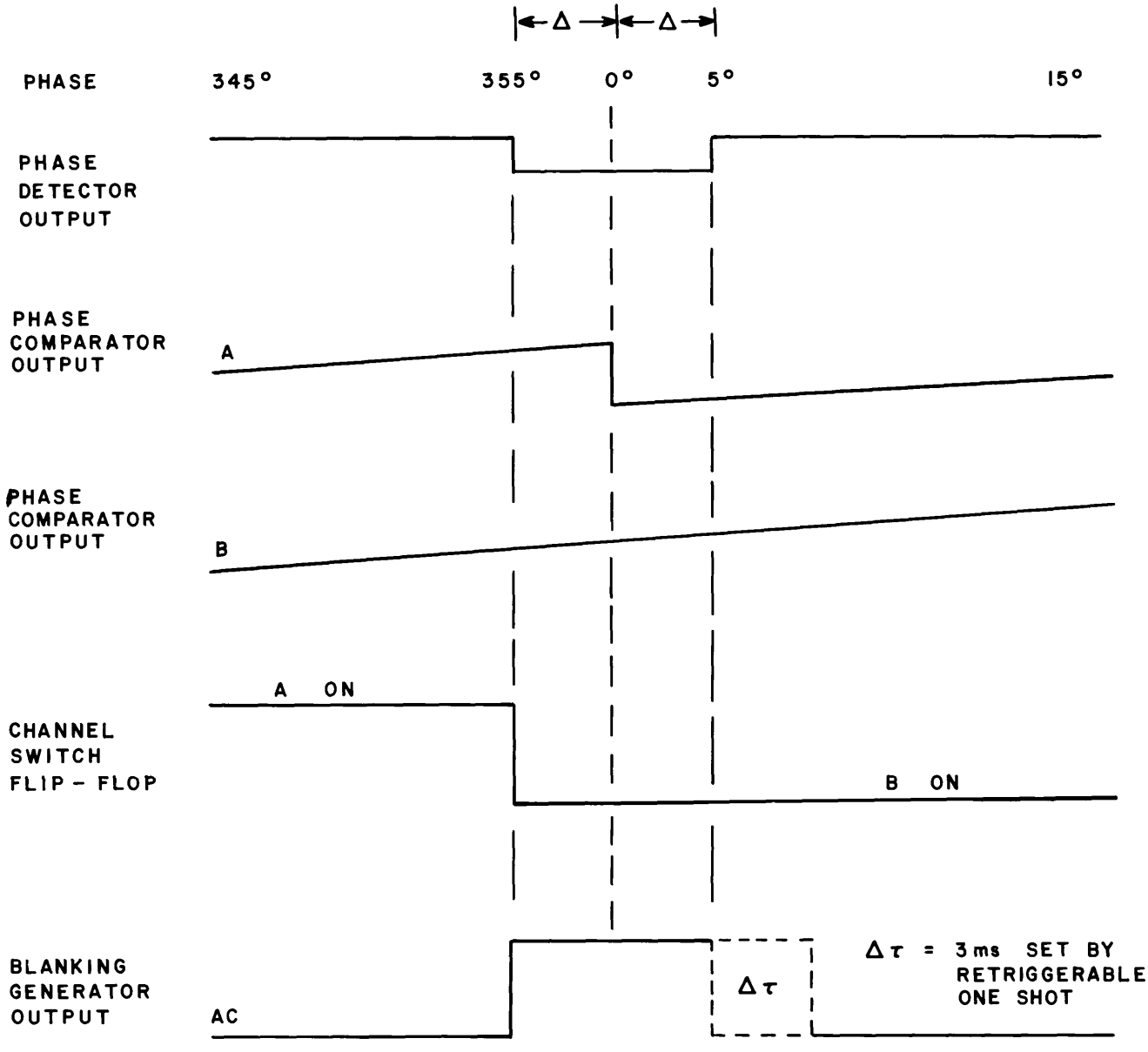


ELECTONIC TACH BLOCK DIAGRAM

FIG. 7

As may be seen the tach system operating principle is by means of a phase comparator providing position data coupled to a differentiator providing rate data. However, since a practical phase comparator output must return to zero (retrace) once every 360 electrical degrees or integer multiple thereof, it was necessary to employ two phase comparator-differentiator combinations with different retrace intervals in a two-channel arrangement such that channel "A" is sampled during channel "B" retrace and vice versa. Accordingly, a phase offset of 180 degrees is introduced into the channel B comparator. The two channels are sampled by channel FET switches A and B which are controlled by the channel switch flip-flop. The flip-flop is set and reset by the two phase detectors. Only one channel at a time is connected to the low pass filter that suppresses the small switching transients that occur. The dotted line in Figure 7 indicates the boundary between the digital and analog portions of the tach system. All of the digital portion is contained on the digital card 1, whereas all analog circuits are located on the analog card, thus minimizing the coupling of digital transients into the analog portions of the system. Also, for the same purpose a heavy shield separates the analog and digital circuits. So, in normal operation with a rate of 26 degrees/minute, 10 Hz sawtooth waveforms are present at the outputs of the phase comparators, one sawtooth shifted 180° in phase with respect to the other. The frequency is a function of rate. The differentiators produce a voltage output proportional to the frequency of the sawtooth waveforms. High differentiator output transients occur during phase comparator retrace. These transients are partially suppressed by the blanking generator.

The phase detectors are referred to as 0° and 180° detectors but in actual practice they detect $0° \pm \Delta$ and $180° \pm \Delta°$ where Δ is a direct function of the pulse widths of one shots A, B, and C. The 0° phase detector may actually produce a phase coincidence indication for 355° to 5° and likewise the 180° detector may indicate 175° to 185°. The precise width of this detection band is not important but only that the band exists. For it allows the channel switch to change states before the phase comparator retrace occurs as shown below in Figure 8.



TIMING DIAGRAM SHOWING THE OPERATION OF THE PHASE DETECTORS IN THE ELECTRONIC TACH. SYSTEM

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Page 14. change last line words "Figure 8" to "Timing Diagram. page 15" and insert the above timing diagram on the bottom of page 15.

The system status is indicated by various indicators as shown around the border of Figure 7.

The independent position readout system employs only three major parts readily obtainable off the shelf, namely, a D/A converter, a voltage divider resistance network, and digital panel meter. The system operating principle is discussed in section 2. A detector circuit was added to the DDP-116 computer to enable the encoders to function when the telescope drive program is not running. The detector circuit detects when the position is being read into the computer and accordingly resets an encoder hold inhibit flip-flop, thus allowing the encoder outputs to be frozen and read by the computer. When the program is halted and master clear is depressed, this flip-flop is set, allowing the independent readout to function when the computer is not readily position.

6. DETAILED ELECTRONIC DESCRIPTION

All schematics referred to in this section may be found in section 11. Pictures of the circuit cards and equipment are in section 10. Much information is contained within the schematics. For example, referring to schematic 1, which is a circuit diagram of card 0 of the Baldwin encoder interface box, we notice that the "chip" located in slot N on card 0 is a hex inverter whose input pin 1 is coupled from the encoder via pin C on the card edge connector and output pin 2 exits card pin 3. It may be helpful to refer to the block diagram in section 5, Figure 6, showing signal routing to card 0. Other block diagrams will similarly show signal routing for other cards and systems. In the schematic is shown spare parts of "chips" that are not used. In some cases signals are called out by a series of letters. The signal designation lists, section 12, defines these designations and functions. Similar notation as that used in schematic 1, for the inverter card 0, is used throughout the schematics. Also found are graphic representations of signals showing the active sense as an aid in drawing timing diagrams for troubleshooting purposes.

Schematic 2 shows the computer buffer card which is a simple level shift circuit interfacing the 20-bit position data (TTL) to the DDP-116 computer logic levels (3-C). A single PNP transistor is used with clamped collector to -6 V DC. The level shift circuit is non-inverting logical sense good to several MHz.

Schematic 3 is the encoder control card 2. The encoder hold synchronizer circuit is at the top of the drawing. The operation is as follows: A hold level command is issued from the computer (-6) which is level shifted to (TTL) ground by "chip" H and inverted by F, causing the D input to the 7474 flip-flop B to go to a high level. This issues a ground level hold to the encoder setting up the readout inhibit condition. The next PVS negative transition will set the flip-flop causing the Q (PIN-5) to go high. Thirty-one microseconds later a second negative transition of the 32 kHz PVS will shift the high level into the second 7474 (PIN 9 goes high), finally causing the ready command (read, -6 V DC) to be issued to the computer at output pins D and 4 on the card. When the computer has read the position data into the input register, the hold is removed thus, allowing the readout inhibit to be removed when the next negative transition of PVS occurs.

The rest of card 2 is devoted to the REF and PVS buffers and 50 ohm line drivers to the electronic tachometer system. The high impedance line receivers (chip M) drive hex inverters coupled to 50 ohm line drivers L and K.

Card 3 shown on schematic 4 is another level shifter but characterized for driving lamps in the remote display by current sinking to -12 V DC. The buffers are non-inverting electrical sense but inverting logical sense.

Card 4 of the Baldwin encoder interface box is a miscellaneous card providing room if expansion is necessary. All power supplies are wired to this card. Presently only a fuse and fan motor thermostatic switch are contained on this card. The schematic 5 shows this card and also the temperature monitor circuit. The simple circuit operates from a Fenwal thermistor located in the Baldwin encoder. The rest of the circuit is in the interface box. The 1 K current limit resistor (to 5 mA) and meter are connected in series with another meter and toggle switching arrangement located in the local independent position readout chassis, allowing the encoder temperature to be monitored remotely.

Schematic 6 is included for convenience (since it is not shown elsewhere) of the Wayne George remote lamp display. Twenty lamps connected to 1.5 K ohm "keep warm" resistors and diodes for isolation provide a monitor of the encoder binary position output.

The W/G to B/E modulator card that replaced the old 400 Hz modulator card in slot 423 of the Wayne George encoder electronics box is shown in schematic 7. The oscillator is a 9601 monostable operated in the astable mode. The 256 kHz oscillator circuit is stable to 1 percent over normal operating temperature range so that a crystal oscillator was not required. If the frequency drifts about 15 percent, then the 128 kHz constant phase bandpass filter output will not be useful. The oscillator drives a divide by two (chip B) coupled to exclusive OR circuits forming a timing generator producing two phase signals operating in quadrature. One exclusive OR operates as a simple inverter (C-4) since it has one input connected to +V. C-3 deocdes the clock and divide by two output into a 90° phase shifted signal. C-3 and C-4 are coupled to FET driver circuits E, producing FET drive signals A and B, thus operating analog switches K to sample the sine and cosine signals present at card pins 10 and 7 through low pass filters. The analog switch signals are summed at the bandpass filter L, producing a phase variable sinusoidal output relative to the chopper drive signals. This sine wave signal is

coupled to the analog comparator producing a square wave output level shifted to TTL logic levels. This square wave frequency is divided by 4 to normalize the Wayne George sin/cos track speed (32,768) to the Baldwin sin/cos track speed (8192). Finally, the PVS is coupled to 50 ohm line drivers N to produce the differential line driven signal to the electronic tach. The REF signal to the tach is produced from EX-OR (C-4) through the divide by 4 (B) to line drivers (M) at pins 16 and 17. Thus, the two signals REF and PVS are produced and may be phase/frequency compared by the electronic tach producing a velocity signal.

Schematic 8 shows the electronic card interconnections and signal flow for the electronic tachometer system. There are 3 pairs of cards 1 and 2 — two active sets and one spare set that may be switched in place of a defective active channel by use of a selector switch on the front panel. The numbering format of this switch is shown in schematic 8. The selector switch is complex with 33 poles to provide isolated switching for all signals into and out of the pair of cards.

Schematic 9 shows the digital circuit card 1. All switching control signals are produced on this card. Signals present in the digital card are shown in Figure 8.

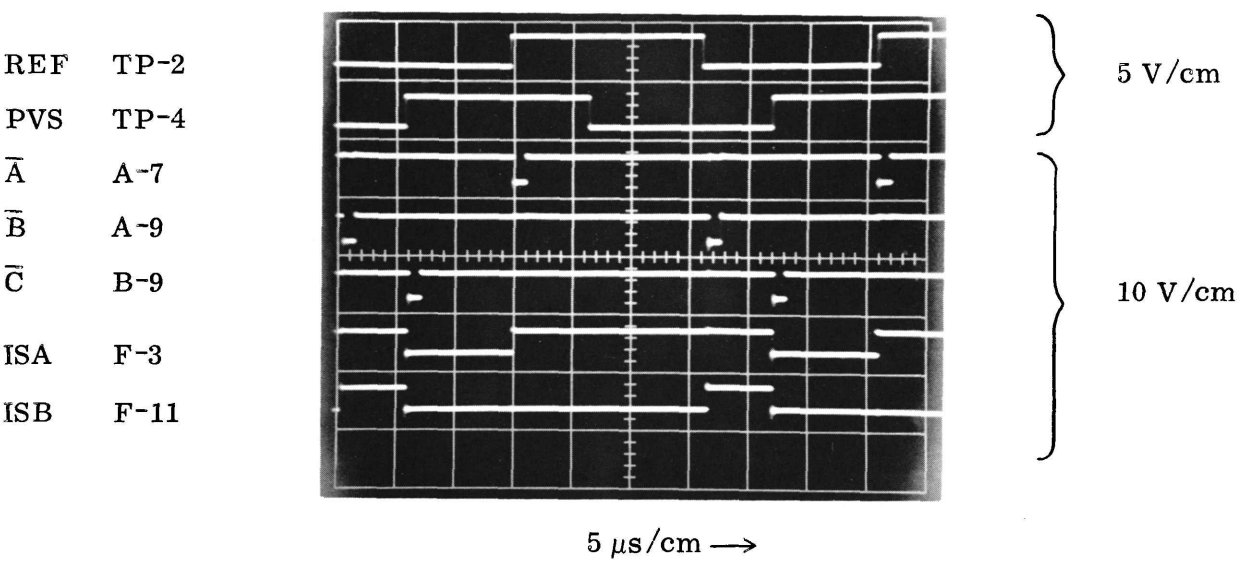


Figure 8 — Phase Comparator Signals present in the Digital Card with Position Set to 40 arc seconds and Zero Rate

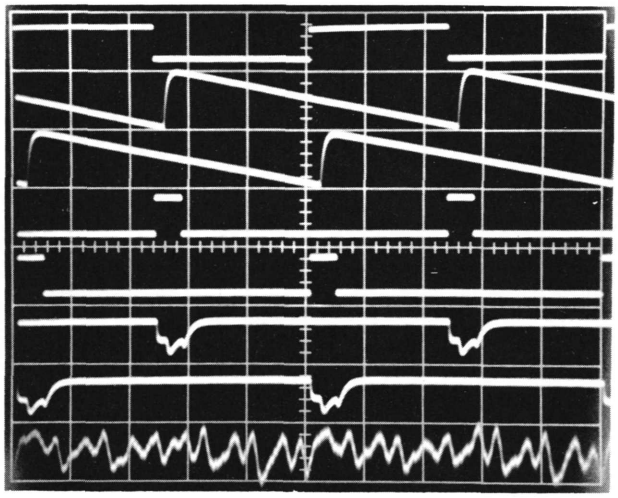
The 32 kHz REF and PVS buffered by K-6 and K-8 are shown in the upper two traces. Rising edges of these waveforms cause $\overline{A}$ and $\overline{C}$, respectively, while $\overline{B}$ is caused by the falling edge of PVS. $\overline{A}$, $\overline{B}$, and $\overline{C}$ are the outputs of one shots A-7, A-9, and B-9 that are coupled to set/reset flip-flops F-3 and F-11, output waveforms of which are shown in the two bottom traces of Figure 8. The phase detector outputs are duty factor variable as a function of position. These two signals are coupled to the low pass filters and differentiators on the analog card.

The 0° and 180° phase detectors are NAND gates L-6 and L-3, respectively coupled to one shots A and B. The channel switch flip-flop is L-8, and L-11 in schematic 9. Also see Figure 7. The flip-flop controls via the drivers CFA and CFB the FET's on the analog card which select the channel to be coupled to the output shown in schematic 10.

Six discrete driver buffers are found along the right side of schematic 9. CFA and CFB are the FET drivers mentioned above. CSA and CSB are light emitting diode (LED) indicator drivers coupled to the respective front panel indicators for channel switch status. AC and BC are blanking FET drivers buffering to ± 15 volt swing the signals from the retriggerable one shots C-6 and C-10. The PFI and RFI are differentiator-integrator combinations sensing the presence of PVS and REF signals providing PVS fail and REF fail indications coupled to front panel LED indicators.

Schematic 10 shows the circuits on the analog circuit card. The signals ISA and ISB are the inputs to the card that are duty factor variable coded position data. These waveforms are averaged by low pass filters K and L, thus producing a DC voltage output that is a function of position and ramp (sawtooth) waveforms for constant rate of telescope motion. The diode current switch input to the low pass filter insures stable current input levels to the low pass filter that is not obtainable directly from the digital IC (F-3 and F-11) of the digital card. Figure 9 below shows the principal analog signals present on the analog card for constant rate. The top trace is the channel switch. When it is high, channel A (traces 2 and 6) is active and when low channel B (traces 3 and 7) is active and coupled to the rate output (bottom trace). The glitches in traces 6 and 7 are caused by blanking traces 4 and 5 and retrace of the phase comparators, traces 2 and 3. The rate output (trace 8) is shown with a very sensitive scope setting (.05 V/cm AC coupled) to show noise content. The DC voltage level indicating rate is about 10 volts and the noise shown is about .05 volts, producing a signal-to-noise voltage ratio of

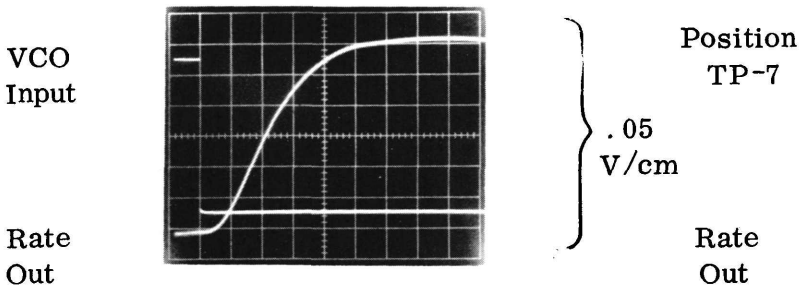
CS	TP-6	1 V/cm
Position-A	TP-7	5 V/cm
Position-B	TP-8	5 V/cm
Blanking-AC	V-18	50 V/cm
Blanking-BC	N-12	50 V/cm
Rate-A	C-out	20 V/cm
Rate-B	H-out	20 V/cm
Rate Out	TP-9	.05 V/cm (AC coupled)



10 milliseconds/cm ⟶

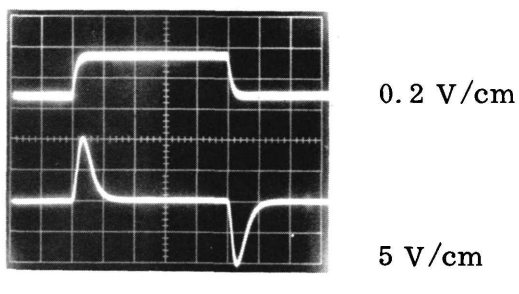
Figure 9 — Principal Analog Signals present in the Analog Card with Constant Rate Equal to 26°/minute.

of about 200 (46 dB). Notice that channel switching transients are practically non-existent. Some or most of the noise in trace 8 may be produced by the test apparatus in the form of phase jitter type noise. The test apparatus comprised a crystal oscillator for REF and frequency synthesizer for PVS. The rate produced is a function of the difference in frequency between the two sources. In this mode the tachometer functions as an FM demodulator. Figure 10 shows the rate step response produced by operating



2 ms/cm ⟶

Figure 10 — Rate Step Response



10 ms/cm

Figure 11 — Rate Impulse Response

the frequency synthesizer as a VCO. The scope is DC coupled. Note that the noise level as well as the rate is much smaller than that in Figure 9. The rate change step is about 0.3°/minute. Notice also that the rise time for this combination is about 4 ms. The rate impulse response of the tach is shown in Figure 11. The position step is about ± 15 arc seconds. The low pass filter (position, upper trace) has a rise time of about 2 ms. The rate impulse reaches about 10 volts during this interval. The test was performed by coupling the tach to one of the WG to BE modulator converter cards and applying 3 V DC to the sine analog input. A 10 Hz square wave was applied to the cosine input and adjusted in amplitude to produce the step position response as shown in Figure 11.

The NRAO telescope position readout converter is comprised of two channels — one for azimuth and one elevation. Pictures may be found in section 10 and schematics in section 11. Schematic 11 gives the circuit card interconnection diagram for the azimuth channel. The 12-bit binary position code from the azimuth encoder is coupled to the level translator card as shown in the upper left corner. The position code is level shifted and coupled to the D/A converter producing an analog output that is scaled by the resistor divider network and then coupled to the digital panel meter providing the decimal readout in degrees. An unscaled analog output (0-10 V) as a function of position is available at both front and rear BNC connectors. The calibration test switch forces the readout to the indicated values (000.7 and 359.9) for calibration purposes.

Schematic 12 for the elevation channel is similar to schematic 11 for azimuth except for the scaling network, the decimal point connection (PI-A) on the DPM, and the calibration switch which is triple pole instead of double pole.

Schematic 13 is the level translator card 1 for the azimuth channel. The position code is converted by the level translators from 3-C (0, -6) negative logic levels to TTL (0, +5) positive levels using DM 8820 integrated circuits. The inputs Y and Z at the bottom of the drawing are inputs from the calibration switch. Through resistor logic controlled by these inputs (Y and Z), the readout is forced to the code considered optimum for calibrating zero and gain of the DPM as selected by the calibration switch.

Schematic 14 is the elevation level translator card and is similar to the azimuth level translator except for logical sense and the calibration switch logic which is more complex with three controls, X, Y, and Z, that selectively force the level shifters to output codes considered optimum for DPM calibration.

The D/A converter is the same in both azimuth and elevation channels and is shown in schematics 15 and 16 which are reproductions of the manufacturer's specification sheet. The D/A converter is a non-potted unit allowing field repair should trouble develop. The D/A card contains IC current switches, resistor network and IC output op-amp and voltage reference, but does not contain the optional input register IC's.

No schematics for the DPM are presented. It operates by means of the dual slope method. If trouble develops, the unit may be sent as a unit to the factory for repairs. A list of the DPM rear connector functions is presented in section 14, connector lists.

An encoder temperature monitoring circuit is built into the readout system. Schematic 5 shows the circuit in the Baldwin encoder interface box. Schematic 17 shows the switching circuit and indicator included in the local readout chassis. Schematic 18 shows the temperature circuit in the Wayne George electronics box.

Two operational amplifiers were changed in the Wayne George encoder electronics package to improve temperature stability of the encoder. These circuit changes were made to the sin/cos preamplifier card 417 as shown in schematic 19. The P-501 was added requiring the zero adjust pot circuit to be changed and a 15-22 picofarad capacitor to be added. The new op-amp dramatically improves the temperature stability of the system. This instability in the past greatly affected the accuracy and reliability of the 5 LSB synthesis circuits.

The computer addition required to allow the local readout to function when the computer is not reading position is shown in schematic 20. Gates A and B form a flip-flop that causes the PIL and inhibits the encoder hold commands via gates C, D and E when it is reset by the master clear. When master clear is depressed the encoder and thus the coarse readout is "unfrozen" when a program runs on the computer that reads position the flip-flop (gates A and B) is set allowing the PIL to be removed and encoder hold commands to be enabled, allowing normal program operation.

7. IN CASE OF DIFFICULTY

In the event difficulty is realized in operation of the telescope drive system, it should be possible to repair it in quick time since a "systems" approach in packaging has been employed. Only a few spare cards are required since some redundancy is present. To repair the system it is only necessary to determine which card has the fault by some means such as "card snatching". In some cases a selector switch is available, allowing a spare to be switched into a defective channel, allowing very simple and speedy repairs, deferring the actual troubleshooting operation until maintenance day.

A more logical approach to troubleshooting the system is to become familiar with the function of each of the different electronic cards in the system. A tabulation of this follows.

Quan.	Baldwin Encoder Interface Box	Slot
2	Inverter Card 0	0
2	Computer Buffer Card 1	1
2	Encoder Control Card 2	2
2	Remote Display Buffer Card 3	3
1	Miscellaneous Card 4	4

Wayne George Encoder Electronics Box

3	W/G to B/E Rate Modulator	423

Electronic Tachometer System

3	Digital Card 1	A1, S1, E1
3	Analog Card 2	A2, S2, E2

Coarse Telescope Position Readout

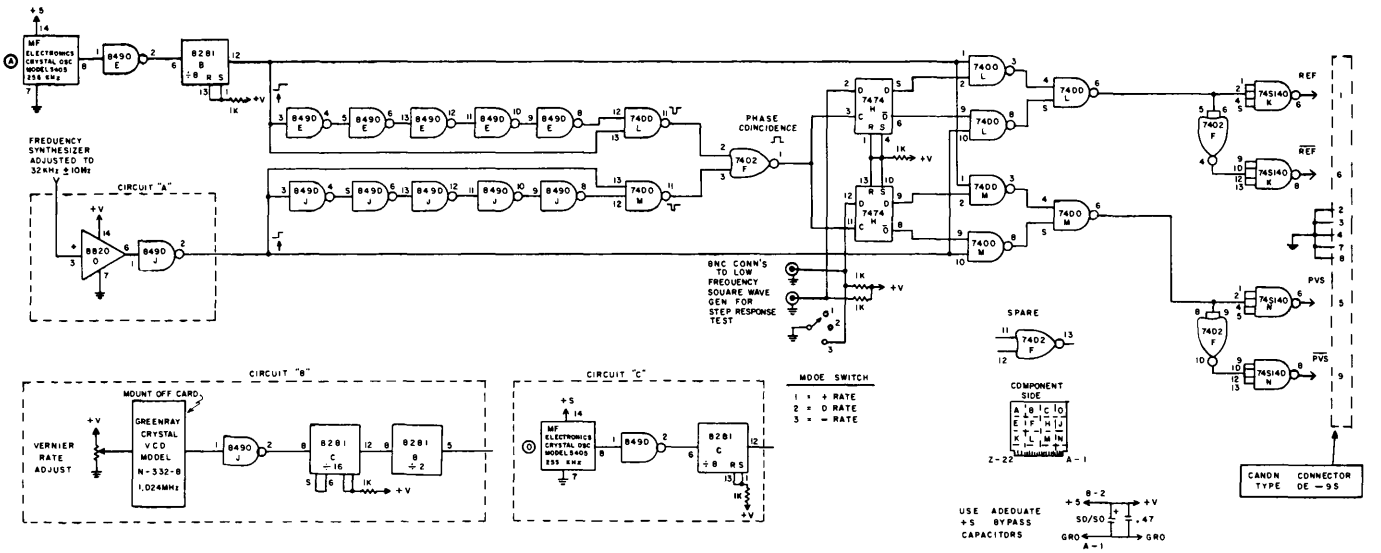
1	Azimuth Interface Card 1	1
2	D/A Converter Card 24	2, 4
1	Elevation Interface Card 3	3

DDP-116 Computer Additions

1	DJ-30 NAND Gate Card	?

As an aid to troubleshooting and encoder indexing, a Douglas card containing 20 LED lamps and jumper cables for connection to J-2 (computer data) and J-5 (remote display) is available. The lamps light-up when the data is a logic "1". The Baldwin encoder also has a rear mounted LED display. Here a logic "0" is indicated when the lamp is lit.

A test jig is suggested for use in repairing the electronic tach system, a schematic of which is shown in Figure 12.



ELECTRONIC TACH TEST SET
FIG. 12

The test set is not a necessity since the tach system may be repaired "on-line". But, more predictable results are obtained in "open loop" performance using the circuit of Figure 12. The circuit requires 10 integrated circuits and two oscillators which may be packaged on a Douglas 11-DE-1 circuit card as shown. The test set is essentially two oscillators that may be selectively coupled, via the mode switch, to either the REF or PVS or both during phase coincidence as determined by the phase detector at chip F-1. Oscillator "A" is an inexpensive crystal oscillator which functions as an LO. Circuits A, B, and C are circuit suggestions providing the FM. If a frequency synthesizer is available then circuit A is preferred. The tach rate output is adjusted by varying the synthesizer output by ± 10 Hz. Circuit "C" employs an oscillator identical to oscillator "A". This is the cheapest method providing only a ± K or zero rate as selected by the mode switch. K is set by the small difference in frequencies of the two oscillators A and D due to differences in manufacturing tolerances. A test rate of a few degrees per minute may be expected using this scheme. Other variations of Figure 12 may be developed according to the preference of the troubleshooting. The important thing is to use crystal oscillators for rate stability, otherwise the rate output may contain a high noise level due to phase jitter of non-crystal oscillators.

CALIBRATION

The Baldwin encoder interface box requires no calibration. The W/G to B/E modulator card oscillator frequency is set so that the reference frequency at TP-4 on the electronic tachometer front panel is 32 kHz ± 10%. It is unlikely that the frequency will ever drift out of this range. The frequency is set by adjusting the trim resistor (higher value of the two resistors connected to pins 8 and 13, chip A) on the W/G to B/E modulator card. The crystal oscillator employed in the Baldwin encoder also affects this frequency but no adjustments are necessary.

There are two adjustments per axis available in the electronic tachometer — gain and balance. Both pots are found on the analog card. The gain pot (location N) sets the scale factor (transfer constant) and may be set using the rate indicator and the test set of Figure 12 with a frequency synthesizer. First adjust the synthesizer for zero rate as seen on the tach rate indicator. Then add 10.00 Hz to the synthesizer frequency and adjust the tach gain pot (slot N) for a rate output of 26.37 degrees/minute. Monitoring the rate output as done for Figure 9 by synchronizing the scope on TP-6 (channel switch) and AC coupling the rate to the scope will provide an indication of channel balance which may be adjusted by the pot located at slot "B" on the analog card. If the balance is misadjusted, then a difference in gain between channels A and B will exist and may be noted as a square wave with transitions coincident with the channel switch. It is not expected that any of these adjustments will ever drift under normal use.

The calibration of the 12-bit position readout is expected to drift and hence was designed for ease of adjustment. All that is necessary is to connect the system for normal operation and then using the toggle switches above the DPM's, the adjustment screw below the toggle in the direction in which the switch is thrown may be adjusted for the proper reading as shown opposite the toggle. Best results are obtained by adjusting the low reading first, followed by the high reading.

8. CONCLUSION

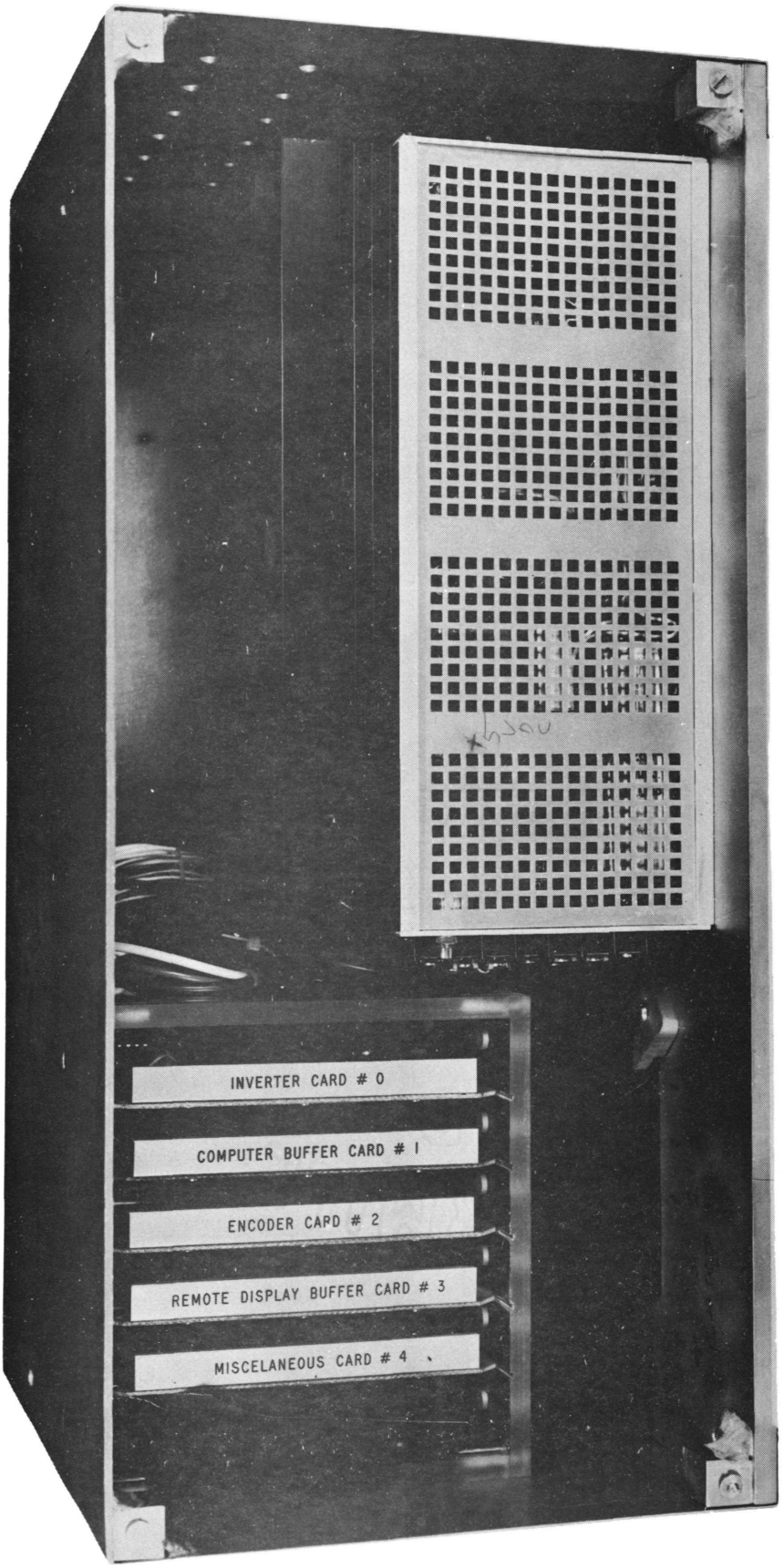
The systems described herein were designed and built to provide reliable service and ease of maintenance. The various systems were laboratory tested under worst case operating extremes. The Baldwin optical shaft encoder will operate over a temperature range of 20 °F to 150 °F. The encoder interface box will operate over a range of -20 °F to +150 °F.

The electronic tachometer system response time, considering proper design for each case, is a direct function of the REF frequency with improvement at higher frequencies. The REF is, however, fixed for a given encoder. The tach circuits may be simplified in future designs by eliminating the blanking circuits in favor of resistor divider networks that limit the signal to the channel switching FET's to less than the FET pinch off voltage subtracted from +V, thereby providing the same result as the blanking circuits. Finally, care should be exercised in selecting capacitors with stable characteristics since considerable trouble was caused by this simple mistake when capacitors employed in the differentiator circuits had capacitance values that varied as a function of the potential between the plates.

9. CREDITS

Ron Weimer	-	helpful consideration and suggestions concerning the circuits.
John Payne	-	suggestions concerning the servo system.
Baldwin Company	-	loan of breadboard 694BL shaft encoder and help in understanding the operation of the encoder.
Gene Wetmore	-	and others at the 36' site for aid in the installation of the system.
Jerry Turner	-	electronic assembly.
Staffan Olson	-	electronic assembly.
Ken Cantrell	-	electronic assembly.
Mechanical Engineering	-	new encoder mounts design.
Machine Shop	-	As usual, the Green Bank metal shop performed an impressive job in cutting and engraving the front panels, and cutting, machining, and fitting all the metal parts used in the mechanical assembly.
Tony Miano	-	drafting.
C. Dunkle	-	typing.
Gene Crist	-	photography and printing.
Ron Monk	-	photography and printing.

10. PICTURES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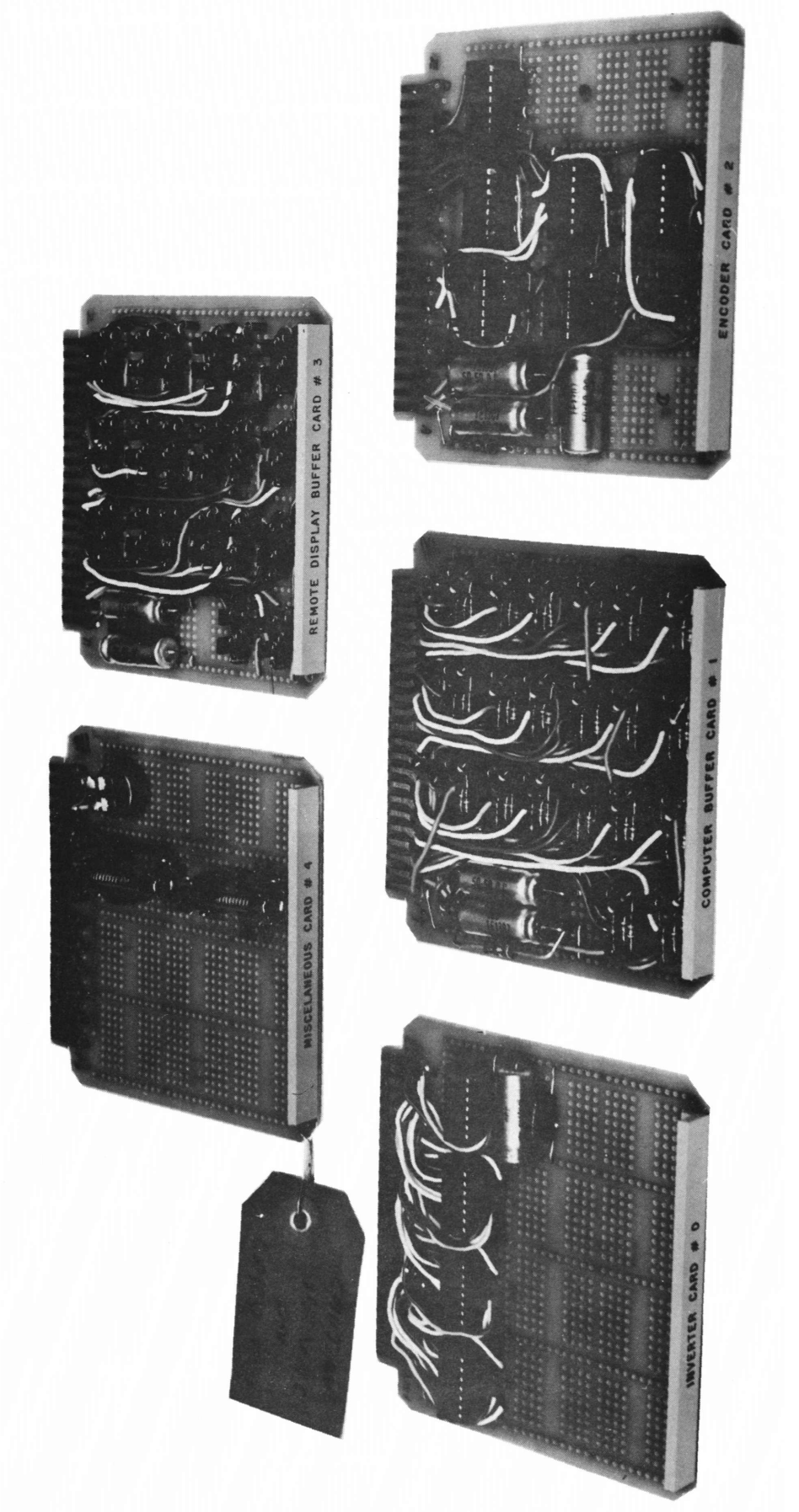
COMPUTER BUFFER CARD # 1
ENCODER CAPD # 2
REMOTE DISPLAY BUFFER CARD # 3
MISCELANEOUS CARD # 4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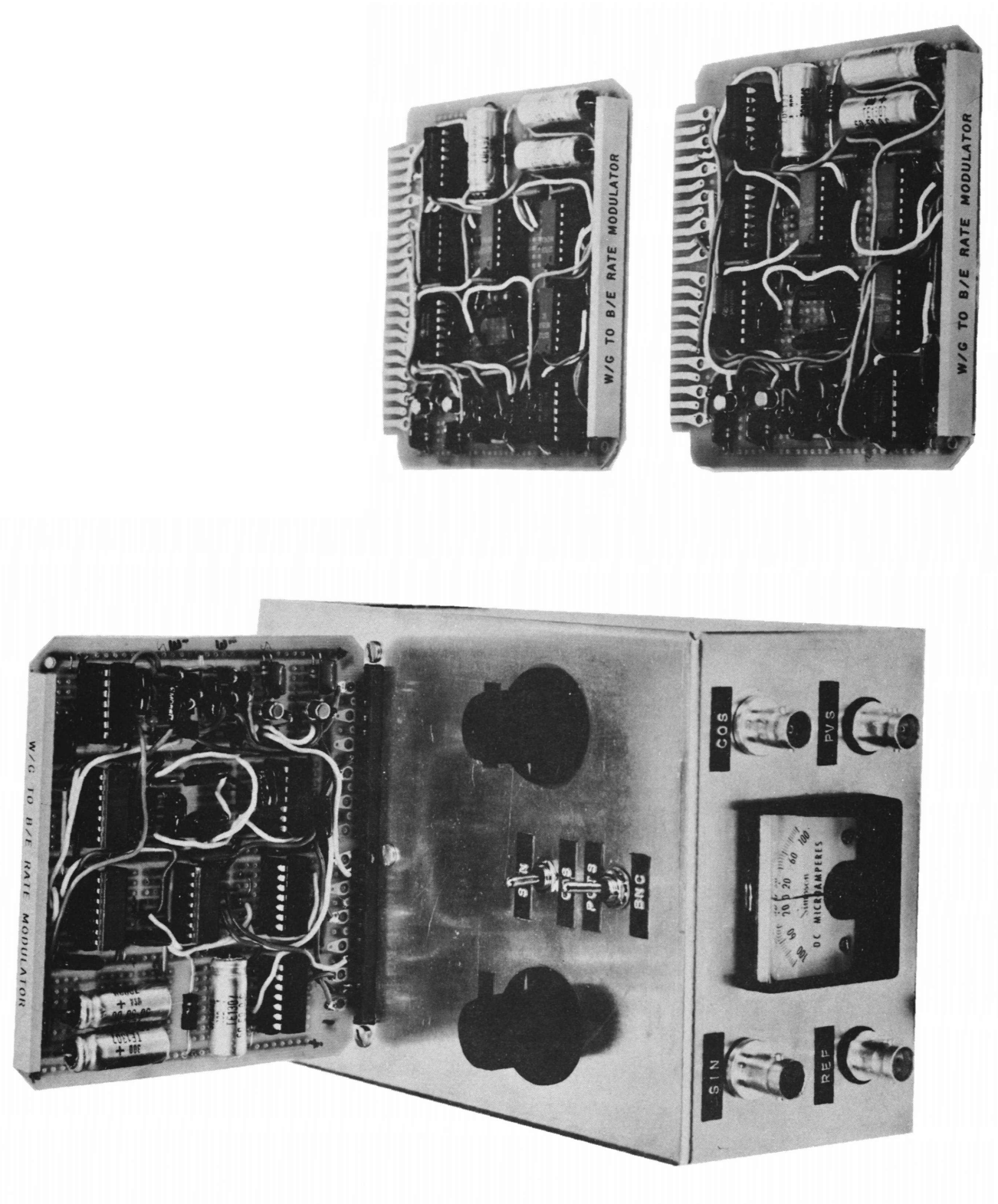
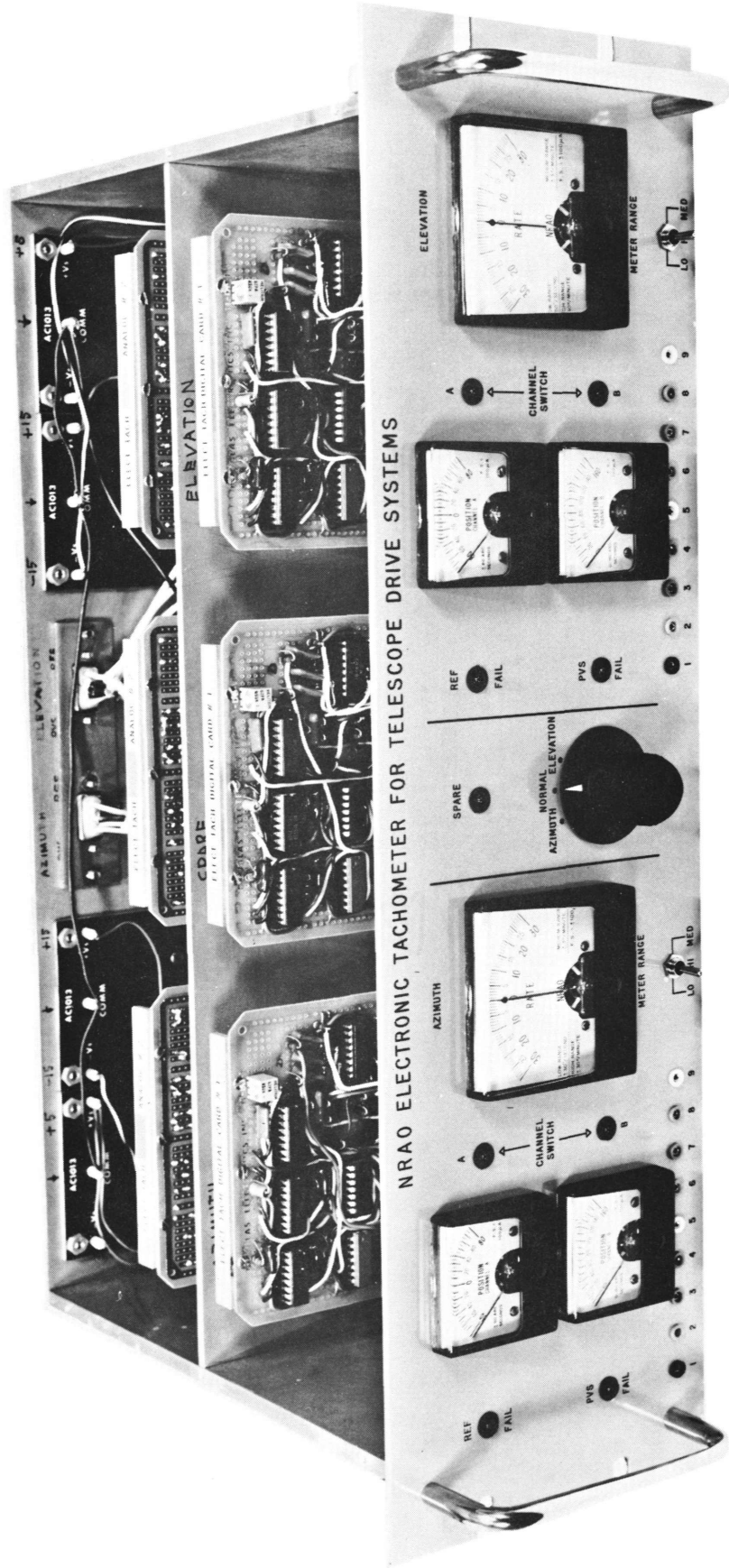
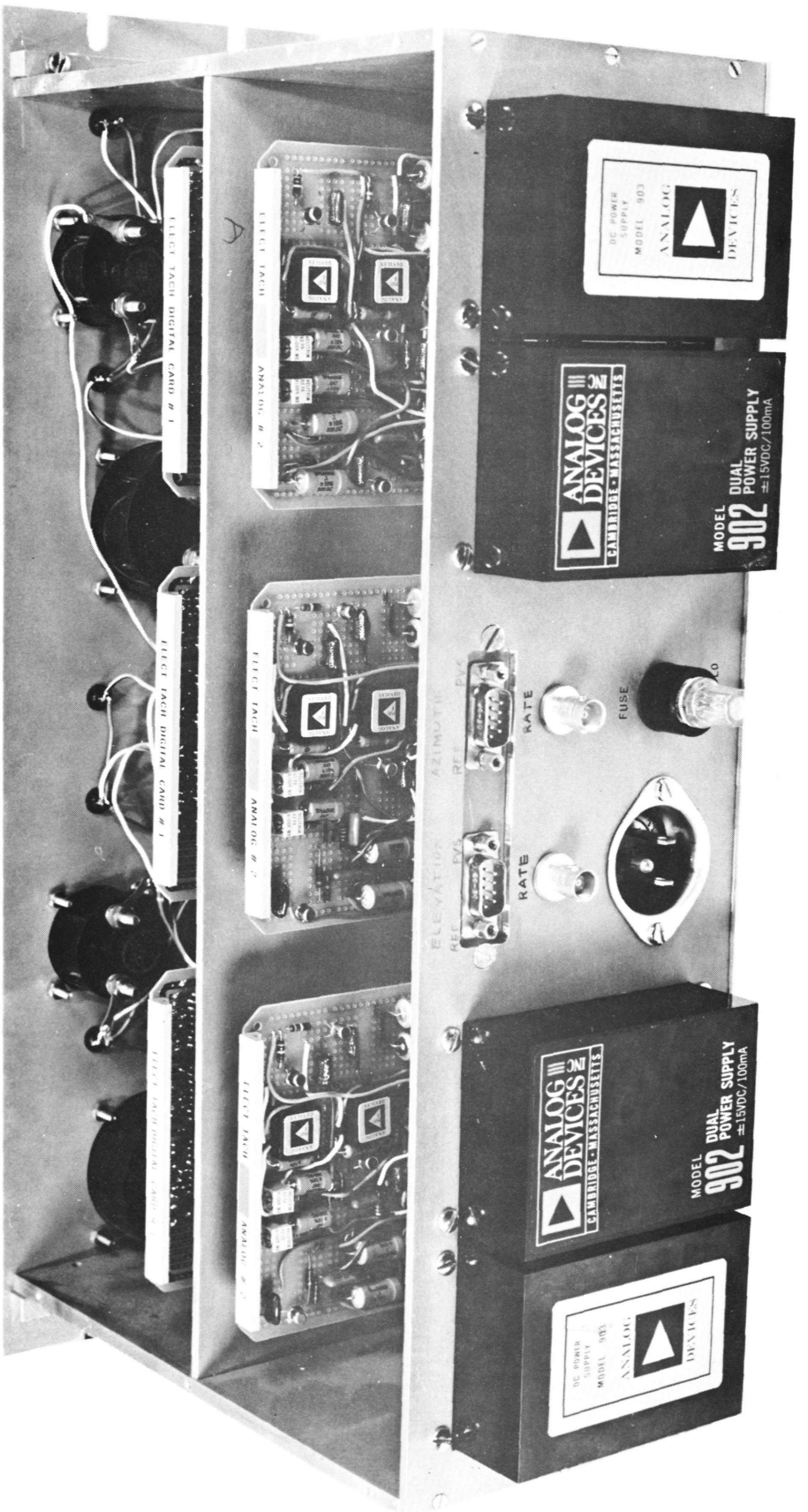
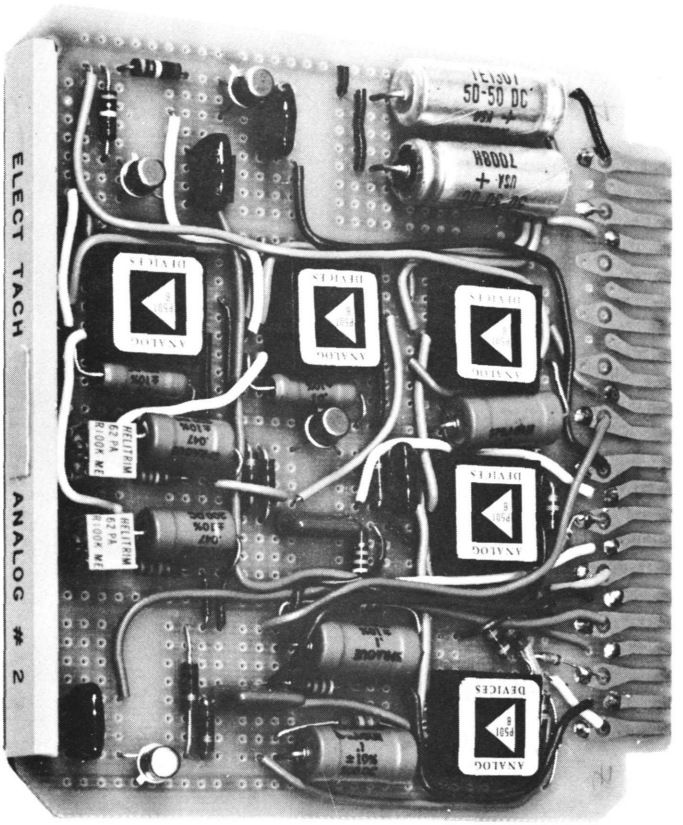
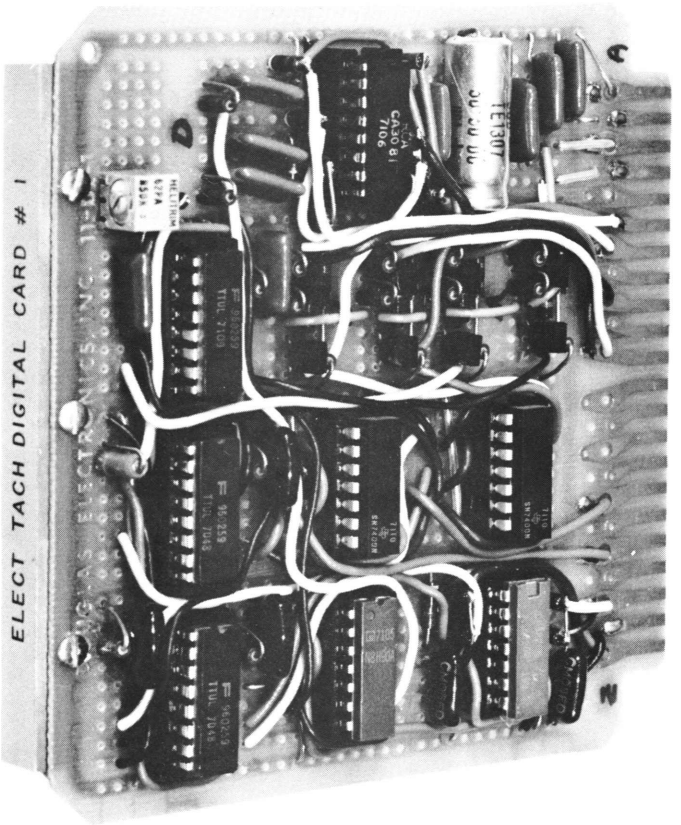
REMOTE DISPLAY BUFFER CARD # 3
COMPUTER BUFFER CARD # 1
MISCELANEOUS CARD # 4
INVERTER CARD # 0

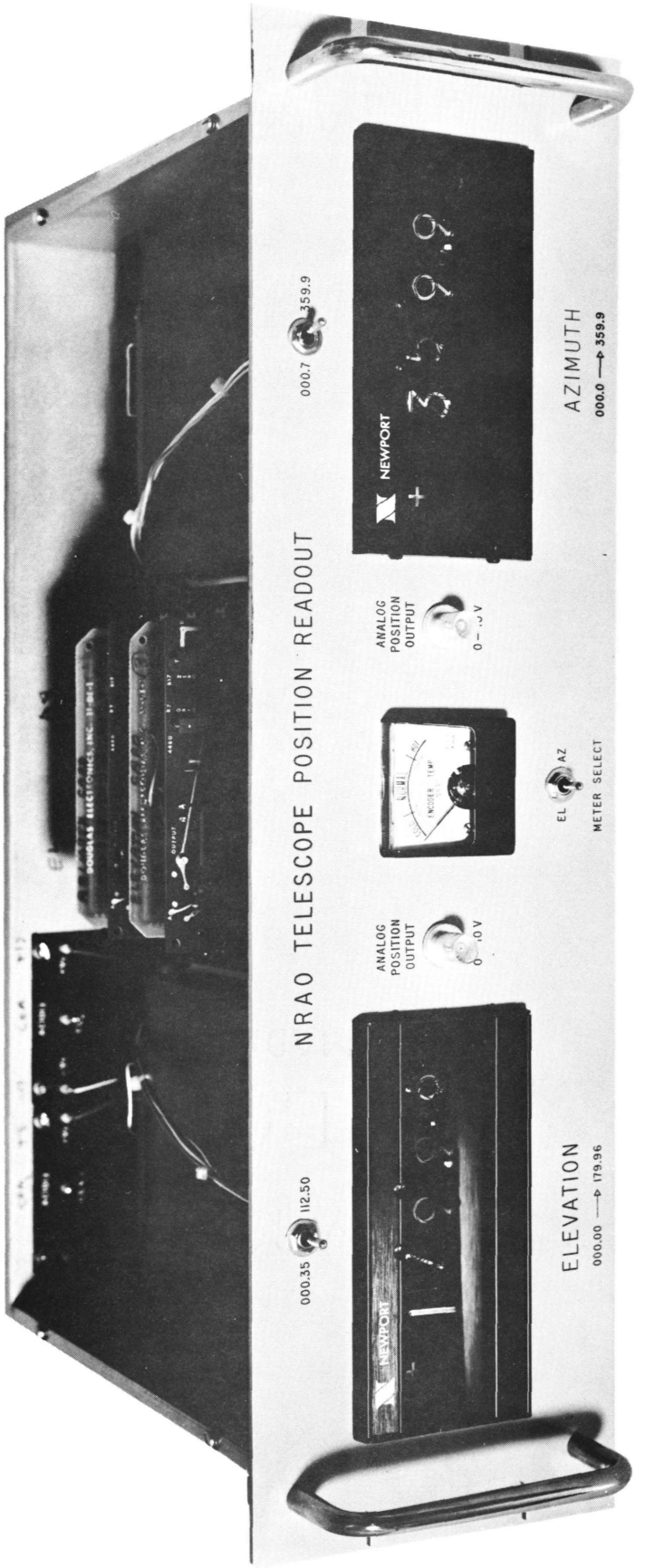

W/G TO B/E RATE MODULATOR
W/G TO B/E RATE MODULATOR
W/G TO B/E RATE MODULATOR
SIN
REF
COS
PVS
SNC
DC MICROAMPERES

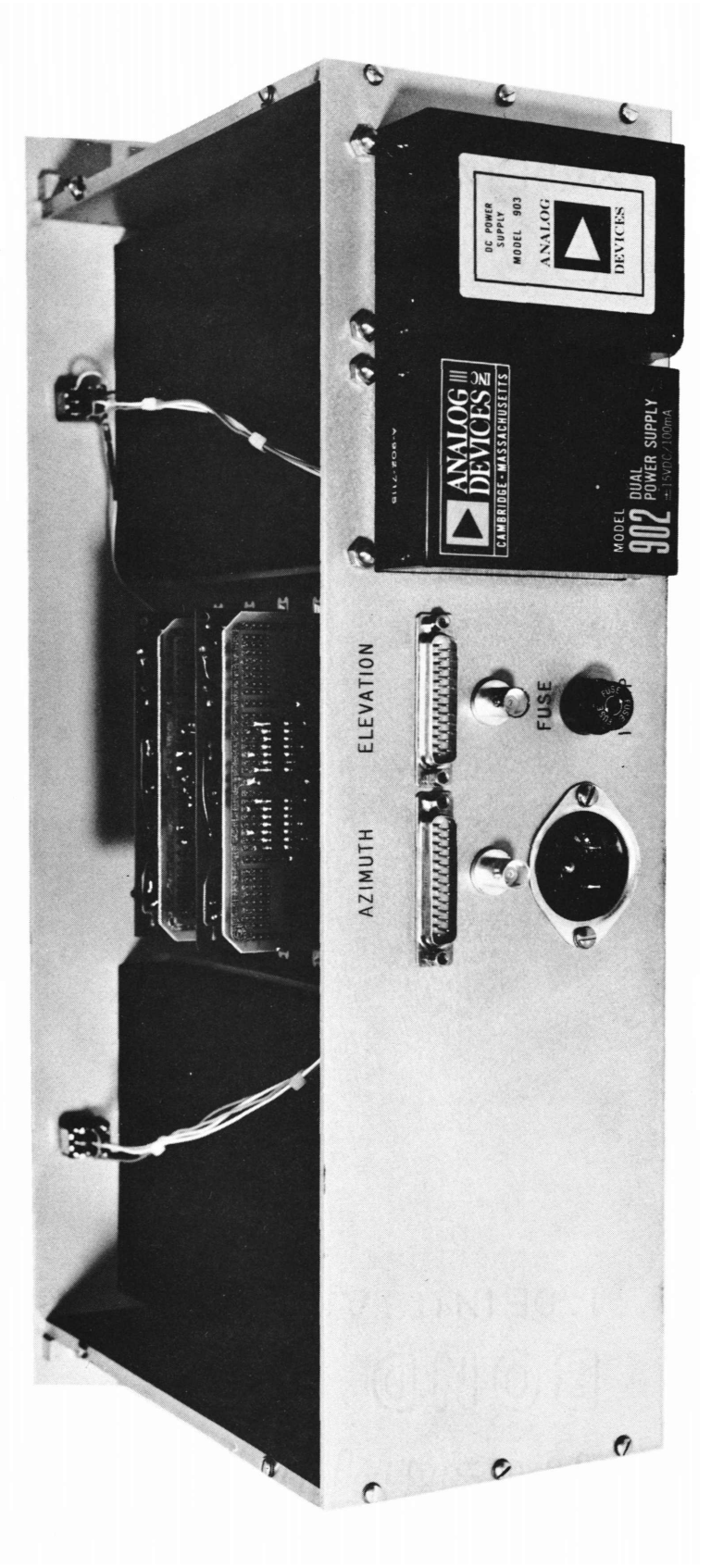

NRAO ELECTRONIC TACHOMETER FOR TELESCOPE DRIVE SYSTEMS
AZIMUTH
ELEVATION
REF FAIL
PVS FAIL
CHANNEL SWITCH
METER RANGE
SPARE
NORMAL
AZIMUTH
ELEVATION
LO
MED
HI

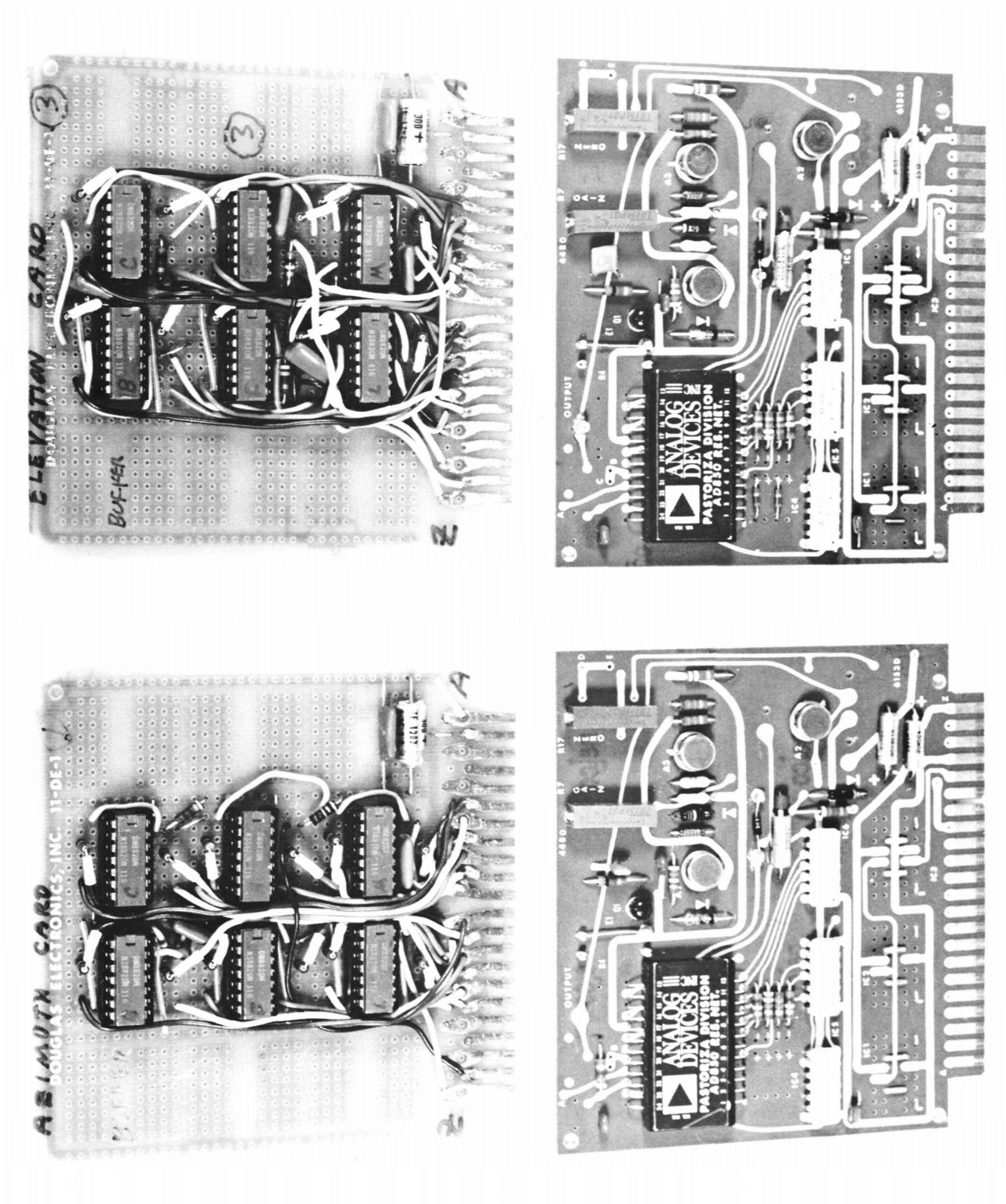

ELEVATION
AZIMUTH
RATE
RATE
FUSE
MODEL 902 DUAL POWER SUPPLY ±15VDC/100mA
ANALOG DEVICES
MODEL 902 DUAL POWER SUPPLY ±15VDC/100mA
ANALOG DEVICES
DC POWER SUPPLY MODEL 903
ANALOG DEVICES


ELECT TACH ANALOG # 2
ANALOG DEVICES

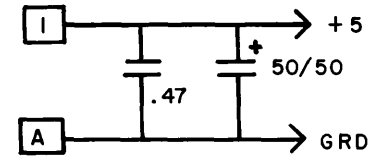

ELECT TACH DIGITAL CARD # 1


NRAO TELESCOPE POSITION READOUT
ELEVATION
000.00 → 179.96
AZIMUTH
000.0 → 359.9
NEWPORT
ANALOG POSITION OUTPUT
0 - 10 V
METER SELECT
EL
AZ
000.35
112.50
000.7
359.9

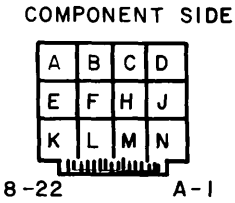

AZIMUTH
ELEVATION
FUSE
ANALOG DEVICES
CAMBRIDGE · MASSACHUSETTS
MODEL 902 DUAL POWER SUPPLY
DC POWER SUPPLY
MODEL 903
ANALOG DEVICES

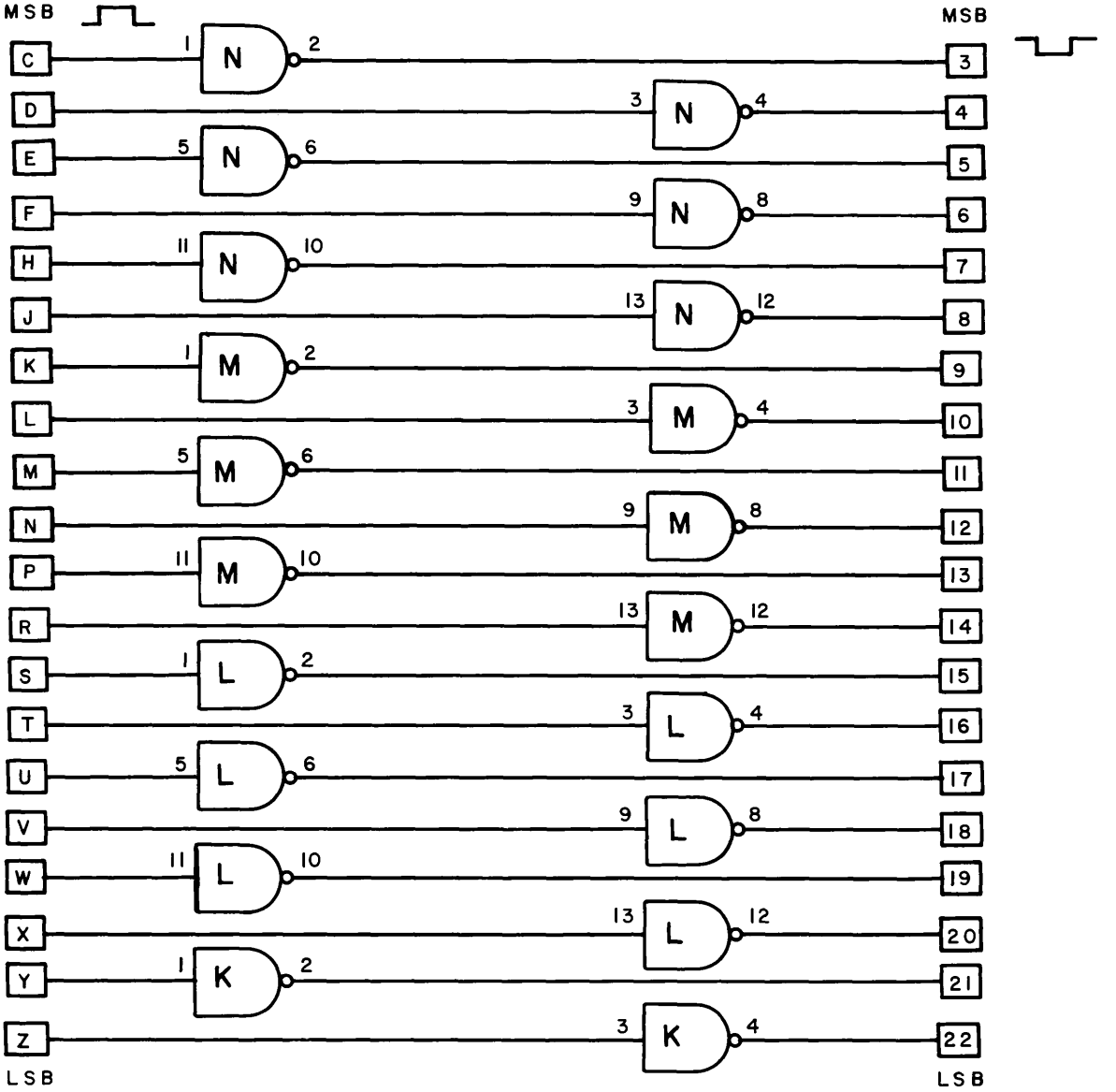

ELEVATION CARD
BUFFER
ANALOG DEVICES
PATENTED

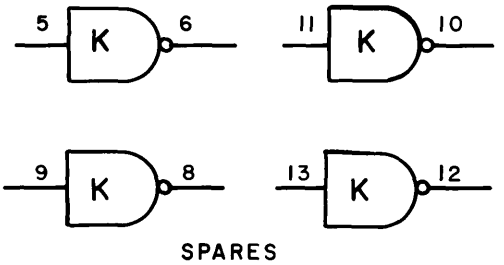
11. SCHEMATICS



ALL IC's 14 PIN
Vcc = PIN 14
GRD = PIN 7

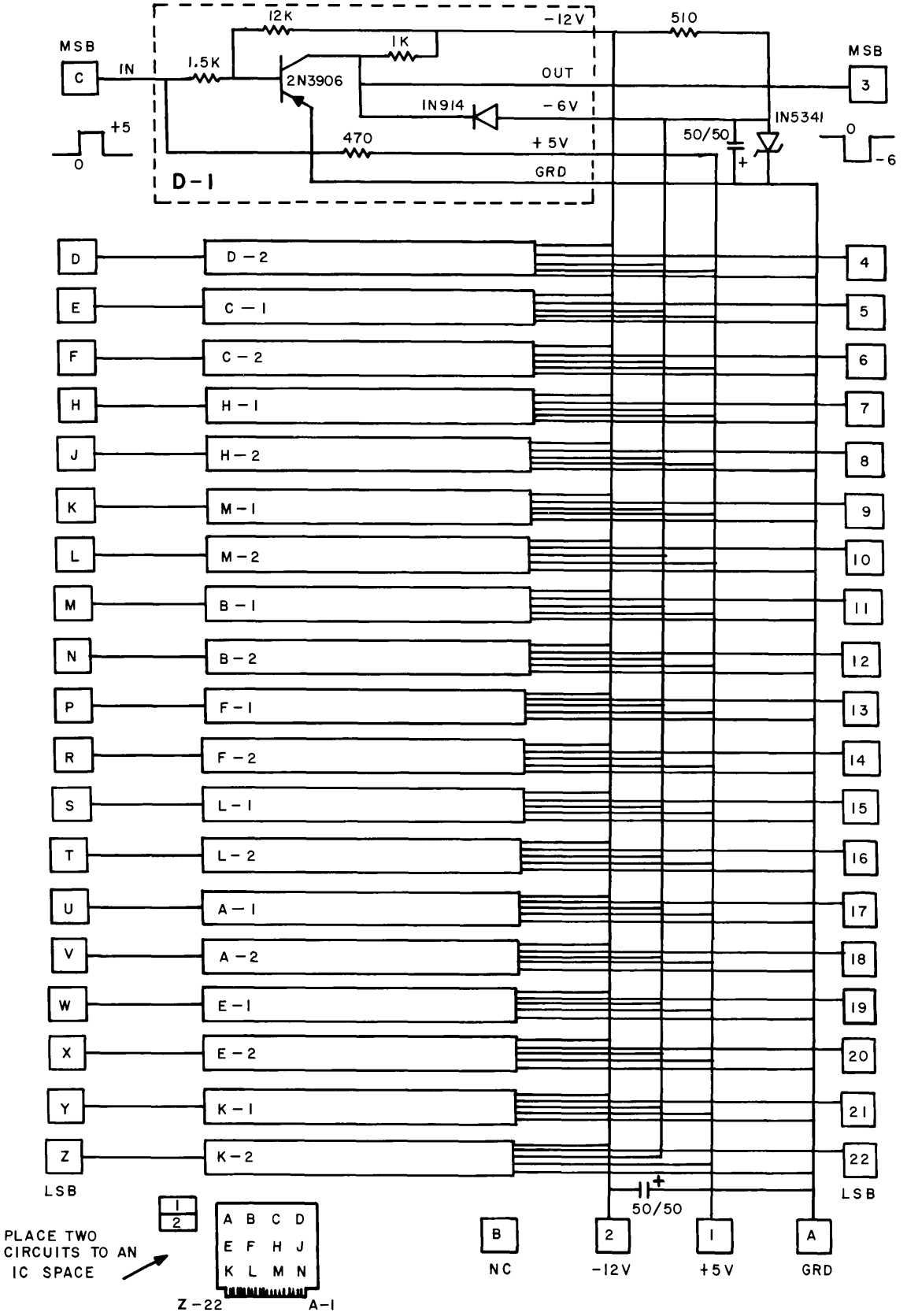






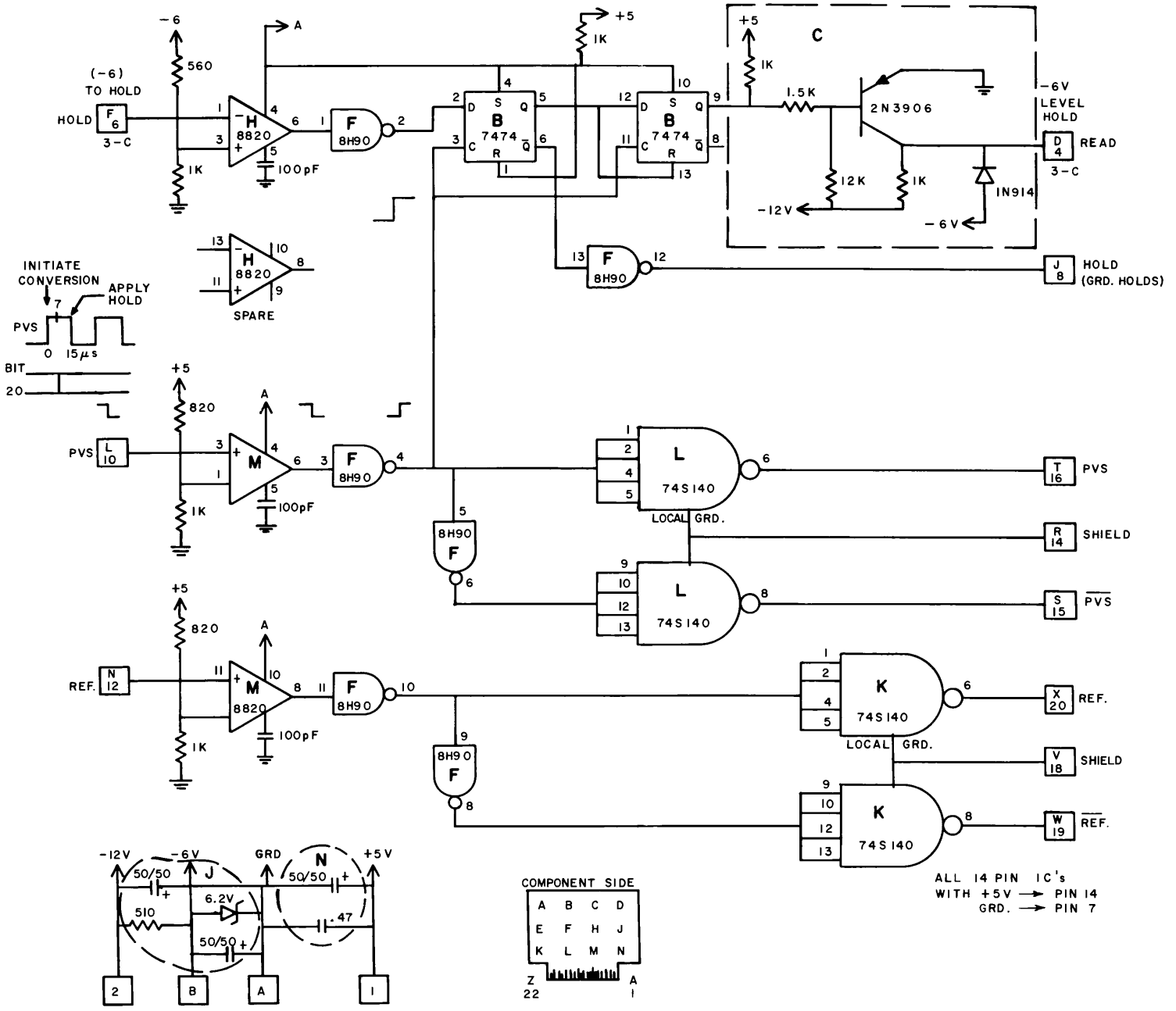
ALL CIRCUITS ARE
8H90 HEX INVERTERS

BALDWIN ENCODER INTERFACE
INVERTER CARD # 0
SCHEMATIC # 1

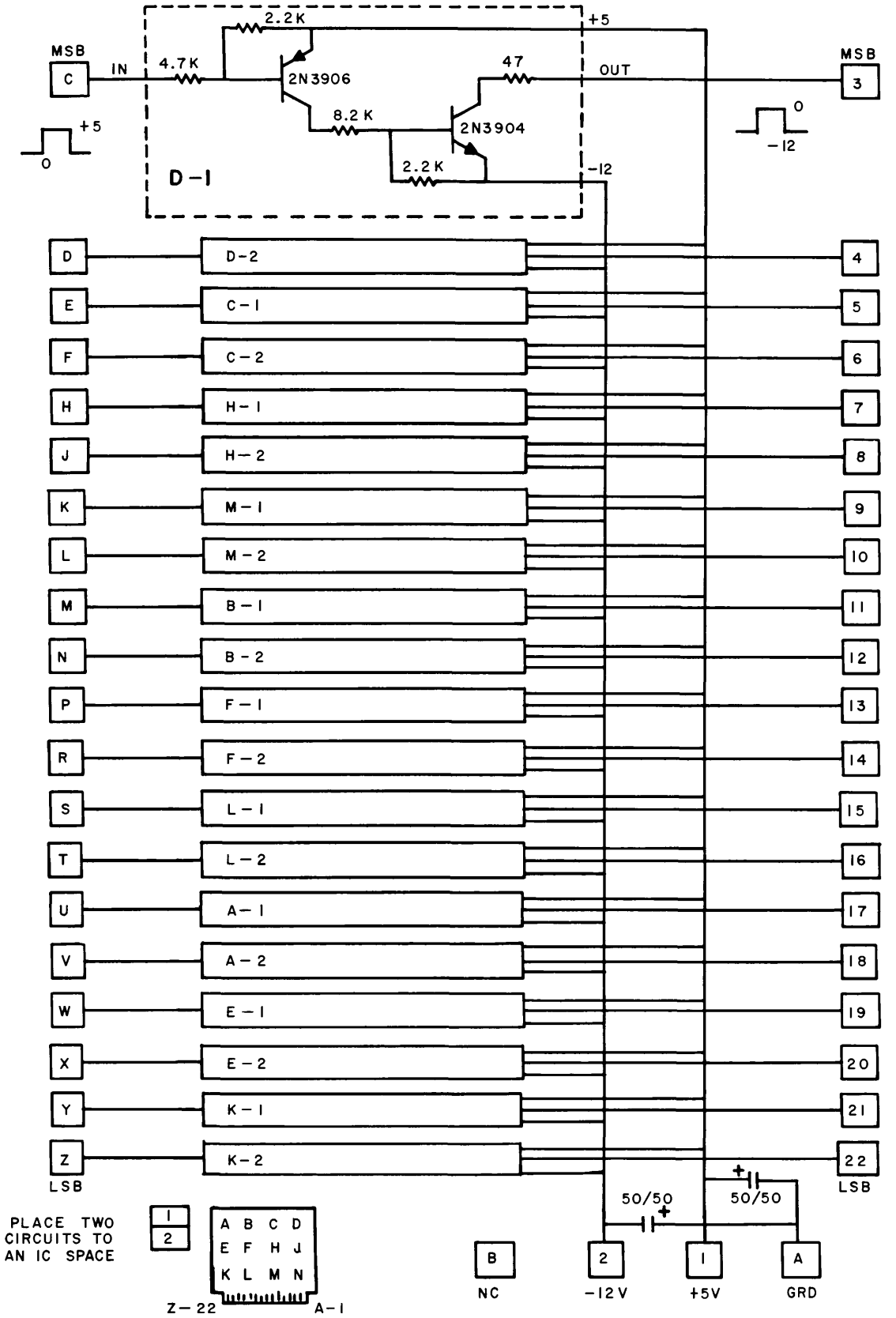


DATA OUTPUT TO COMPUTER BUFFER CARD # 1

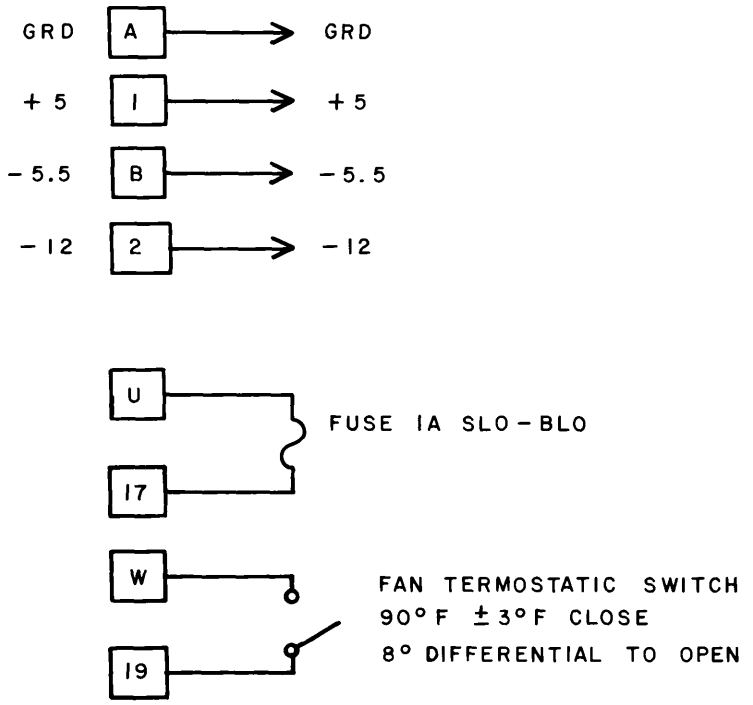
SCHEMATIC # 2



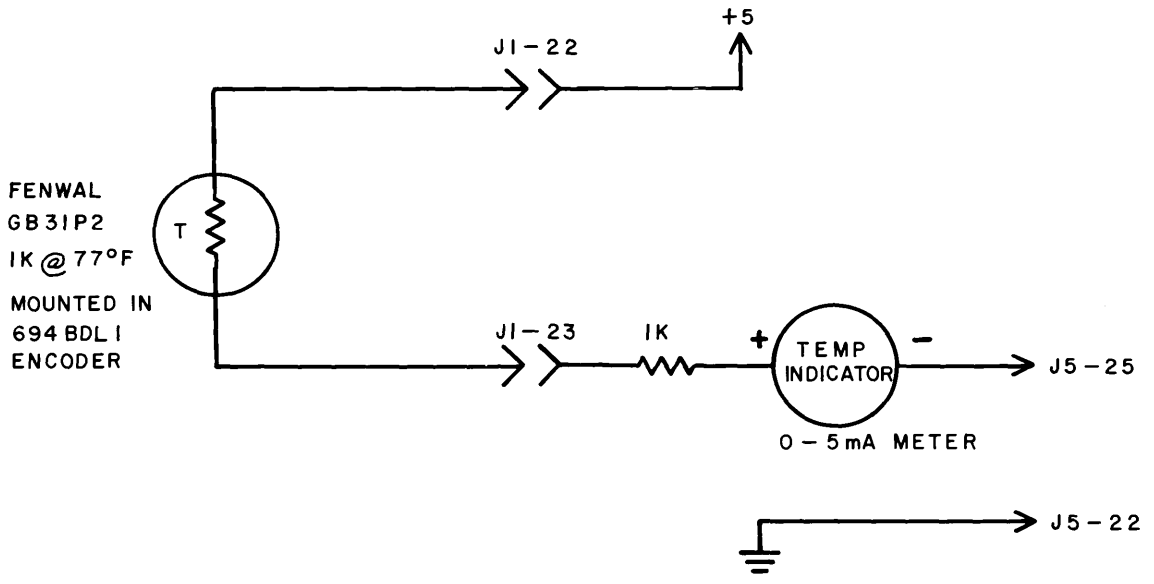
BALDWIN ENCODER INTERFACE
ENCODER HOLD LOGIC AND REF/PVS BUFFERS CARD # 2
SCHEMATIC # 3



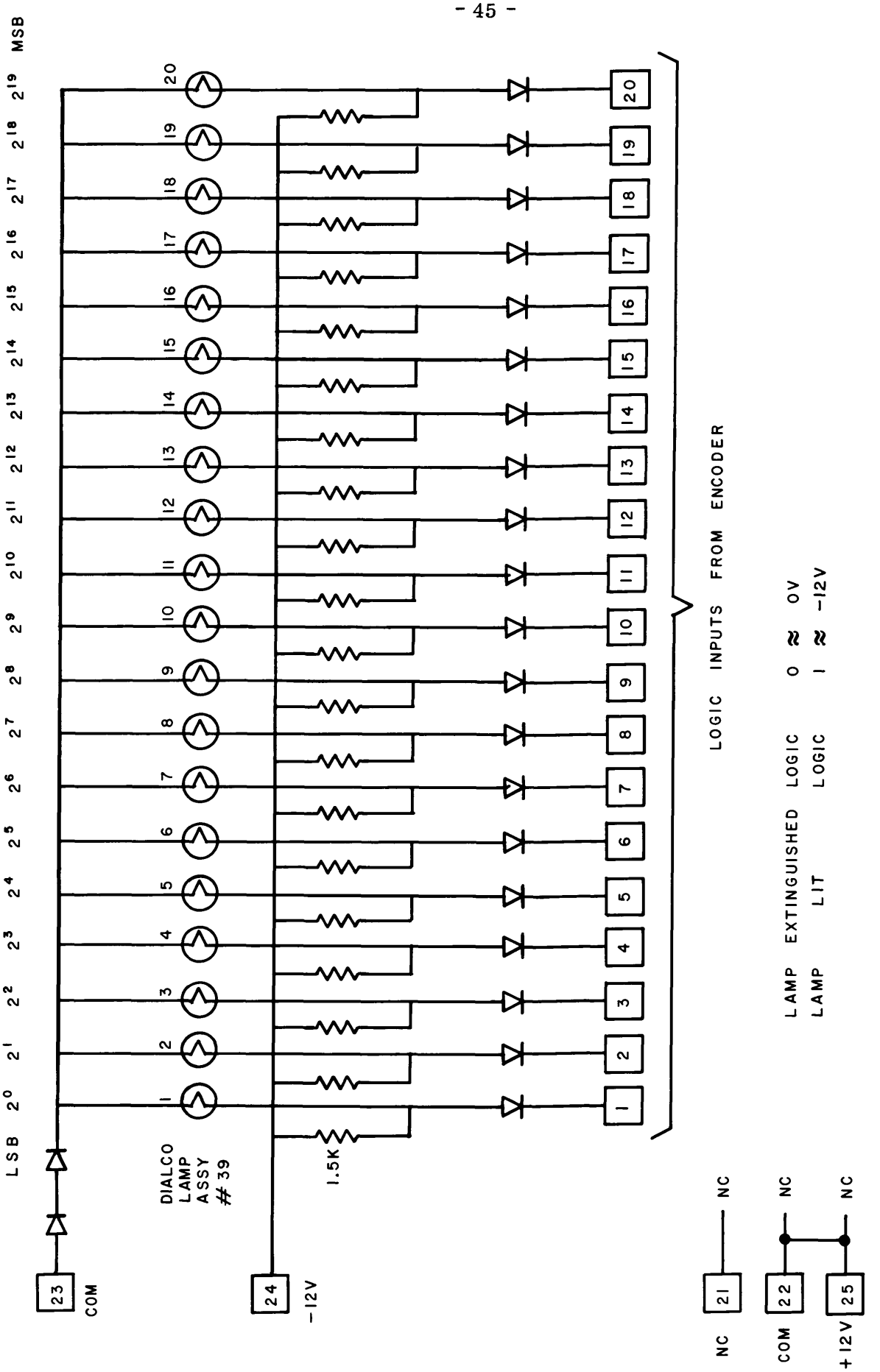
REMOTE LAMP DISPLAY BUFFER CARD # 3
SCHEMATIC # 4



BALDWIN ENCODER INTERFACE PACKAGE
CARD # 4

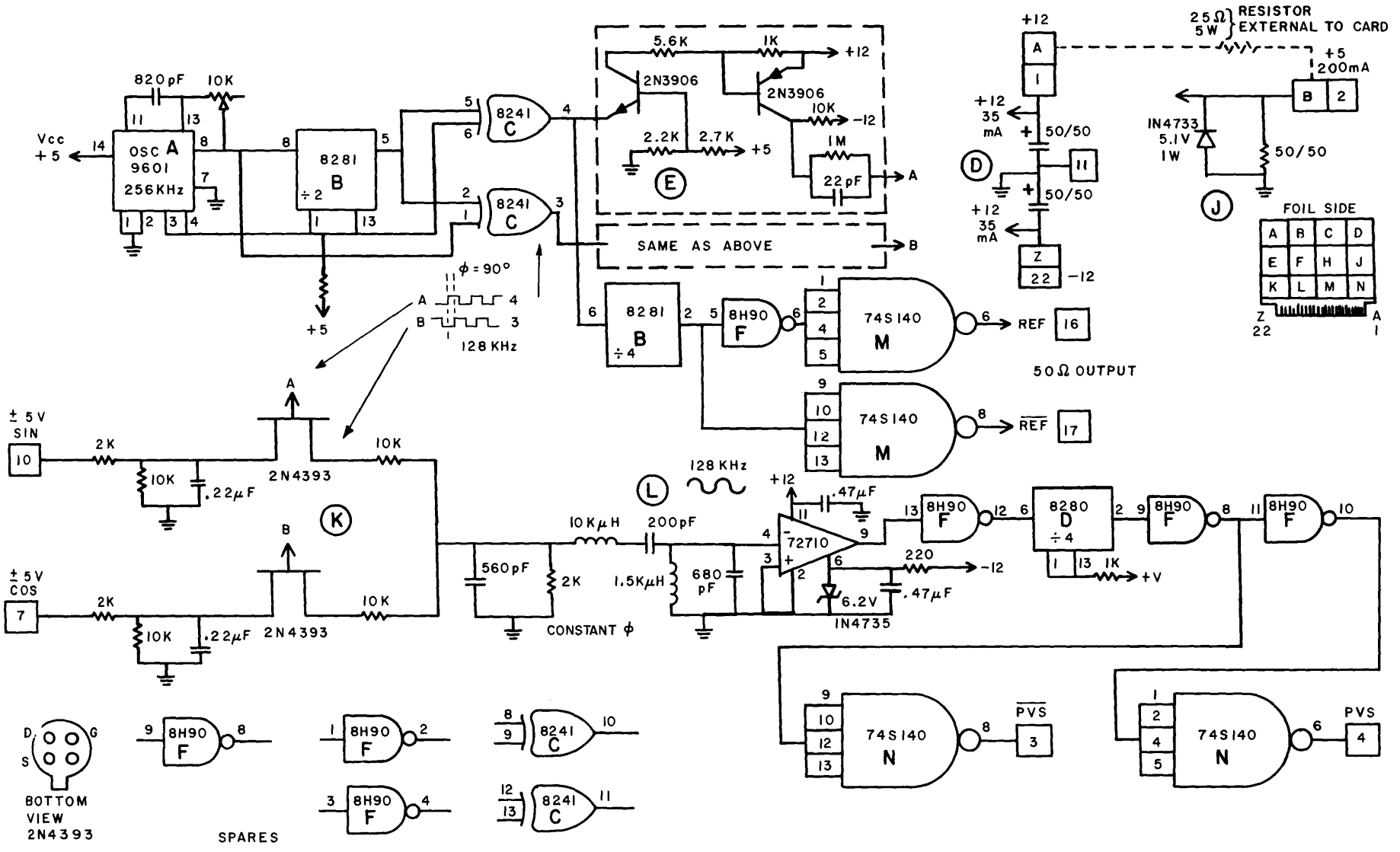


BALDWIN INTERFACE BOX
ENCODER TEMPERATURE INDICATOR CIRCUIT
SCHEMATIC # 5



36' POSITION READOUT W/G REMOTE DISPLAY

SCHEMATIC # 6

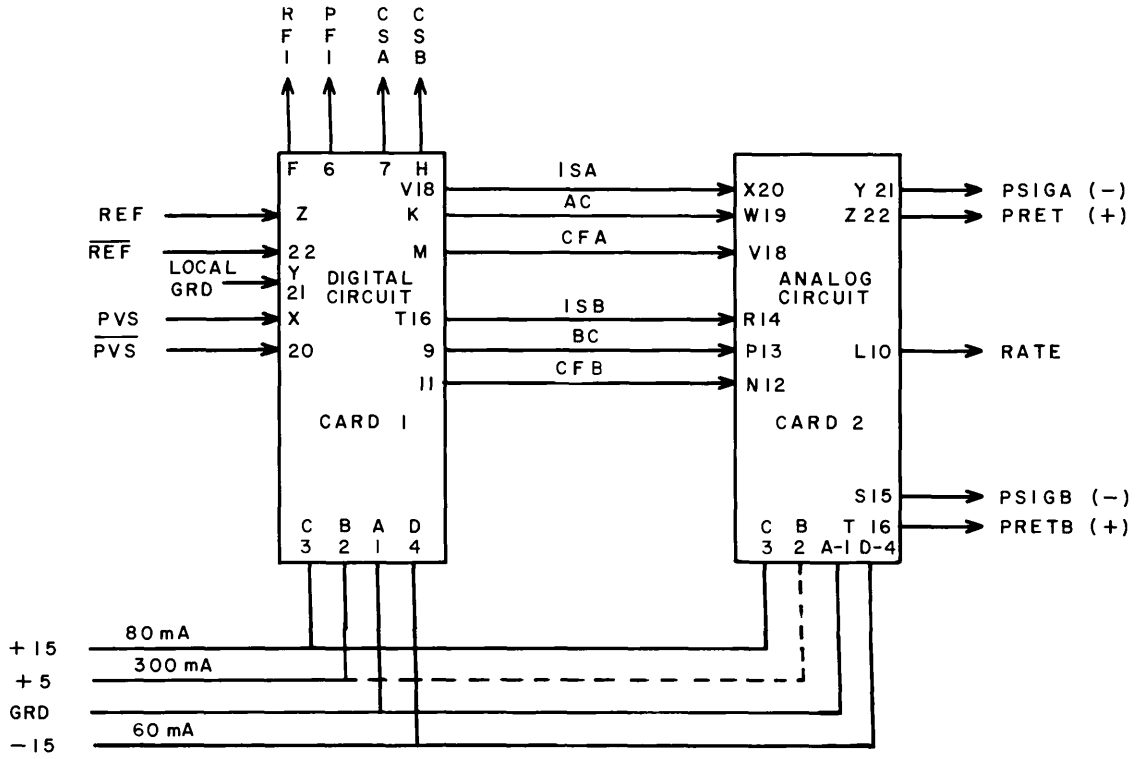


WIRING COLOR CODE

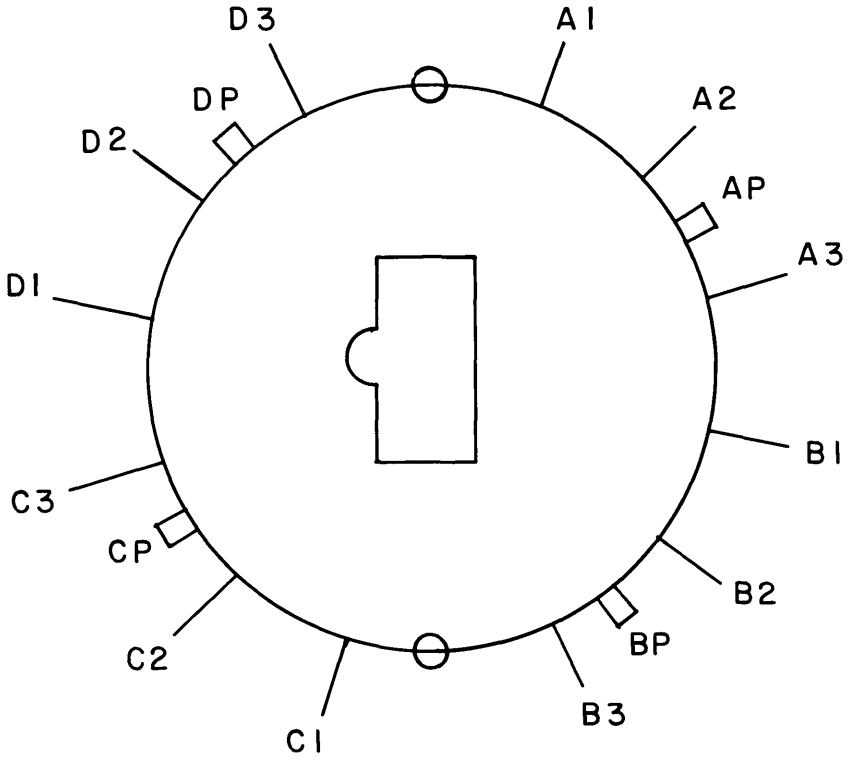
+12V — ORN ; GRD — BLK; +5V — RED; -12V — GRAY.

IC's	EXC. 72710
PIN 14	+5V
PIN 7	GRD

W/G TO BALDWIN MODULATOR CARD
SCHEMATIC # 7



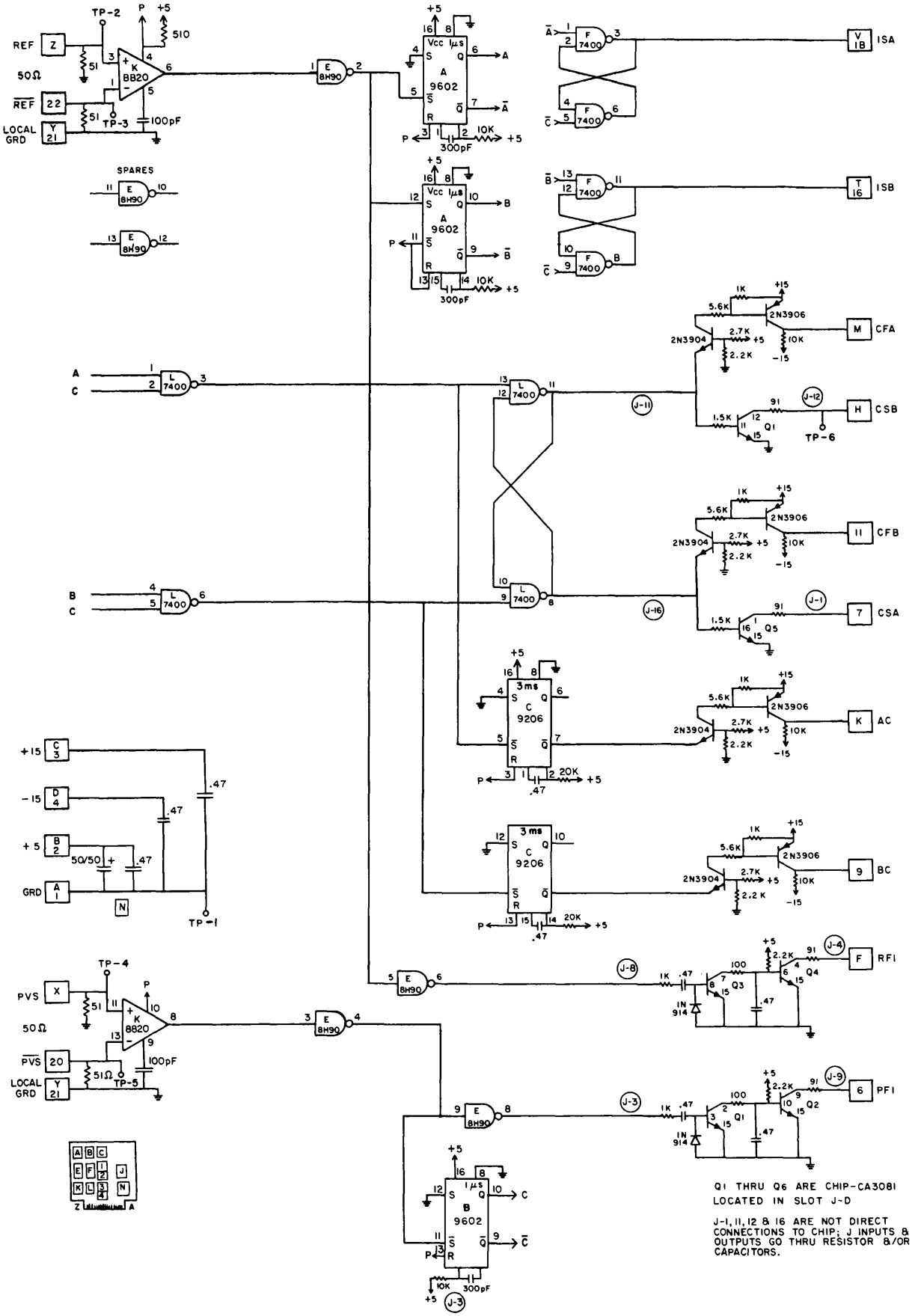
ELECTRONIC TACH CARD INTERCONNECTIONS



FRONT VIEW (KNOB END)

SELECTOR SWITCH NUMBERING FORMAT

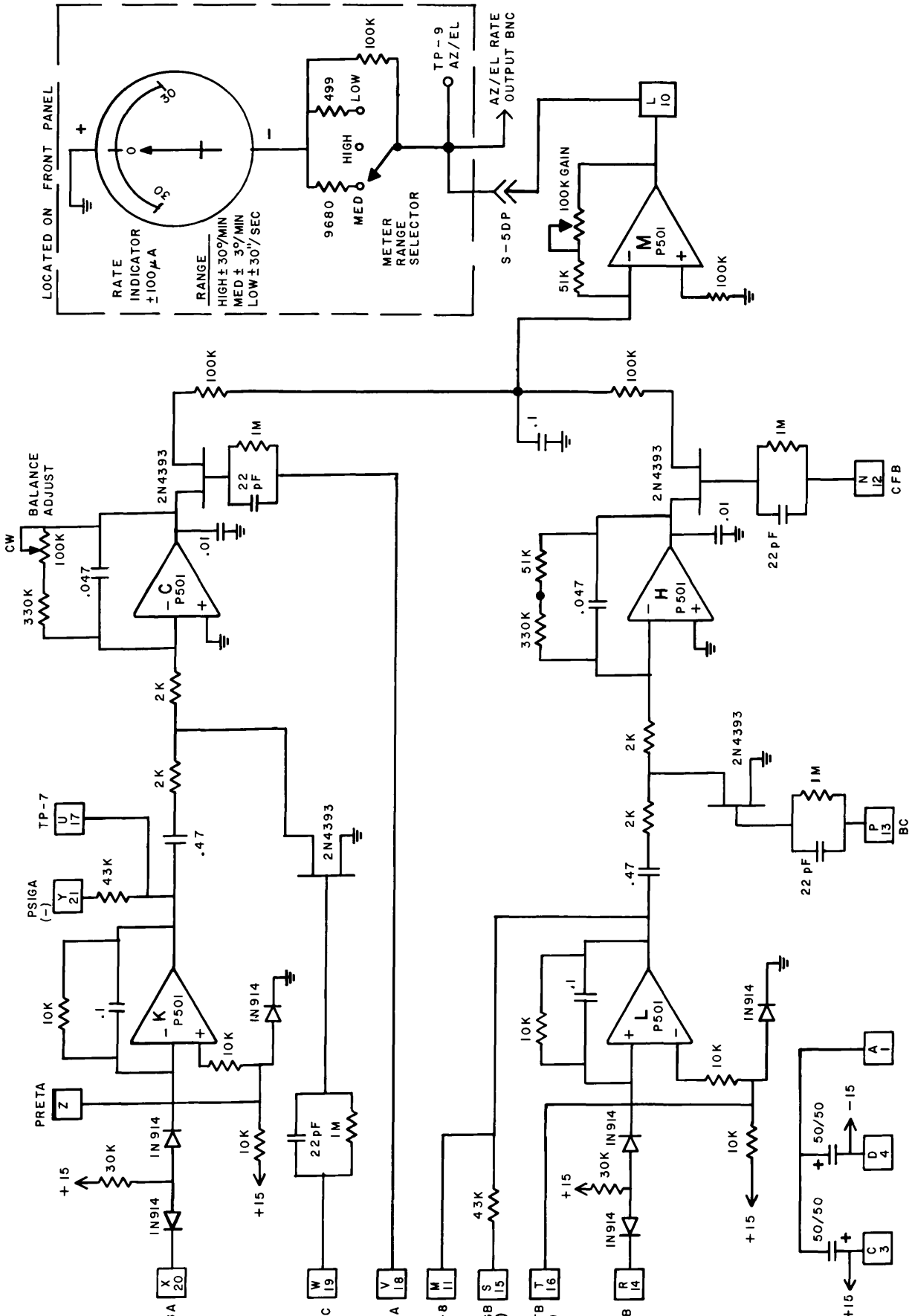
SCHEMATIC # 8



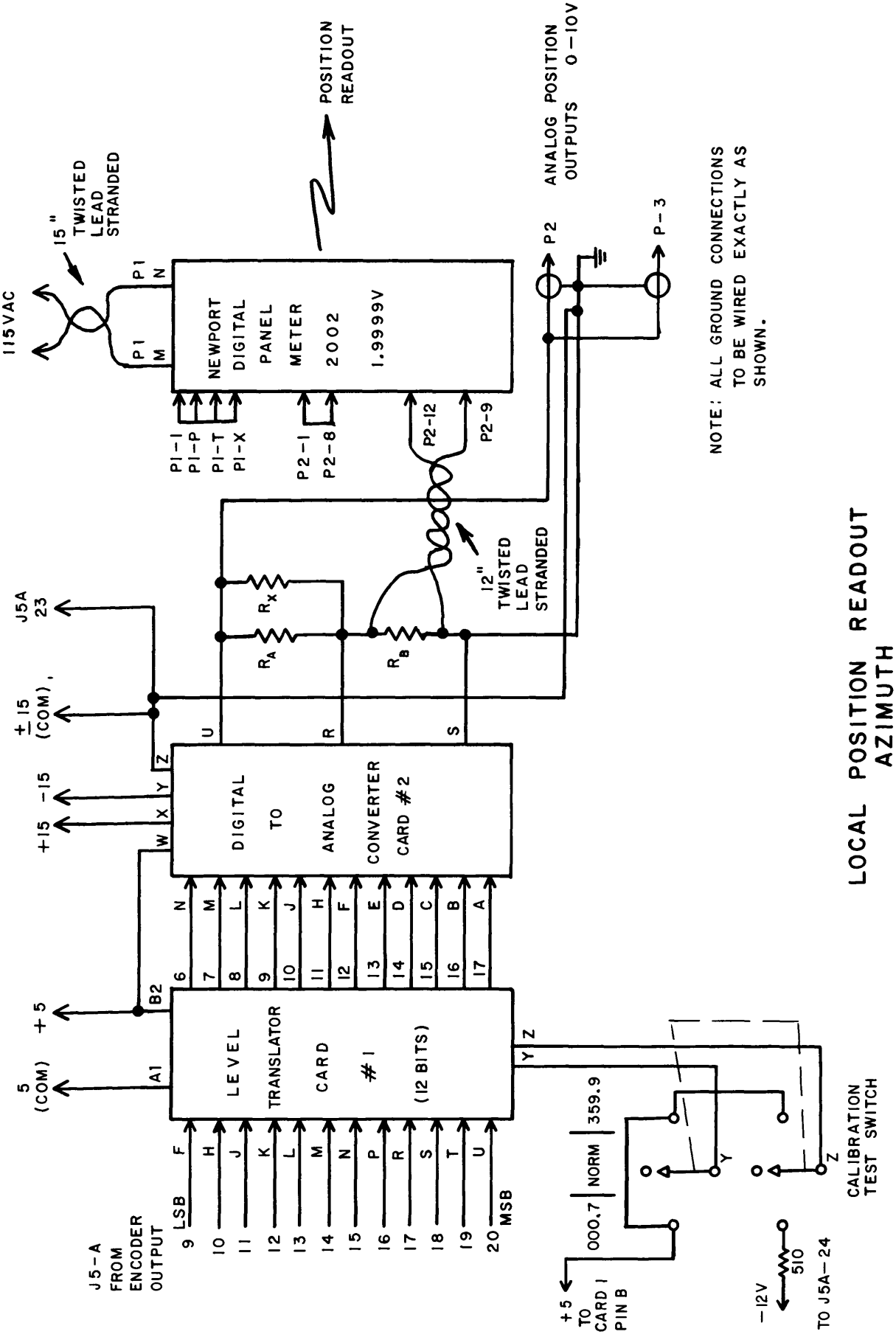
Q1 THRU Q6 ARE CHIP-CA3081 LOCATED IN SLOT J-D

J-1, 11, 12 & 16 ARE NOT DIRECT CONNECTIONS TO CHIP; J INPUTS & OUTPUTS GO THRU RESISTOR &/OR CAPACITORS.

NRAO ELECTRONIC TACHOMETER FOR TELESCOPE DRIVE SYSTEMS
DIGITAL CIRCUIT CARD # 1
SCHEMATIC # 9

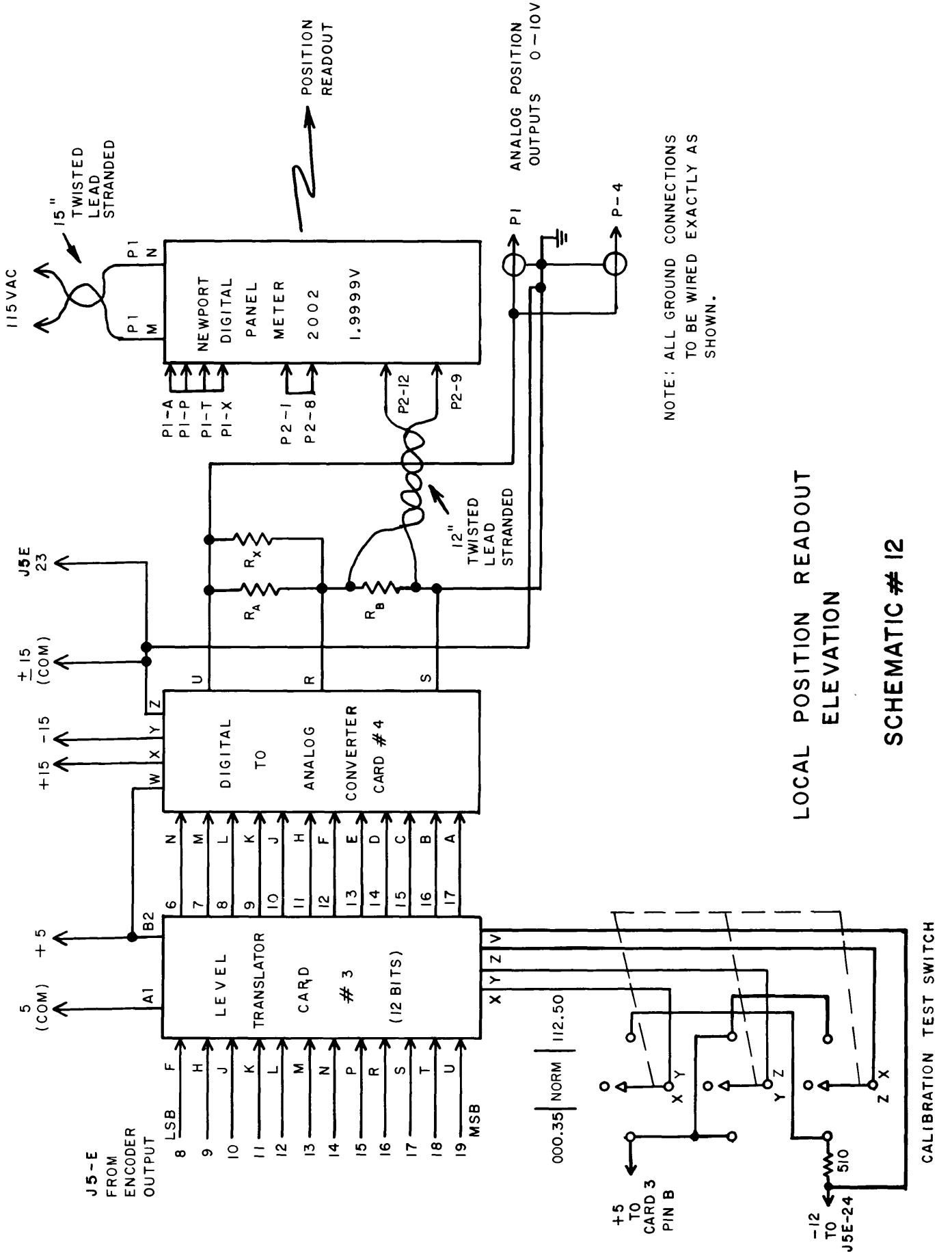


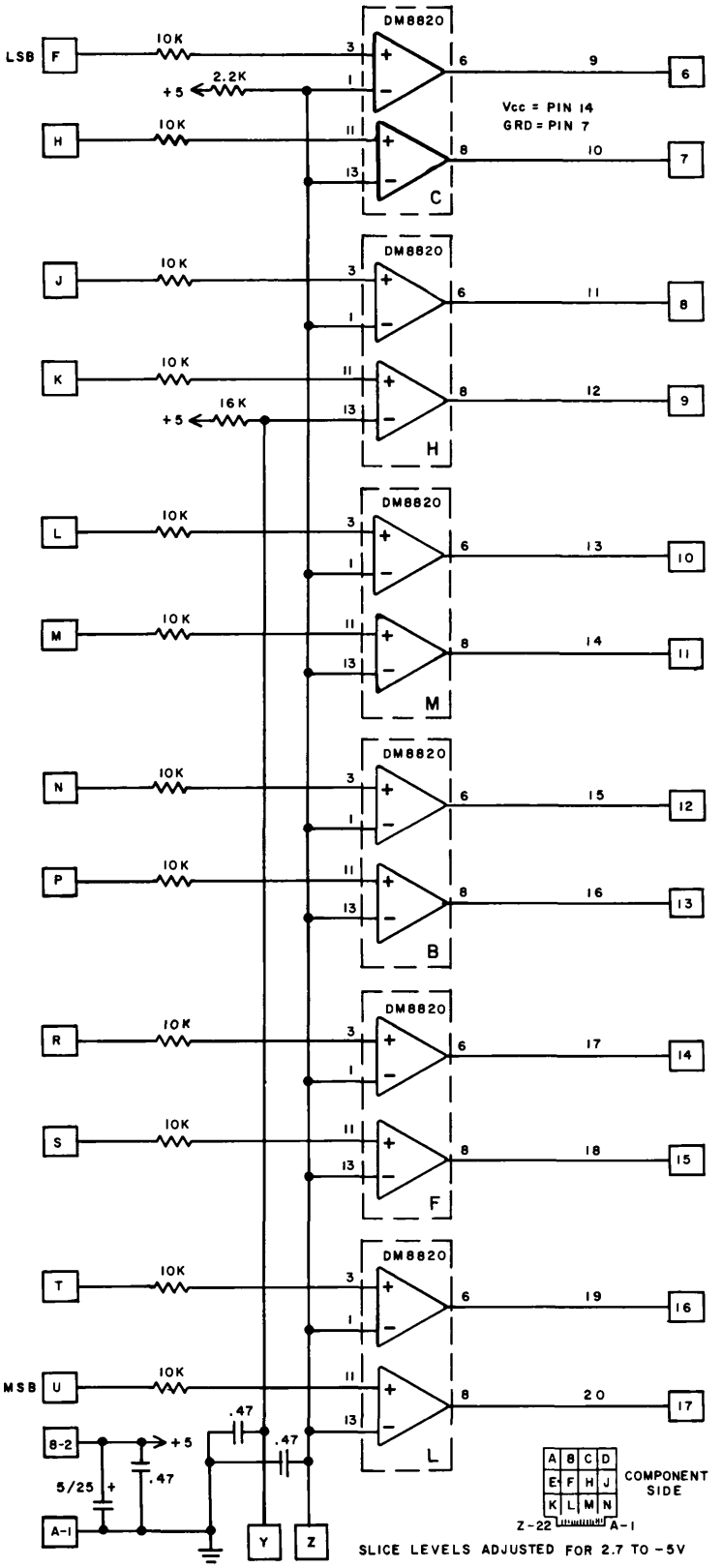
NRAO ELECTRONIC TACHOMETER FOR TELESCOPIC DRIVE SYSTEMS
ANALOG CIRCUIT CARD 2
SCHEMATIC # 10



LOCAL POSITION READOUT
AZIMUTH

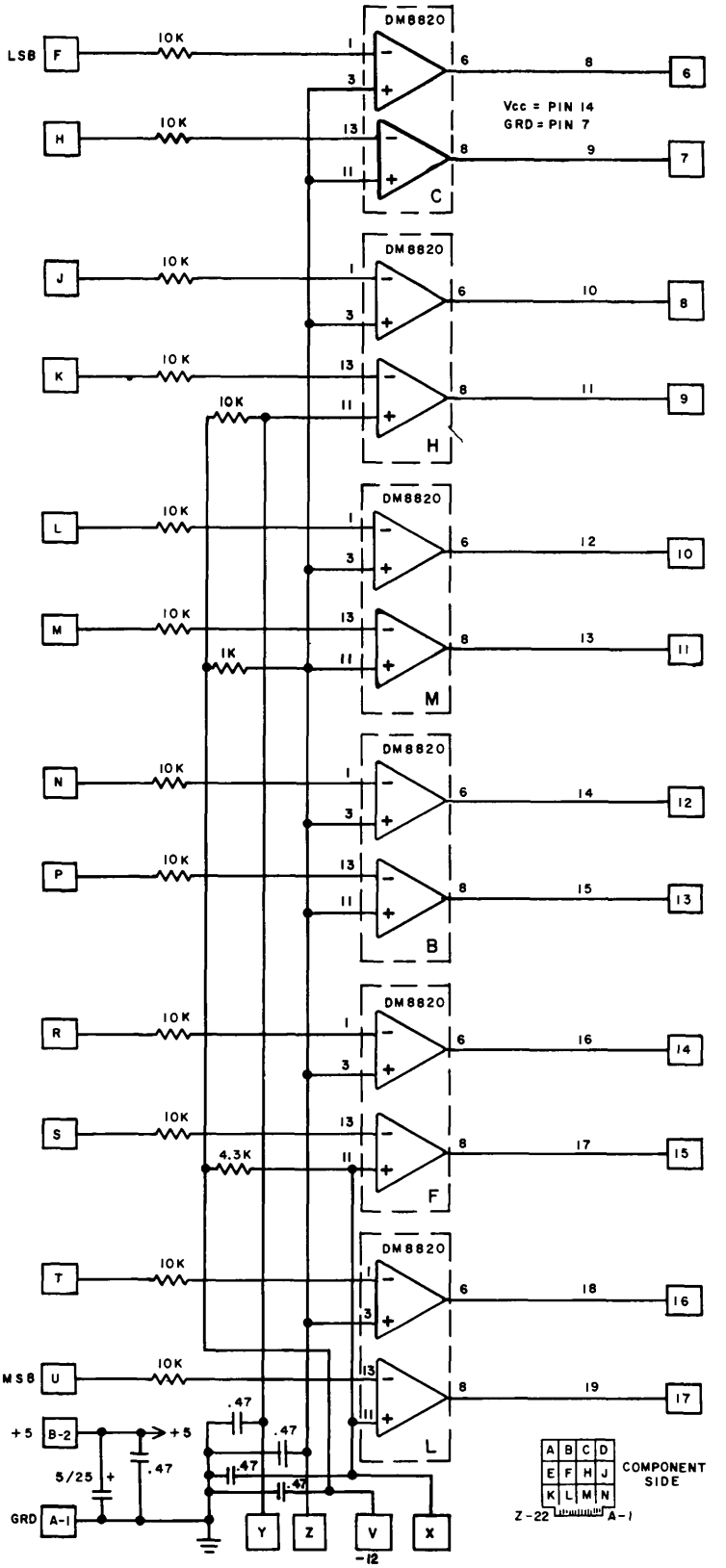
SCHEMATIC # 11


115VAC
15" TWISTED LEAD STRANDED
P1 N
P1 M
NEWPORT DIGITAL PANEL METER 2002
1.9999V
POSITION READOUT
P1 ANALOG POSITION OUTPUTS 0-10V
P-4
P1-A
P1-P
P1-T
P1-X
P2-1
P2-8
P2-12
P2-9
12" TWISTED LEAD STRANDED
R_X
R_A
R_B
J5E 23
±15 (COM)
+15 -15
U
R
S
Z
Y
X
W
DIGITAL TO ANALOG CONVERTER CARD #4
N M L K J H F E D C B A
6 7 8 9 10 11 12 13 14 15 16 17
B2
A1
5 (COM) +5
LEVEL TRANSLATOR CARD # 3 (12 BITS)
V Z Y X
J5-E FROM ENCODER OUTPUT
LSB F H J K L M N P R S T U MSB
8 9 10 11 12 13 14 15 16 17 18 19
000.35 NORM 112.50
X Y Z X
+5 TO CARD 3 PIN B
-12 TO J5E-24
510
CALIBRATION TEST SWITCH
NOTE: ALL GROUND CONNECTIONS TO BE WIRED EXACTLY AS SHOWN.
LOCAL POSITION READOUT ELEVATION
SCHEMATIC # 12



12 BIT LOCAL POSITION READOUT LEVEL TRANSLATOR CARD
FOR AZIMUTH ENCODER CARD # 1

SCHEMATIC # 13



12 BIT LOCAL POSITION READOUT LEVEL TRANSLATOR CARD
FOR ELEVATION ENCODER CARD # 3

SCHEMATIC # 14

GENERAL DESCRIPTION

The DAC-Q is a high performance compact, low profile single-card, general purpose Digital-to-Analog Converter. Units are available in resolutions of 8, 10, and 12 bits. In its most complete form, it accepts a 12 bit Binary code, or a 3-decade Binary-Coded-Decimal number, and stores the number in an internal register upon command of an external strobe. Upon entering the register, the stored number is immediately converted to an output voltage (of optional scaling and polarity) and held until the next strobe command. As a complete unit, it contains a storage register, monolithic IC current switches, a complete thin film resistor network, a reference supply plus amplifier, and an output operational amplifier. It requires only DC power.

INPUT OPTIONS

The DAC-Q includes an optional storage register, which can be wired for either + full scale with all "1"s, or + full scale with all "0"s at the inputs (complementary inputs). Input codes can be binary, offset binary, or their complements, or 2's complement, or BCD. Also, an external reference can be supplied by the user.

OUTPUT OPTIONS

Unipolar or bipolar outputs are available. For bipolar outputs offset binary, or 2's complement code is required. Unipolar ranges are 0 to +5V or 0 to +10V standard. Bipolar ranges are ±5V or ±10V.

ALL MONOLITHIC COMPONENTS

Construction of the new DAC-Q series centers around the new monolithic μDAC IC D/A components. The Model AD550 quad current switches are used in conjunction with a thin film modular resistor network. The AD550 IC switches are designed for optimal temperature tracking. The thin film resistor network includes all the critical, gain determining resistors. A high gain reference amplifier assures that all variations in switch parameters are ideally compensated. The interquad attenuation network is 16:1 for straight binary and 10:1 for BCD. The output amplifier may be wired for unipolar or bipolar output voltage. An external reference, if used, may have any value from full scale to 50% of F.S.

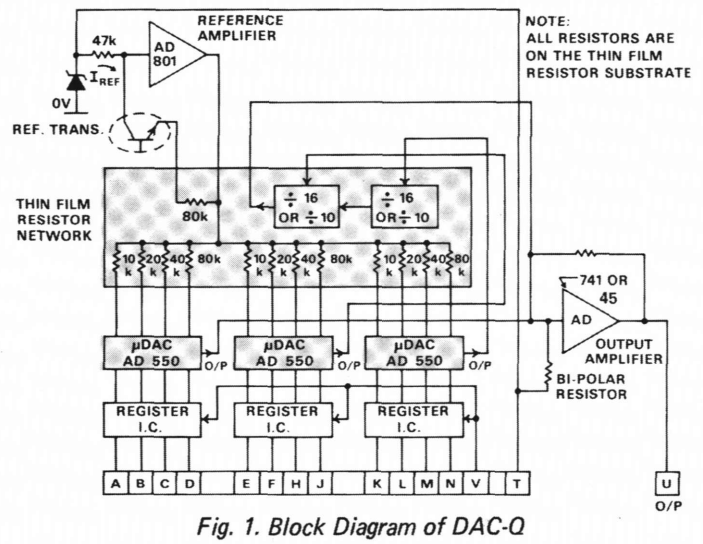
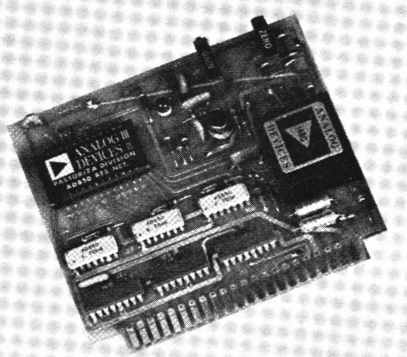


Fig. 1. Block Diagram of DAC-Q

DAC-Q
DIGITAL TO ANALOG CONVERTERS
Complete Compact D/A Converters to 12 Bits with High Performance, Low Cost, & Many Options

FEATURES

- 8, 10, and 12 Bit Resolutions and Accuracies
- Low Cost/Performance Ratio
- Low TC (±7ppm/°C)
- Ultra-Low (0.42") Profile
- Excellent Power Supply Rejection 0.002%/%ΔV_S
- Binary or BCD Coding
- -55°C to +125°C on Request
- Many Options



ANALOG DEVICES INC
PASTORIZA DIVISION
221 FIFTH ST., CAMBRIDGE, MASS. 02142
TEL: 617/492-6000 TWX: 710/320-0325

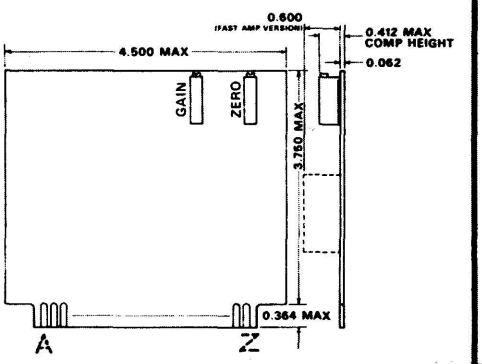
DAC-Q
DIGITAL-TO-ANALOG CONVERTERS
SPECIFICATIONS (typical @ 25°C unless otherwise noted)

MODEL	DAC-Q
RESOLUTION	DAC- 8Q 8 Bits DAC-10Q 10 Bits DAC-12Q 12 Bits
DIGITAL INPUTS	"0" +0.8V max @ −3.2mA "1" +2.0V min @ 80μA TTL Compatible
STROBE	Data transfers from inputs to register on "0" to "1" change. Width at least 50nsec, "0–1" transition at least 100nsec after data change.
INPUT CODES	Binary, Offset Binary, Complementary Binary, Complementary Offset Binary, BCD, 2's Complement, Comp. 2's Complement
OUTPUT RANGE	0 to +5V @ 10mA 0 to +10V @ 10mA ±5V or ±10V @ ±10mA
OUTPUT IMPEDANCE	0.02 ohm
CONVERSION SPEED	Fast Amplifier; 2.5μsec to < 0.01% Slewing Rate: 50V/μsec Standard Amplifier; 50μsec to < 0.01% Slewing Rate: 0.5V/μsec
LINEARITY	±½LSB
ACCURACY Relative Absolute	 ±½LSB ±½LSB (when internal reference supplied)
TEMP COEFFICIENT	±7ppm/°C max
TEMP RANGE	0°C to +70°C −55°C to +125°C (add suffix ET*)
POWER REQUIRED	+15VDC @ +25mA −15VDC @ −30mA +5VDC @ 150mA—with register @ 25mA—without register
POWER SUPPLY SENSITIVITY	0.002%/% supply variation (±15VDC supplies—only)
ADJUSTMENTS	Zero, Gain (DAC-Q converters are factory pre-adjusted)

*ET = Extended Temperature (Std. Amplifier only)
Specifications subject to change without notice

PRICES (1–9)	DAC-8Q	DAC-10Q	DAC-12Q
without storage register	$135.	$165.	$185.
with storage register	$165.	$205.	$225.
Fast Amplifier	Add $50. to above prices		

OUTLINE DIMENSIONS



Mates with Cinch 250-22-30-170 Socket (Supplied)

PIN CONNECTIONS

PIN	FUNCTION
A	BIT 1 MSB
B	BIT 2
C	BIT 3
D	BIT 4
E	BIT 5
F	BIT 6
H	BIT 7
J	BIT 8 LSB DAC-8Q
K	BIT 9
L	BIT 10 LSB DAC-10Q
M	BIT 11
N	BIT 12 LSB DAC-12Q
P	CONNECTED TO R
R	CONNECTED TO P
S	ANALOG GROUND
T	REFERENCE
U	OUTPUT
V	STROBE
W	+5V
X	+15V
Y	−15V
Z	DIGITAL GROUND

Note: S and Z are normally connected. Disconnect by drilling plated hole.

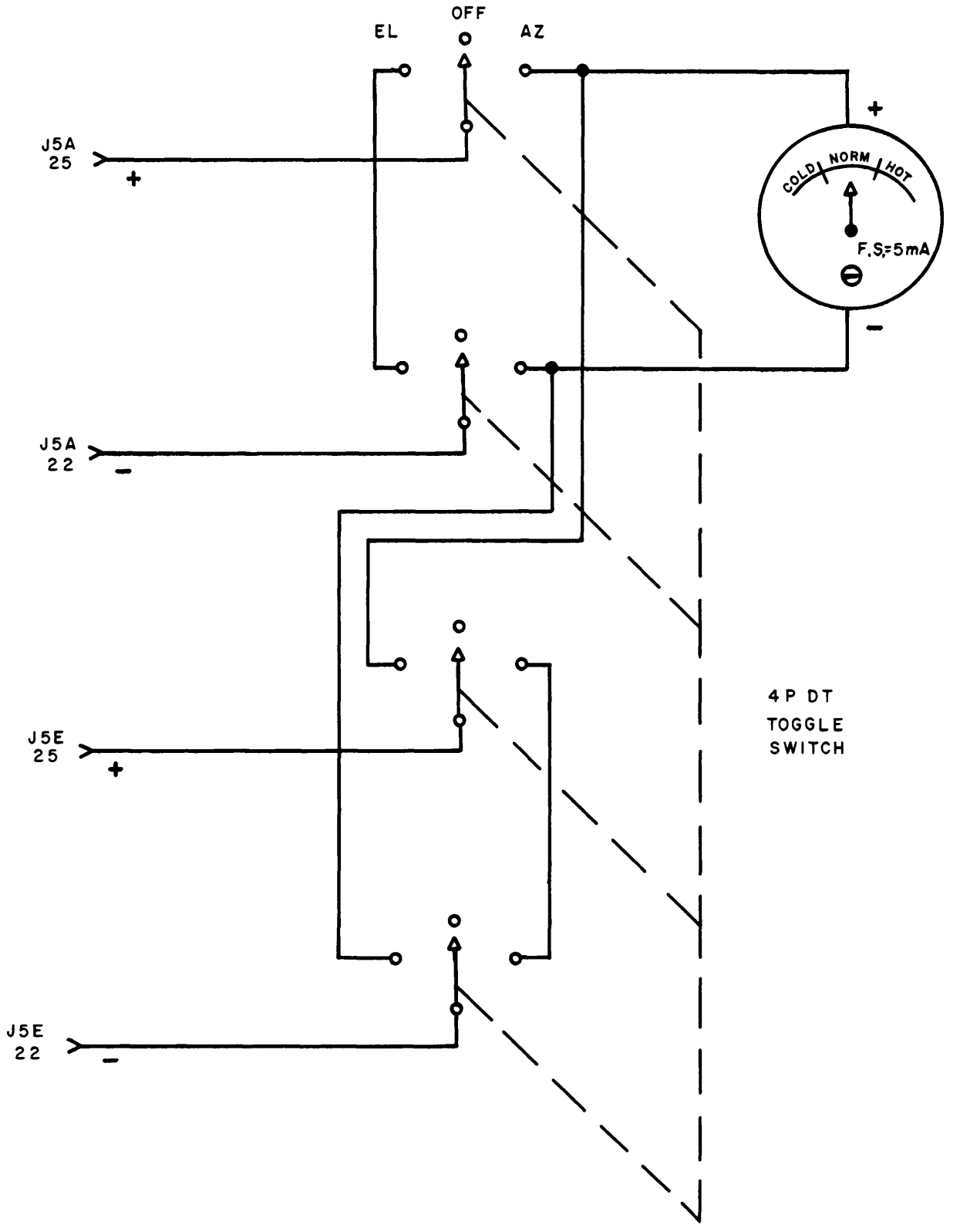
ORDERING GUIDE: DAC-Q

MODEL NO. — DAC XX XX / XXX / XXX / ±XXX / XXXX

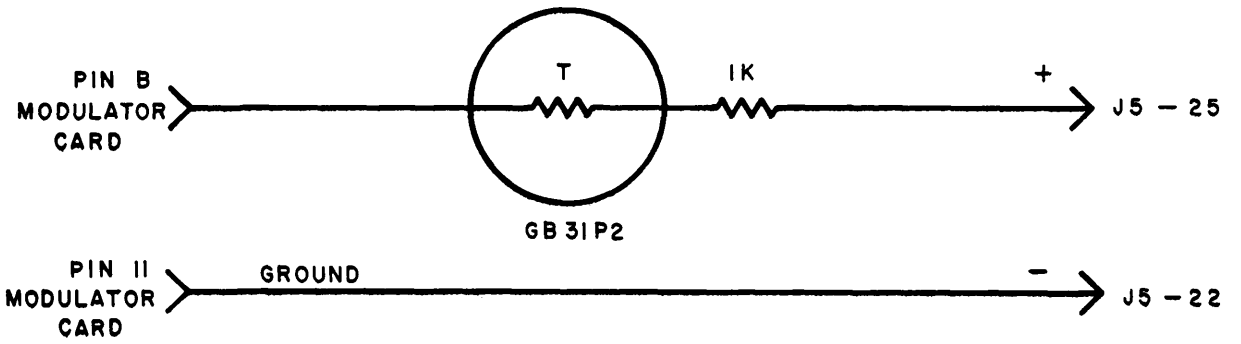
	No. of Bits	Series	Input Code	Input Register	Output Range	Output Amplifier
Conv. type	8 10 12	Q (P.C. Card) QM (Module)	BIN (binary) C–B (comp. binary) OBN (offset binary) COB (comp. off. bin.) 2SC (2's comp.) C2C (comp. 2's comp.) BCD	REG DIR (direct)	+5V +10V ±5V ±10V	STD FAST

Notes: (1) Complementary Binary is the standard code when register is omitted.
(2) Internal Reference included unless specified otherwise. (+5.875V nominal)
(3) 0°C to +70°C Standard; for −55°C to +125°C, specify "Extended Temperature" (consult Factory for price).

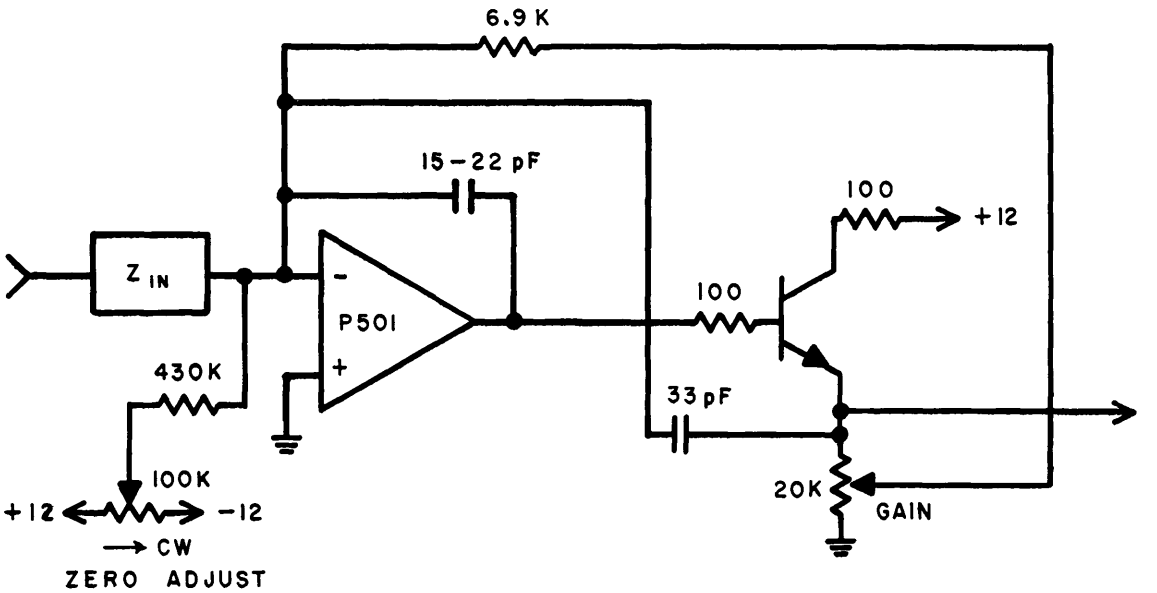
For information on the Modular DAC-QM (2"X4"X 0.4") consult your local ADI Representative, or call the Factory direct.



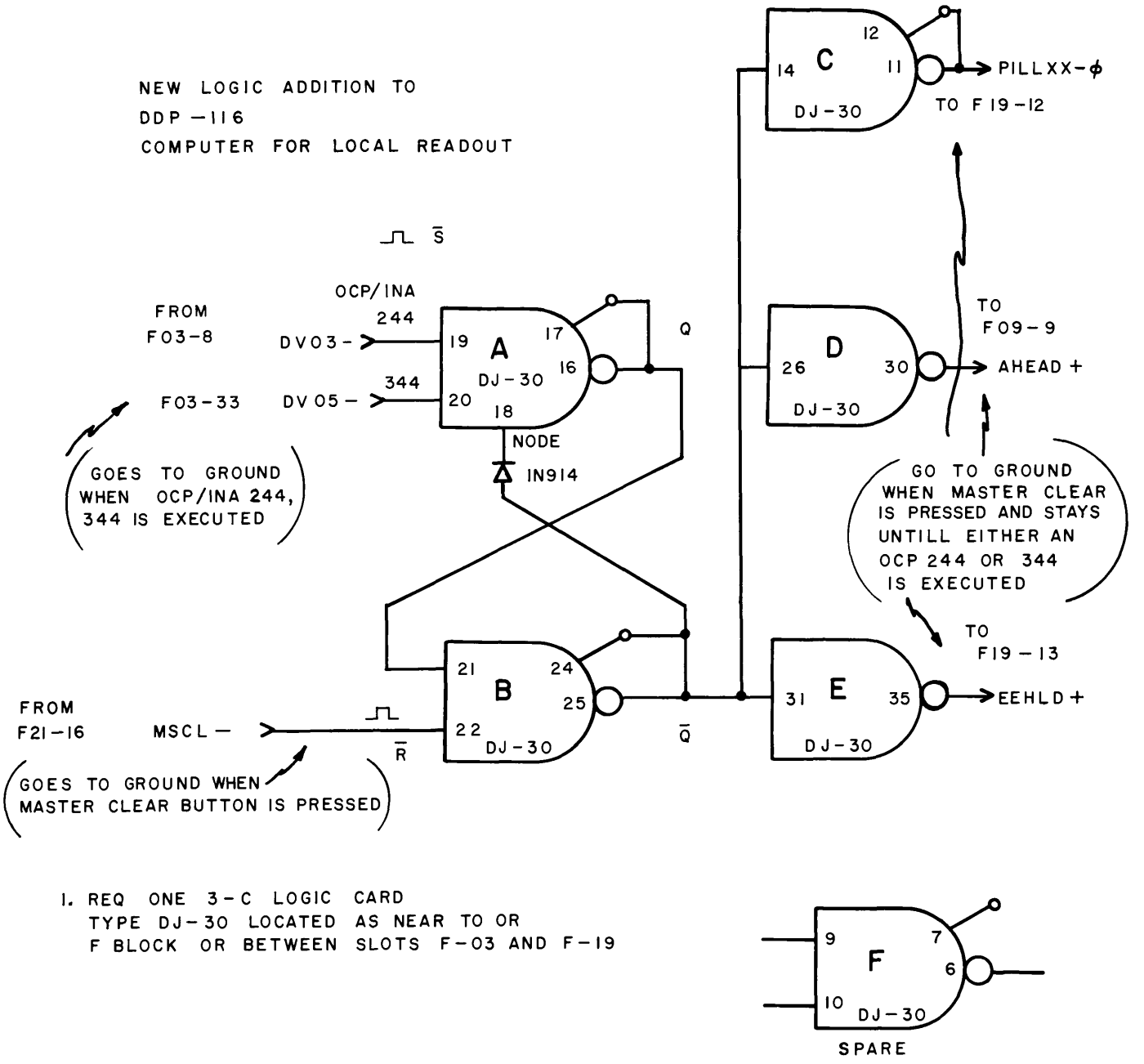
ENCODER TEMPERATURE INDICATOR
AUXILLARY POSITION READOUT CHASSIS
SCHEMATIC # 17



TEMPERATURE CIRCUIT IN WAYNE GEORGE ELECTRONICS BOX
SCHEMATIC # 18



MODIFICATION TO W/G SIN/COS PREAMPLIFIER CARD # 417
SCHEMATIC # 19



36.' LOCAL READOUT

LOGIC TO ENABLE LOCAL READOUT WHEN COMPUTER NOT READING ENCODERS

SCHEMATIC # 20

12. SIGNAL DESIGNATION LISTS

Mnemonic	Function
AC	Tach channel A blanking
AEHLD	Computer azimuth encoder hold line
BC	Tach Channel B blanking
CFA.....	Channel switch FET A control
CFB	Channel switch FET B control
COS	Encoder signal varies cosinusoidally as a function of position
CSA	Channel switch A indicator
CSB	Channel switch B indicator
EEHLD	Computer elevation encoder hold line
HOLD	Inhibits encoder refresh
ISA	Duty factor variable position encoded signal, tach channel A
ISB	Duty factor variable position encoded signal, tach channel B
MSCL	Master clear
PFI	PVS fail indicator
PILXX	Priority interrupt line
PRETA	Position channel A return
PRETB	Position channel B return
PSIGA	Position channel A signal
PSIGB	Position channel B signal
PVS	Phase variable signal as a function of position with respect to REF
$\overline{\text{PVS}}$	Inverse PVS in differential link
RATE	Tach output signal
READ	Signals computer to read encoder data
REF	32 kHz reference signal to tach
$\overline{\text{REF}}$	Inverse REF in differential link
RFI	REF Fail indicator
SIN	Encoder signal varies sinusoidally as a function of position

13. TEST POINT LIST (ELECTRONIC TACH)

TP	Function
1	Ground
2	REF
3	$\overline{\text{REF}}$
4	PVS
5	$\overline{\text{PVS}}$
6	Channel Switch
7	Position Channel A
8	Position Channel B
9	Rate Output to Servo

14. CONNECTOR LISTS

The following connectors are located on the Baldwin encoder:

Circuit Designation	Type	Description	Function
J-0	DC 37P	37 Pin Male	Encoder power, control, and data.

The following connectors are located on the Baldwin encoder interface package:

Circuit Designation	Type	Description	Function
J-1	Cannon DC 37P	37 Pin Male	Encoder data
J-2	Cannon DC 37S	37 Pin Female	Computer data
J-3	Cannon DE 9S	9 Pin Female	Modulator to Elec. Tach
J-4	Cannon DE 9P	15 Pin Male	AC Power
J-5	Cannon DB 25S	25 Pin Female	Remote display

The following connectors are located on the electronic tach chassis:

Circuit Designation	Type	Description	Function
J-3A & E	Cannon DE 9P	9 Pin Male	Modulated input
R-A & E	BNC	Female	Rate output

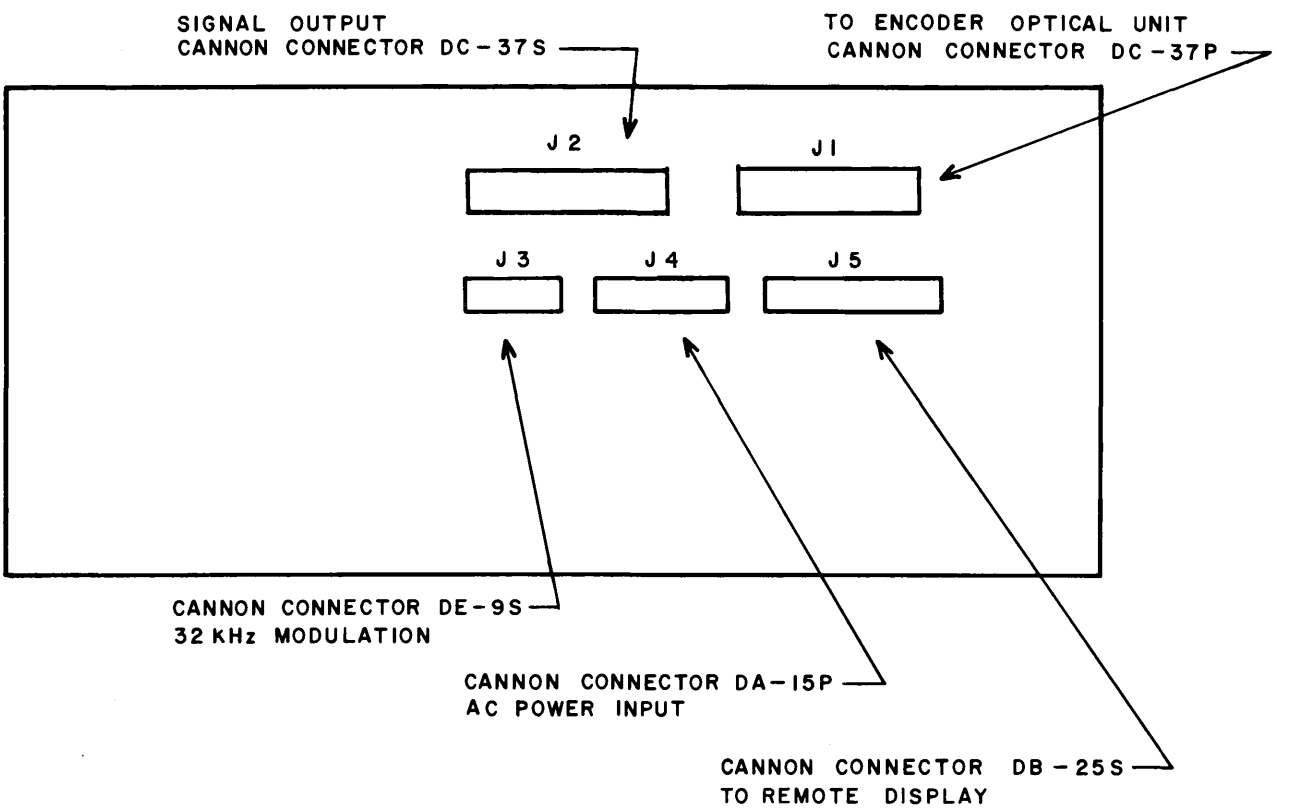
The following connectors are located on the coarse position readout chassis:

Circuit Designation	Type	Description	Function
J-5	Cannon DB 25P	25 Pin Male	Remote display
P-1, 2, 3, 4	BNC	Female	Analog position

The following connectors are located on the rear of the DPM's associated with the coarse readout:

Circuit Designation	Type	Description	Function
P-1	Cinch 50-44A-30	44 Pin	Digital board
P-2	Cinch 50-15A-20	15 Pin	Analog board

Figure 13 shows the connectors and function for the Baldwin encoder interface box.



FRONT PANEL, BALDWIN ENCODER INTERFACE BOX
FIG. 13

CONNECTOR LISTS

J-0 & J-1

Pin	Function	
1	2^{19} Output	MSB
2	2^{18} "	
3	2^{17} "	
4	2^{16} "	
5	2^{15} "	
6	2^{14} "	
7	2^{13} "	
8	2^{12} "	
9	2^{11} "	20 Bit Binary
10	2^{10} "	Encoded Posi-
11	2^{9} "	tion Output
12	2^{8} "	
13	2^{7} "	
14	2^{6} "	
15	2^{5} "	
16	2^{4} "	
17	2^{3} "	
18	2^{2} "	
19	2^{1} "	
20	2^{0} "	LSB
21	NC	
22	Thermistor	
23	Thermistor	
24	Ground Test	
25	NC	
26	+5 V Test	
27	NC	
28	-5.5 V Test	
29	NC	
30	REF	
31	PVS	
32	Hold Logic "0" = Hold	
33	Circuit Ground	
34	+5 V DC, 1.1 amp	
35	-5.5 V DC, 0.8 amp	
36	Marker Pulse	
37	Case Ground	

J-2

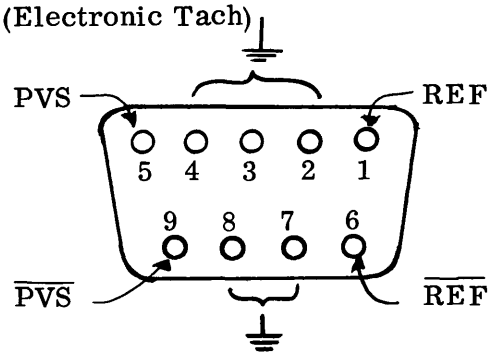
Pin	Function
1	2^{0} Output
2	2^{1} "
3	2^{2} "
4	2^{3} "
5	2^{4} "
6	2^{5} "
7	2^{6} "
8	2^{7} "
9	2^{8} "
10	2^{9} "
11	2^{10} "
12	2^{11} "
13	2^{12} "
14	2^{13} "
15	2^{14} "
16	2^{15} "
17	2^{16} "
18	2^{17} "
19	2^{18} "
20	2^{19} "
21	NC
22	NC
23	NC
24	NC
25	Ground - Data Common
26	NC
27	NC
28	NC
29	Ground - Shield
30	NC
31	NC
32	Hold (-6 V Holds)
33	NC
34	Ground - Inhibit, Hold Return - Control Common
35	Inhibit Output (-6 V When Held)
36	NC
37	Ground - Case Ground

CONNECTOR LISTS

J-3, J-3A, J-3E

DE 9S Female Conductor J-3.

(Electronic Tach)



Pin	Function	W/G Slot 462
1	REF	16
2	Ground	11
3	Ground	NC
4	Ground	11
5	PVS	4
6	$\overline{REF}$	17
7	Ground	11
8	Ground	11
9	$\overline{PVS}$	3

Pin	Function
1	AC Input
2	NC
3	AC Input
4	NC
5	NC
6	NC
7	NC
8	NC
9	Case Ground
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC

J-5

Pin	Function
1	2^0 Output
2	2^1 "
3	2^2 "
4	2^3 "
5	2^4 "
6	2^5 "
7	2^6 "
8	2^7 "
9	2^8 "
10	2^9 "
11	2^{10} "
12	2^{11} "
13	2^{12} "
14	2^{13} "
15	2^{14} "
16	2^{15} "
17	2^{16} "
18	2^{17} "
19	2^{18} "
20	2^{19} "
21	NC
22	- Encoder Temperature Indicator
23	Signal Common
24	-12 V DC
25	+ Encoder Temperature Indicator

CONNECTOR PIN ASSIGNMENTS - DIGITAL PANEL METER - SERIES 2000

P1 Digital Board - Upper Side		P1 Digital Board - Lower Side		P2 Analog Board -Either Side	
Pin	Function	Pin	Function	Pin	Function
1	D. P. 1xxx. x	A	D. P. 1xx. xx	1	Guard
2	1 bit	B	4 bit	2	
3	2 bit	C	8 bit	3	-30 volts
4	4 K bit	D	20 bit	4	
5	8 K bit	E	10 bit	5	
6	40 bit	F	80 bit	6	+30 volts
7	200 bit	H	100 bit	7	
8	400 bit	J	800 bit	8	Sig Gnd (analog)
9	2 K bit	K	1 K bit	9	Sig Gnd (analog)
10	OL bit	L	10 K bit	10	G_m Resistor
11	Open	M	AC Line HI	11	AC Sig Input
12	Open	N	AC Line LO	12	DC Sig Input
13	Gnd (case & power line)	P	Gnd (case & power line)	13	Atten Com
14	Serial Out	R	Measurement Enable Rate	14	Ext Ref In
15	$\overline{\text{Measurement Enable}}$	S	Strobe Transfer	15	Guard
16	Gnd (Digital)	T	Gnd (Digital)		
17	Conversion Period	U	+5 volts		
18	Integration Period	V	Measurement Enable		
19	30/Second Enable	W	20/Second Enable		
20	Neg Polarity bit	X	4/Second Enable		
21	D. P. 1. xxxx	Y	Buffer Out		
22	D. P. 1x. xxx	Z	+250 volts (1/2 wave)		

NOTE: To initiate readings, connect P1-W, P1-X, or P1-19 to P1-16 or P1-T.

15 WIRING LISTS

Wiring lists are presented in two subsections:

15-A Encoder Interface Box Lists

15-B Electronic Tachometer Lists

No list is shown for the coarse readout since the wiring may be obtained from schematics 11 and 12 in Section 11.

15-A ENCODER INTERFACE BOX

Card 0

From	To
1	+5, 1-1, J1-35
2	-12, 1-2
3	1-C
4	1-D
5	1-E
6	1-F
7	1-H
8	1-J
9	1-K
10	1-L
11	1-M
12	1-N
13	1-P
14	1-R
15	1-S
16	1-T
17	1-U
18	1-V
19	1-W
20	1-X
21	1-Y
22	1-Z

From	To
A	Common Ground - J1-37 (use binding post), J-33, All supplies
B	-5.5, J1-35, 4-B
C	3C, J1-1
D	3D, J1-2
E	3E, J1-3
F	3F, J1-4
H	3H, J1-5
J	3J, J1-6
K	3K, J1-7
L	3L, J1-8
M	3M, J1-9
N	3N, J1-10
P	3P, J1-11
R	3R, J1-12
S	3S, J1-18
T	3T, J1-14
U	3U, J1-15
V	3V, J1-16
W	3W, J1-17
X	3X, J1-18
Y	3Y, J1-19
Z	3Z, J1-20

15-A ENCODER INTERFACE BOX

Card 1

From	To
1	2-1
2	2-2
3	J2-20
4	J2-19
5	J2-18
6	J2-17
7	J2-16
8	J2-15
9	J2-14
10	J2-13
11	J2-12
12	J2-11
13	J2-10
14	J2-9
15	J2-8
16	J2-7
17	J2-6
18	J2-5
19	J2-4
20	J2-3
21	J2-2
22	J2-1

From	To
A	0-A, 2-A
B	NC
C	--
D	--
E	--
F	--
H	--
J	--
K	--
L	--
M	--
N	--
P	--
R	--
S	--
T	--
U	--
V	--
W	--
X	--
Y	--
Z	--

15-A ENCODER INTERFACE BOX

Card 2

From	To
1	3-1
2	3-2
3	NC
4	
5	NC
6	
7	NC
8	
9	NC
10	
11	NC
12	
13	NC
14	
15	
16	
17	NC
18	
19	
20	
21	NC
22	NC

From	To
A	3-A, J2-25, J2-29 (use binding post), J2-34, J2-37
B	NC
C	NC
D	J2-35
E	NC
F	J2-32
H	NC
J	J1-32
K	NC
L	J1-31
M	NC
N	J1-30
P	NC
R	J3-2, 3, 7 (shields) (two coax leads)
S	J3-9
T	J3-5
U	NC
V	J3-3, 4, 8 (shields) (two coax leads)
W	J3-6
X	J3-1
Y	NC
Z	NC

15-A ENCODER INTERFACE BOX

Card 3

From	To
1	4-1
2	4-2, J5-24
3	J5-20
4	J5-19
5	J5-18
6	J5-17
7	J5-16
8	J5-15
9	J5-14
10	J5-13
11	J5-12
12	J5-11
13	J5-10
14	J5-9
15	J5-8
16	J5-7
17	J5-6
18	J5-5
19	J5-4
20	J5-3
21	J5-2
22	J5-1

From	To
A	4-A, J5-22 (use binding post), J5-23
B	NC
C	--
D	--
E	--
F	--
H	--
J	--
K	--
L	--
M	--
N	--
P	--
R	--
S	--
T	--
U	--
V	--
W	--
X	--
Y	--
Z	--

15-A ENCODER INTERFACE BOX

Card 4

From	To	From	To
1	--	A	--
2	--	B	--
3		C	
4		D	
5		E	
6		F	
7		H	
8		J	
9		K	
10		L	
11		M	
12		N	
13		P	
14		R	
15		S	
16		T	
17	To AC Hot of 3 supplies. See Note 1.	U	J4-2
18		V	
19	4-17	W	To AC Hot of fan
20		X	
21		Y	
22		Z	

Note 1 — Wire J4-3 to AC common of 3 power supplies and fan, by removing supplies and leaving 6 inches slack between them. Wire J4-9 to chassis.

15-B ELECTRONIC TACH WIRING LISTS

The electronic tach wiring is mostly associated with the selector switch for interchanging spares. The numbering format for the switch is shown in schematic 8 in Section 11.

Also, the following mnemonics are used in the wiring tables:

Mnemonic	Function	
A	Azimuth	1st letter
S	Spare	
E	Elevation	
1	Digital Card 1, Tach	2nd number
2	Analog Card 1, Tach	

Wire Location:

S	1	F
↑	↑	↑
1st Letter (Channel)	2nd Number (Card Number)	3rd Letter or Number (Pin Number)

15-B ELECTRONIC TACH

Selector Switch Wiring Table for Indicator Lamps

Wafer Number	1	2	
S1F	A1	A1	E1F
A1F	A2	A2	
ARFI Lamp	AP	AP	ERFI Lamp
	A3	A3	
S16	B1	B1	E16
A16	B2	B2	
APFI Lamp	BP	BP	EPFI Lamp
	B3	B3	
S17	C1	C1	E17
A17	C2	C2	
A CSA Lamp	CP	CP	E CSA Lamp
	C3	C3	
S1H	D1	D1	E1H
A1H	D2	D2	
A CSB Lamp	DP	DP	E CSB Lamp
	D3	D3	

WAFERS COUNTED FROM KNOB END

15-B ELECTRONIC TACH

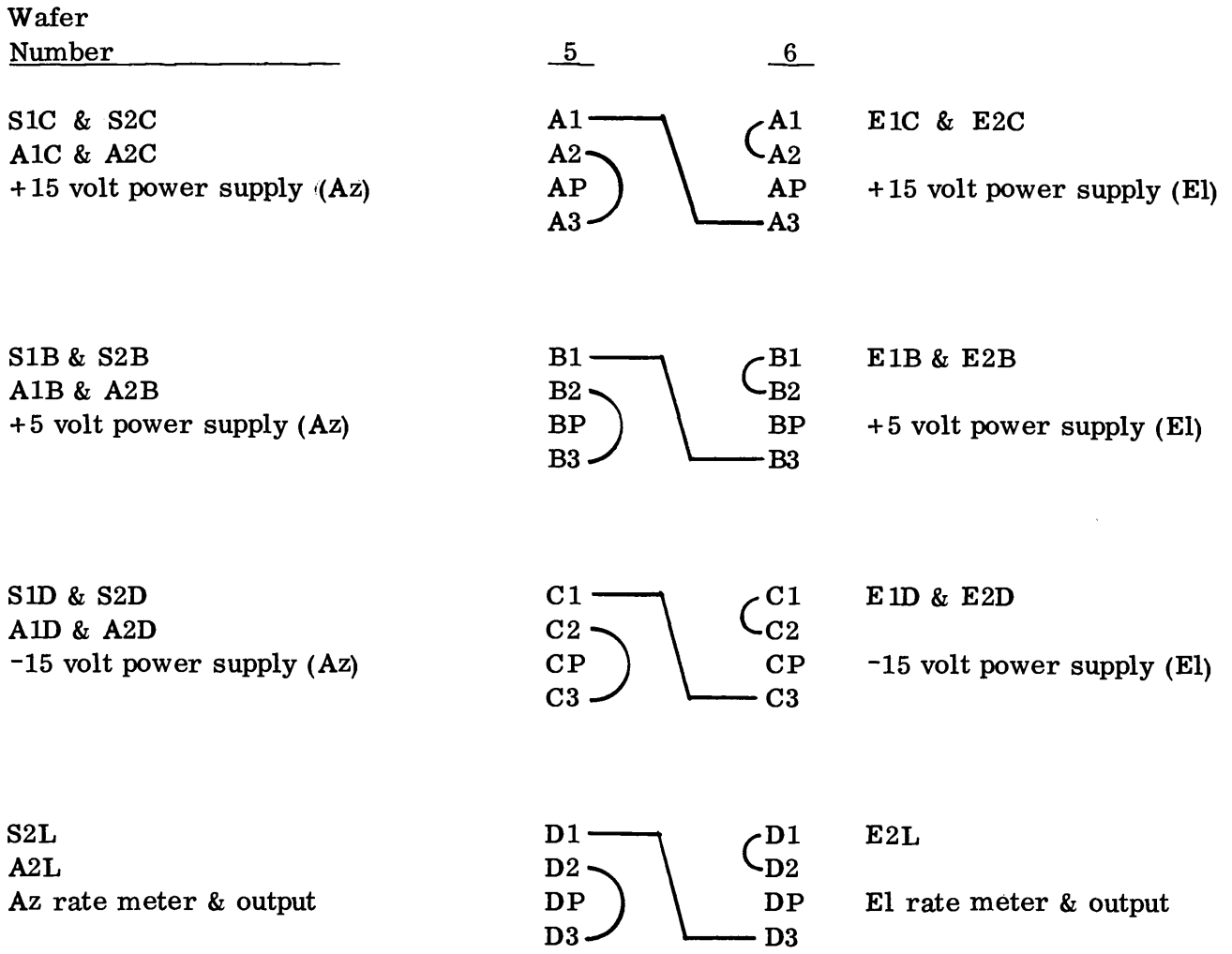
Selector Switch Wiring Table for Meters

Wafer Number	3	4	
S2Y A2Y Az position meter Channel A (-) term	A1 A2 AP A3	A1 A2 AP A3	E2Y El position meter Channel A (-) term
S2Z A2Z Az position meter Channel A (+) term	B1 B2 BP B3	B1 B2 BP B3	E2Z El position meter Channel A (+) term
S2S A2S Az position meter Channel B (-) term	C1 C2 CP C3	C1 C2 CP C3	E2S El position meter Channel B (-) term
S3T A2T Az position meter Channel B (+) term	D1 D2 DP D3	D1 D2 DP D3	E2T El position meter Channel B (+) term

WAFERS COUNTED FROM KNOB END

15-B ELECTRONIC TACH

Selector Switch Wiring Table for Power and Rate Output and Meter



WAFERS COUNTED FROM KNOB END

15-B ELECTRONIC TACH

Selector Switch Wiring Table for REF & PVS Twinax

Wafer Number	7	8	
S1Z A1Z Az REF input rear panel	A1 A2 AP A3	A1 A2 AP A3	E1Z El REF input rear panel
S 1 22 A 1 22 Az $\overline{\text{REF}}$ input rear panel	B1 B2 BP B3	B1 B2 BP B3	S 1 22 El $\overline{\text{REF}}$ input rear panel
S 1 X A 1 X Az PVS input rear panel	C1 C2 CP C3	C1 C2 CP C3	E 1 X El PVS input rear panel
S 1 20 A 1 20 Az $\overline{\text{PVS}}$ input rear panel	D1 D2 DP D3	D1 D2 DP D3	E 1 20 El $\overline{\text{PVS}}$ input rear panel

WAFERS COUNTED FROM KNOB END

15-B ELECTRONIC TACH

Selector Switch Wiring Table for Spare Indicator Lamp

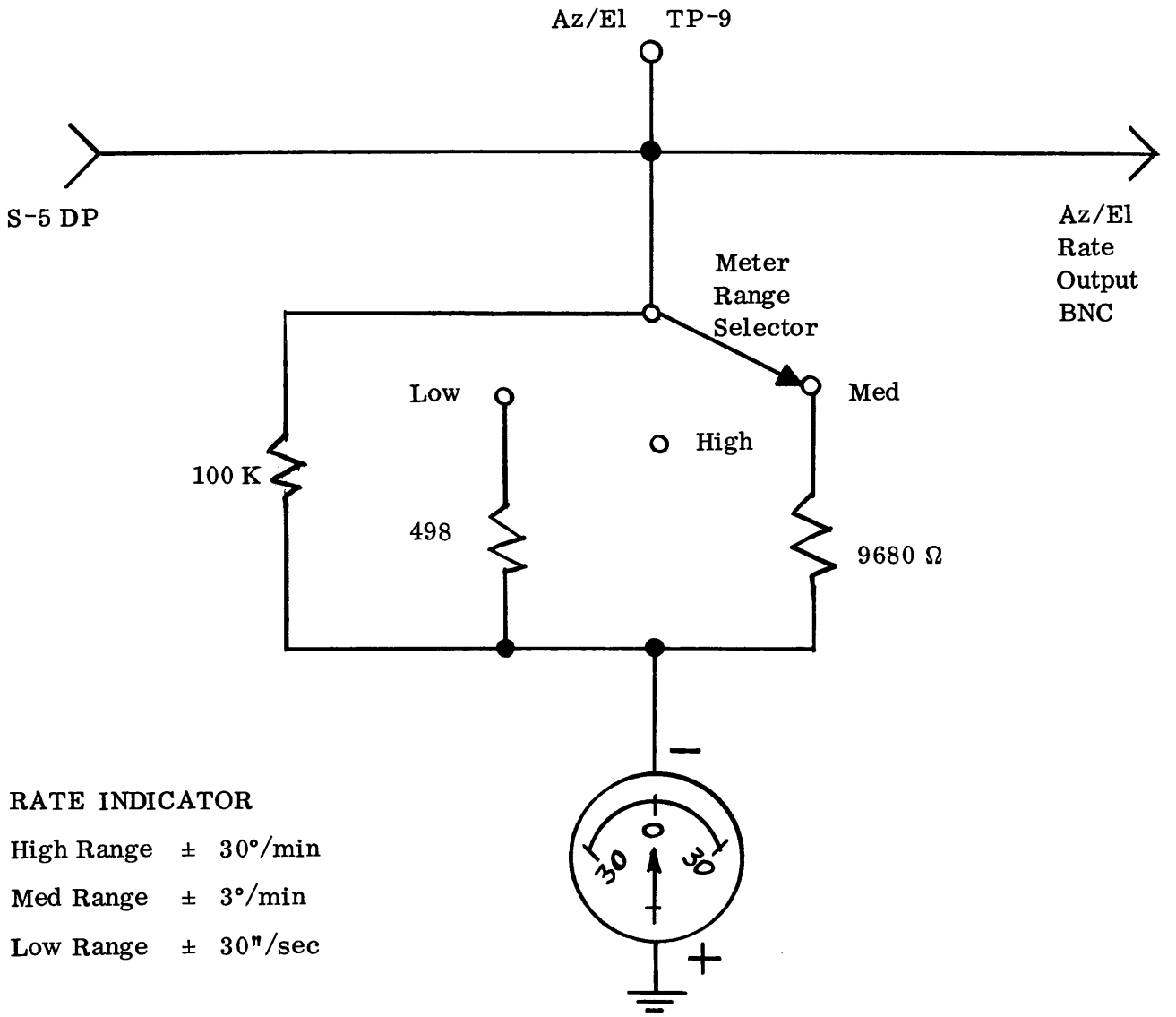
Wafer Number	9
Ground	A1
NC	A2
Spare Indicator Lamp through 100 ohm resistor	AP
Ground	A3

WAFERS COUNTED FROM KNOB END

Test Points Wire List

From	To		Function
TP-1	2A		Ground
TB-2	7/8 AP	through 1 K Ω	REF
TP-3	7/8 BP	through 1 K Ω	$\overline{\text{REF}}$
TP-4	7/8 CP	through 1 K Ω	PVS
TP-5	7/8 DP	through 1 K Ω	$\overline{\text{PVS}}$
TP-6	1/2 DP		Channel Switch
TP-7	A/E-2-U17		Position Channel A
TP-8	A/E-2-S15		Position Channel B
TP-9	5/6 DP		Rate

15-B ELECTRONIC TACH



RATE INDICATOR

High Range ± 30°/min

Med Range ± 3°/min

Low Range ± 30"/sec