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A 50-CHANNEL MULTIFILTER RECEIVER
(1.2 MHz Bandwidth Per Channel)

N. V. G. Sarma

EDIR No. 117 - Make following changes:

Page 5, Figure 5, change "temperature" to "output voltage".
Make this same change in the actual figure title.

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General

The multifilter receiver described in this report utilizes the general design principle of using several filters with different center frequencies and a common local oscillator to synthesize a band. The filter bandwidth (-3 dB) is 1.2 MHz (nominal) and the separation between adjacent channels is also 1.2 MHz (nominal). The receiver can be used either as a contiguous comb of 50 filters (series mode) or as two identical sets of contiguous comb of 25 filters (parallel mode) each. In the series mode of operation, an IF input band covering the frequency range 120.6 to 179.4 MHz is synthesized. In the parallel mode of operation, an IF input band covering the frequency range 135.6 to 164.4 MHz is synthesized. One special feature that is incorporated in this receiver is the provision of a test noise source which may help in the adjustment of gain and square law characteristics of individual channels.

The receiver is contained in two chassis, one containing the power supplies and temperature control circuitry and the other containing the rest of the receiver. Provision has been made to temperature control the plates on which square law detectors and DC amplifiers are mounted. This may be wired in at a future date after seeing the performance for some time without temperature control.

Description

A block diagram of the receiver is shown in Figure 1. Front panel and the component layout are shown in Figure 2 and a front view of the power supply chassis is shown in Figure 3. Channels 1 to 25 and part of the IF circuitry are housed in the top deck of the chassis, whereas channels 26 to 50 and the rest of the IF circuitry are housed in the bottom deck of the chassis. Bandpass filters used are the tubular bandpass filters manufactured by Lark Engineering Company. Their center frequencies range from 70.6 MHz to 99.4 MHz with an increment of 1.2 MHz. Due to poor workmanship and quality control, we had to accept errors of ± 0.2 MHz in center frequency as well as bandwidth even though our original, agreed specification is ± 0.1 MHz. Channels 1 to 25 are obtained by mixing the input IF signals with a local oscillator

frequency of 220 MHz and channels 26 to 50 are obtained in a similar manner by mixing with a local oscillator frequency of 250 MHz. In the parallel mode, the input IF signals are mixed with a local oscillator frequency of 235 MHz. Each driver-amplifier drives four filters and associated square law detectors and DC amplifiers. The driver-amplifier is type UA-305 manufactured by Avantek. The 1 dB output compression point is +20 dBm.

Front and Rear Panel Controls

IF input signal levels can be adjusted to the desired level by operating the Gain Control attenuator. This control is effective only in the series mode operation. In this mode of operation, an IF input power of -50 dBm over 80 MHz band will produce (with 10 dB in the Gain Control attenuator) an output DC signal of about 2 volts. Total power outputs from any channel can be displayed on the front panel meter by switching on the appropriate switch on the front panel. The meter sensitivity, 4 V or 10 V full scale, can also be chosen by a front panel switch. Total power output of any channel, selected by a switch, is also available at the BNC connector marked "Meter Output".

In the parallel mode of operation, gain control attenuators are cut out of the circuit and IF gain has to be adjusted externally to the 50-channel receiver. An IF signal power of -40 dBm over 80 MHz bandwidth is required to produce 2 V output DC signal.

System can be converted from series mode to parallel mode by changing the patch-cord connections at the rear panel. Also situated at the rear panel are the "Zero Test" control input signal, test noise source output which can be fed into the receiver input by means of a cable, total power DC output connectors J1 and J2 for the computer, and a round connector through which power supply voltages are brought in. The test noise source output is adjusted to -50 dBm and can be increased to -30 dBm, if required, by removing the attenuators located inside the chassis. Table 1 gives the filter frequencies, bandwidths, and IF input frequencies to the receiver for series mode of operation, whereas Table 2 gives the same information for parallel mode of operation. Table 3 lists the cable connections and color code for the rear panel connectors. Table 4 gives the filter and detector arrangement in banks of four.

Square Law Detector and DC Amplifier Circuit

Figure 4 shows the circuit diagram of square-law detector and DC amplifier combination. BD7 back diode manufactured by G.E. is used as a square-law detector diode. It is found to have excellent temperature coefficient as well as good square-law characteristics at power levels up to -20 dBm. Analog Devices AD741L integrated circuit operational amplifier follows the square-law detector for amplification of the detected voltage to the required level. Figure 5 gives the error from perfect square-law characteristics vs. output DC voltage. At the normal operating level of 2 V, the error is never more than 2% for any detector. Zero offset and gain of the DC amplifier can be adjusted by trim pots.

Monitor Circuits

Figure 6 shows the circuit diagram of the meter amplifier. It is mounted in the lefthand corner near the front panel. The offset voltage can be adjusted to zero by means of the trim pot. Figure 7 gives the circuit diagram of the driver for zero test relay. When the zero test input port (on the rear panel) is either terminated or 0 V is applied, the relay opens and cuts off the DC powers (+15 V and -15 V) applied to the IF amplifiers (SC330 and NRAO-WB2 amplifiers), so there is no input IF power to the detectors. Figure 8 shows the circuit diagram of the power supply monitor circuit. The power supplies are read on the front panel meter mounted on the power supply chassis. When the voltages are correct, they should all read center scale.

Test Procedure and Some Performance Results

1. Connect a digital voltmeter to the BNC connector marked "Meter Output". With no input to the 50-channel receiver and with all the switches on the front panel in OFF position, adjust meter amplifier trim pot to read zero volts on DVM.

2. With no input to the 50-channel receiver (or "Zero Test" input terminated in 50 ohms) adjust the offset voltages of each channel to zero, selecting them one by one by means of the front panel switches.

3. Connect the test noise source output to the input of the 50-channel receiver. All the total power DC outputs should read around 2 volts. If not, adjust the gains of the DC amplifiers for equality of outputs.

When the gains are all adjusted in the series mode, it is found that they are no longer the same when switched over to parallel mode. All the channels connected to 1N. 1. 25 Ch (marked A in Table 2) have about 2 dB less gain when compared to those connected to 1N. 2. 25 Ch (marked B in Table 2). Hence, a fixed gain offset of about 2 dB is required external to the receiver when it is operated in parallel mode. These gain differences are due to the ripple in the IF band.

4. Detector law adjustment potentiometers were all set for best performance around 2 V output level.

An attempt is made to determine the gain coefficient of the receiver against temperature variation and power supply variation. A 1% change in supply voltage (+15 V and -15 V) produces a 2. 5% change in the total power output DC voltage. The gain coefficient vs. temperature is found to be 0. 07 dB/°C. Band shapes have been measured for some of the channels and Figure 9 shows the response characteristics for Channels 23, 24, 25, 26 and 27. There is about 10 dB isolation between adjacent channels.

Acknowledgments

P. Camana has participated in the initial design of the receiver. R. Ervine has helped in the construction of the receiver. D. S. Weinreb has provided the general guidance. I have had many helpful discussions with M. Balister during the course of this project.

LIST OF FIGURES

TABLE 1

Filter and IF Frequencies for Series Mode Operation

Channel No.	Filter Center Frequency MHz		Bandwidth MHz	IF Input MHz		Frequency Separation MHz
	Nominal	Measured	Measured	Nominal	Measured	
1	99.4	99.29	1.23	120.6	120.71	
2	98.2	98.19	1.28	121.8	121.81	1.10
3	97.0	97.01	1.19	123.0	122.99	1.18
4	95.8	95.77	1.17	124.2	124.23	1.24
5	94.6	94.49	1.22	125.4	125.51	1.28
6	93.4	93.41	1.18	126.6	126.59	1.08
7	92.2	92.32	1.38	127.8	127.68	1.09
8	91.0	91.18	1.38	129.0	128.82	1.13
9	89.8	89.65	1.31	130.2	130.35	1.53
10	88.6	88.65	1.30	131.4	131.35	1.00
11	87.4	87.34	1.32	132.6	132.66	1.31
12	86.2	86.25	1.30	133.8	133.75	1.09
13	85.0	85.05	1.10	135.0	134.95	1.20
14	83.8	83.8	1.05	136.2	136.2	1.25
15	82.6	82.45	1.25	137.4	137.55	1.35
16	81.4	81.52	1.35	138.6	138.48	0.90
17	80.2	80.10	1.15	139.8	139.90	1.42
18	79.0	78.94	1.21	141.0	141.06	1.16
19	77.8	77.61	1.21	142.2	142.39	1.33
20	76.6	76.60	1.19	143.4	143.40	1.01
21	75.4	75.40	1.00	144.6	144.60	1.20
22	74.2	74.26	1.28	145.8	145.74	1.14
23	73.0	73.0	1.25	147.0	147.00	1.26
24	71.8	71.90	1.20	148.2	148.10	1.10
25	70.6	70.60	1.25	149.4	149.40	1.30

Continued --

TABLE 1 (Continued)

Channel No.	Filter Center Frequency MHz		Bandwidth MHz	IF Input MHz		Frequency Separation MHz
	Nominal	Measured	Measured	Nominal	Measured	
26	99.4	99.57	1.25	150.6	150.43	1.05
27	98.2	98.00	1.25	151.8	152.00	1.57
28	97.0	96.97	1.34	153.0	153.03	1.03
29	95.8	95.72	1.25	154.2	154.28	1.25
30	94.6	94.53	1.26	155.4	155.47	1.19
31	93.4	93.47	1.26	156.6	156.53	1.06
32	92.2	92.08	1.28	157.8	157.92	1.39
33	91.0	90.89	1.16	159.0	159.11	1.19
34	89.8	89.72	1.35	160.2	160.28	1.17
35	88.6	88.7	1.38	161.4	161.30	1.02
36	87.4	87.37	1.39	162.6	162.63	1.33
37	86.2	86.35	1.29	163.8	163.65	1.02
38	85.0	84.98	1.30	165.0	165.02	1.37
39	83.8	83.78	1.35	166.2	166.22	1.20
40	82.6	82.54	1.25	167.4	167.48	1.26
41	81.4	81.45	1.30	168.6	168.55	1.08
42	80.2	80.25	1.30	169.8	169.75	1.20
43	79.0	78.98	1.24	171.0	171.02	1.27
44	77.8	77.85	1.39	172.2	172.15	1.13
45	76.6	76.67	1.33	173.4	173.33	1.18
46	75.4	75.25	1.40	174.6	174.75	1.42
47	74.2	74.12	1.04	175.8	175.88	1.13
48	73.0	72.99	1.28	177.0	177.01	1.13
49	71.8	71.64	1.28	178.2	178.36	1.35
50	70.6	70.49	1.28	179.4	179.51	1.15

TABLE 2

IF Frequencies for Parallel Mode Operation

Channel No.	IF Input MHz		Channel No.	IF Input MHz	
	Nominal	Measured		Nominal	Measured
A 1	135.6	135.71	B 1	135.6	135.43
2	136.8	136.81	2	136.8	137.00
3	138.0	137.99	3	138.0	138.03
4	139.2	139.23	4	139.2	139.28
5	140.4	140.51	5	140.4	140.47
6	141.6	141.59	6	141.6	141.53
7	142.8	142.68	7	142.8	142.92
8	144.0	143.82	8	144.0	144.11
9	145.2	145.35	9	145.2	145.28
10	146.4	146.35	10	146.4	146.30
11	147.6	147.66	11	147.6	147.63
12	148.8	148.75	12	148.8	148.65
13	150.0	149.95	13	150.0	150.02
14	151.2	151.2	14	151.2	151.22
15	152.4	152.55	15	152.4	152.48
16	153.6	153.48	16	153.6	153.55
17	154.8	154.90	17	154.8	154.75
18	156.0	156.06	18	156.0	156.02
19	157.2	157.39	19	157.2	157.15
20	158.4	158.40	20	158.4	158.33
21	159.6	159.60	21	159.6	159.75
22	160.8	160.74	22	160.8	160.88
23	162.0	162.00	23	162.0	162.01
24	163.2	163.10	24	163.2	163.36
25	164.4	164.40	25	164.4	164.51

TABLE 3

Back Panel Connectors, Cable Connection, and Color Coding

Channel	Color	Connector	Pin
1	S Yellow	J-2	EE
1	R Black	J-2	FF
26	S Violet	J-1	CC
26	R Black	J-1	DD
2	S Blue	J-2	HH
2	R Black	J-2	JJ
27	S Red	J-2	A
27	R Black	J-2	B
3	S Orange	J-1	A
3	R Black	J-1	B
28	S Green	J-2	C
28	R Black	J-2	D
4	S Gray	J-1	C
4	R Black	J-1	D
29	S White	J-2	E
29	R Black	J-2	F
5	S Yellow	J-1	E
5	R Black	J-1	F
30	S Violet	J-2	H
30	R Black	J-2	J
6	S Blue	J-1	H
6	R Black	J-1	J
31	S Red	J-2	K
31	R Black	J-2	L
7	S Orange	J-1	K
7	R Black	J-1	L
32	S Green	J-2	M
32	R Black	J-2	N
8	S Gray	J-1	M
8	R Black	J-1	N
33	S White	J-2	P
33	R Black	J-2	R
9	S Yellow	J-1	P
9	R Black	J-1	R
34	S Violet	J-2	S
34	R Black	J-2	T
10	S Blue	J-1	S
10	R Black	J-1	T
35	S Red	J-2	U
35	R Black	J-2	V
11	S Orange	J-1	U
11	R Black	J-1	V
36	S Green	J-2	W
36	R Black	J-2	X
12	S Gray	J-1	W
12	R Black	J-1	X
37	S White	J-2	Y
37	R Black	J-2	Z
13	S Yellow	J-1	Y
13	R Black	J-1	Z
38	S Violet	J-2	a
38	R Black	J-2	b
14	S Blue	J-1	a
14	R Black	J-1	b
39	S Red	J-2	c
39	R Black	J-2	d

TABLE 3 - page 2

Channel	Color	Connector	Pin
15	S Orange	J-1	c
15	R Black	J-1	d
40	S Green	J-2	e
40	R Black	J-2	f
16	S Gray	J-1	e
16	R Black	J-1	f
41	S White	J-2	h
41	R Black	J-2	j
17	S Yellow	J-1	h
17	R Black	J-1	j
42	S Violet	J-2	k
42	R Black	J-2	l
18	S Blue	J-1	k
18	R Black	J-1	l
43	S Red	J-2	m
43	R Black	J-2	n
19	S Orange	J-1	m
19	R Black	J-1	n
44	S Green	J-2	p
44	R Black	J-2	r
20	S Gray	J-1	p
20	R Black	J-1	r
45	S White	J-2	s
45	R Black	J-2	t
21	S Yellow	J-1	s
21	R Black	J-1	t
46	S Violet	J-2	u
46	R Black	J-2	v

Channel	Color	Connector	Pin
22	S Blue	J-1	u
22	R Black	J-1	v
47	S Red	J-2	w
47	R Black	J-2	x
23	S Orange	J-1	w
23	R Black	J-1	x
48	S Green	J-2	y
48	R Black	J-2	z
24	S Gray	J-1	y
24	R Black	J-1	z
49	S White	J-2	AA
49	R Black	J-2	BB
25	S Yellow	J-1	AA
25	R Black	J-1	BB
50	S Violet	J-2	CC
50	R Black	J-2	DD
Total Power 1-25	S Black	J-1	EE
	R	J-1	FF
Total Power 26-50	S Black	J-2	KK
	R	J-2	

POWER CONNECTOR

AC Connector In	DC Connector Out		
A AC	A	+15 V	Red
B AC	B	-15 V	Orange
C Gnd	C	± 15 V Ret	Black
	D	+12 V	Blue
	E	+12 V Ret	Green
	F	+28 V	Yellow
	G	+28 V Ret	Green

TABLE 4

Filter and Detector Arrangement

Top Side			Bottom Side		
Ch. No.	Filter Freq. (MHz)		Ch. No.	Filter Freq. (MHz)	
2	98.2)		26	99.4)	
8	91.0)	Det. 1	32	92.2)	Det. 8
14	83.8)	Bank	38	85.0)	Bank
20	76.6)		44	77.8)	
3	97.0)		27	98.2)	
9	89.8)	Det. 2	33	91.0)	Det. 9
15	82.6)	Bank	39	83.8)	Bank
21	75.4)		45	76.6)	
4	95.8)		28	97.0)	
10	88.6)	Det. 3	34	89.8)	Det. 10
16	81.4)	Bank	40	82.6)	Bank
22	74.2)		46	75.4)	
T. P.	1-25 Ch)		T. P.	26-50 Ch.	
1	99.4)	Det. 4	50	70.6)	Det. 11
Spare	)	Bank	Spare	)	Bank
Spare	)		Spare	)	
5	94.6)		29	95.8)	
11	87.4)	Det. 5	35	88.6)	Det. 12
17	80.2)	Bank	41	81.4)	Bank
23	73.0)		47	74.2)	
6	93.4)		30	94.6)	
12	86.2)	Det. 6	36	87.4)	Det. 13
18	79.0)	Bank	42	80.2)	Bank
24	71.8)		48	73.0)	
7	92.2)		31	93.4)	
13	85.0)	Det. 7	37	86.2)	Det. 14
19	77.8)	Bank	43	79.0)	Bank
25	70.6)		49	71.8)	

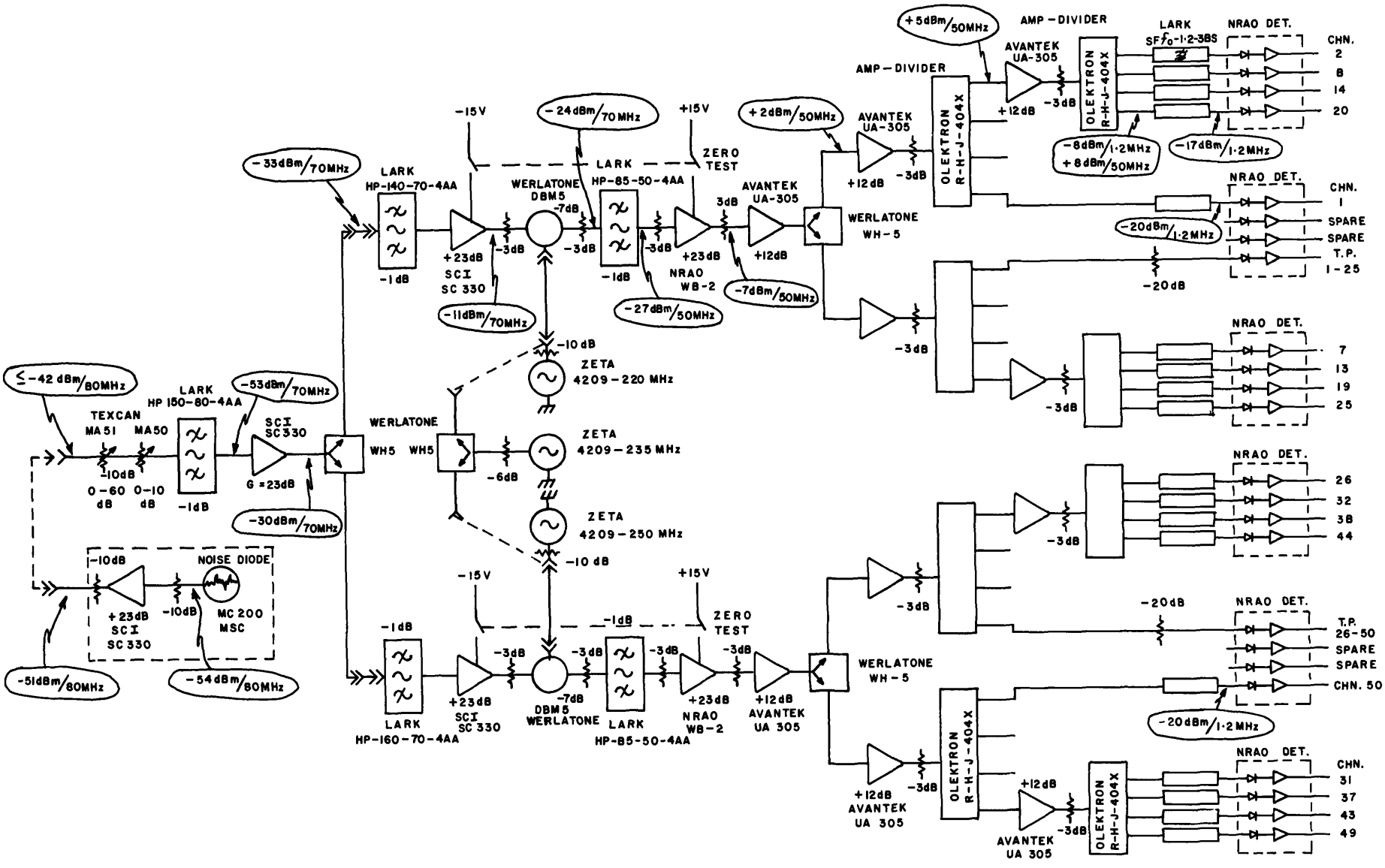


Figure 1 Block diagram of the receiver.

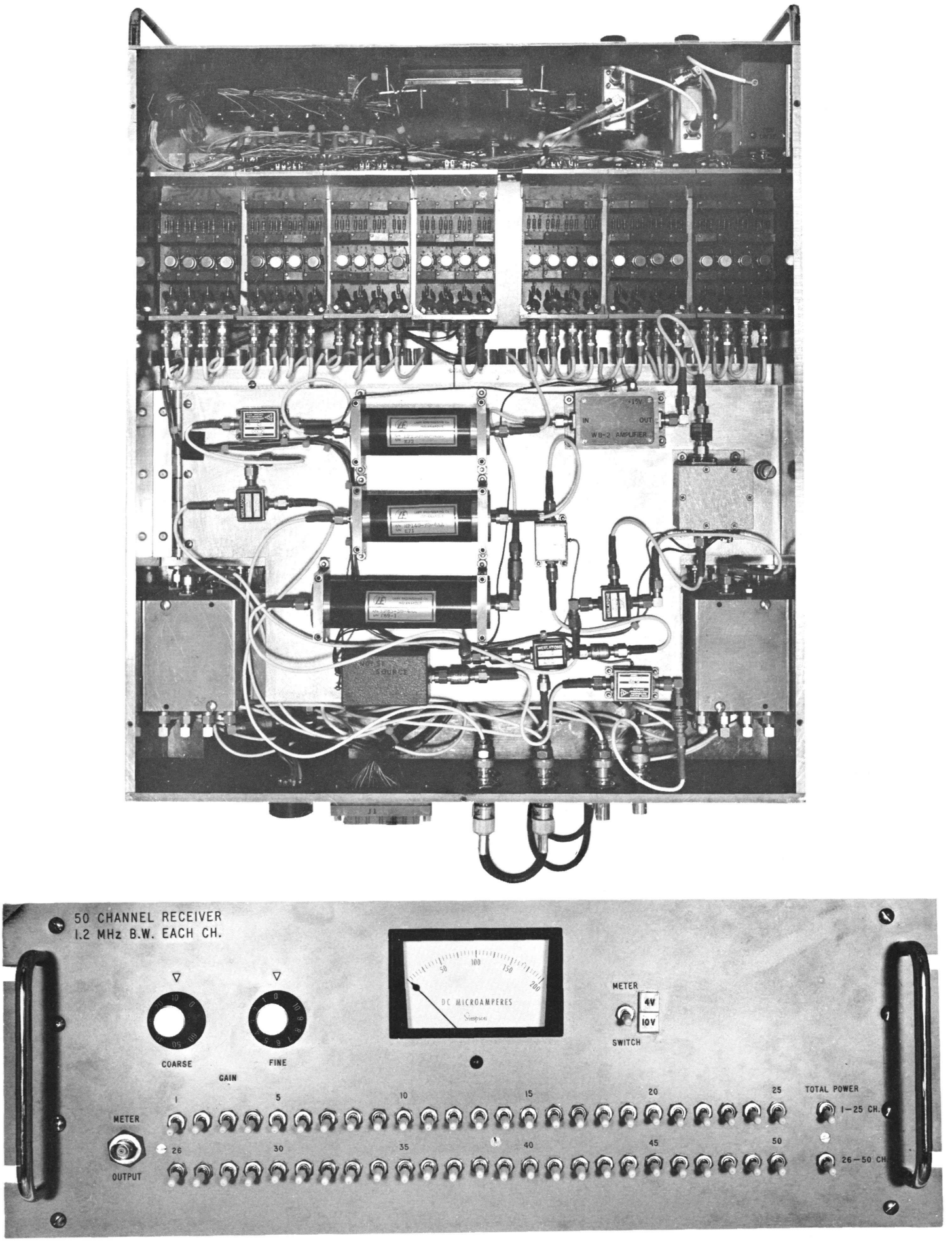


Figure 2 **Front panel and top view of the receiver.**

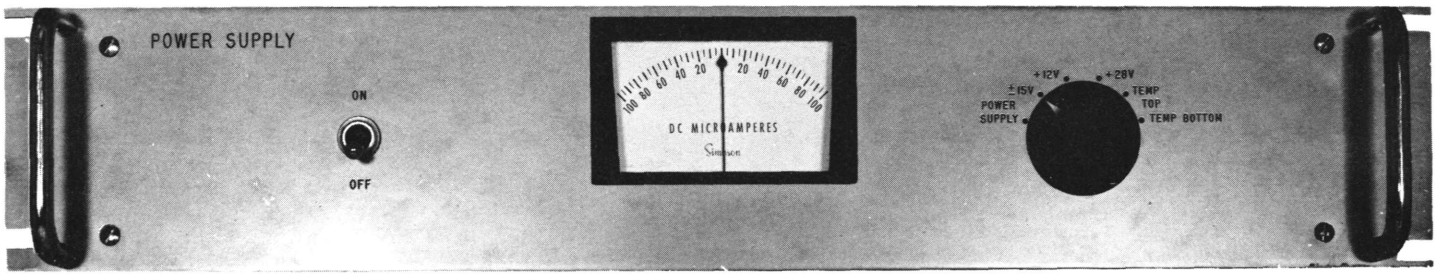
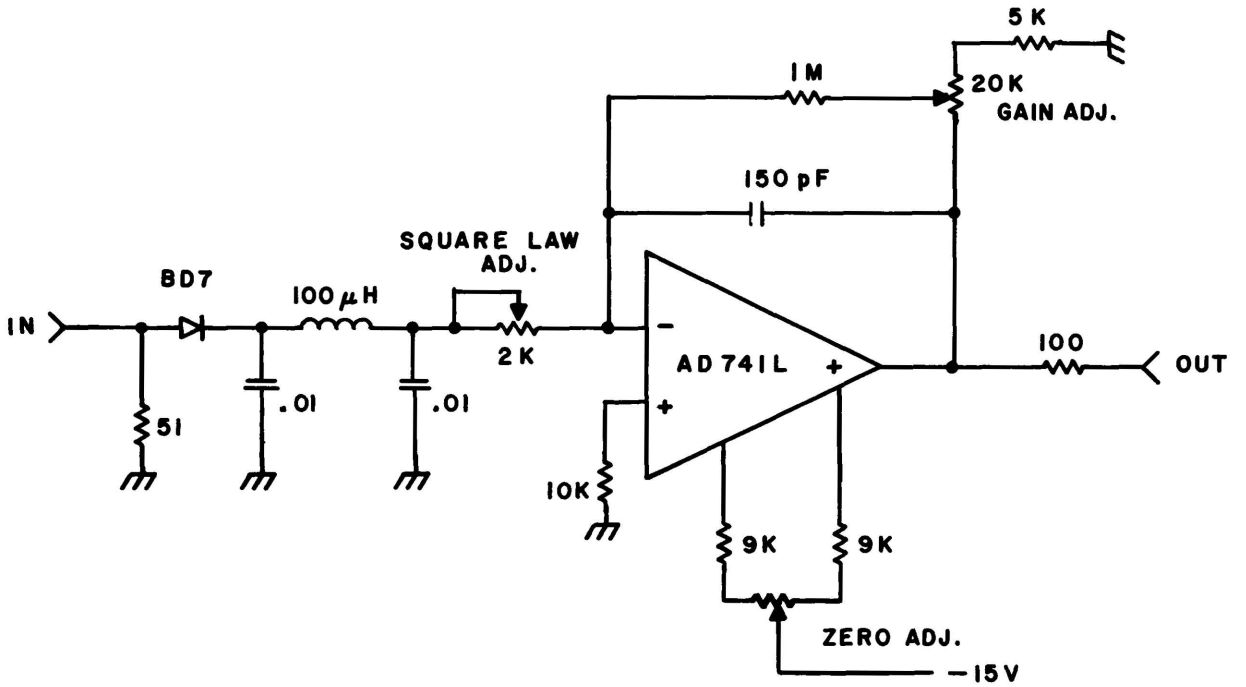


Figure 3 Front view of power supply.



FOUR SUCH CIRCUITS ARE WIRED IN ONE DETECTOR CARD.

OUTPUT PIN CONNECTIONS ON DET. CARD

1	DET. 1 OUT
2	DET. 2 OUT
3	−15 V
4	DET. 3 OUT
5	DET. 4 OUT
6	+15 V

Figure 4 Square-law detector and DC amplifier.

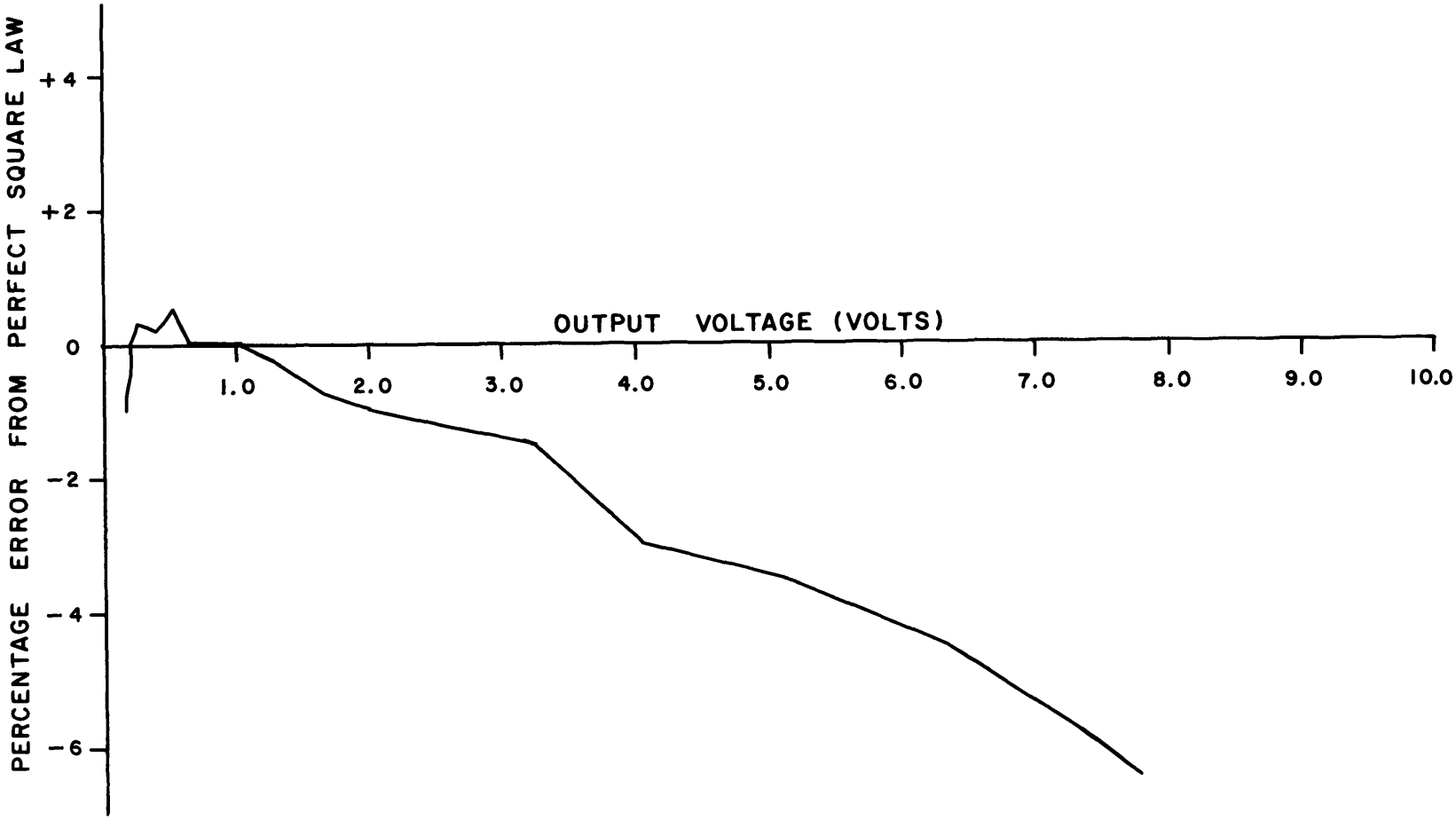


Figure 5 Error in square-law vs. temperature.

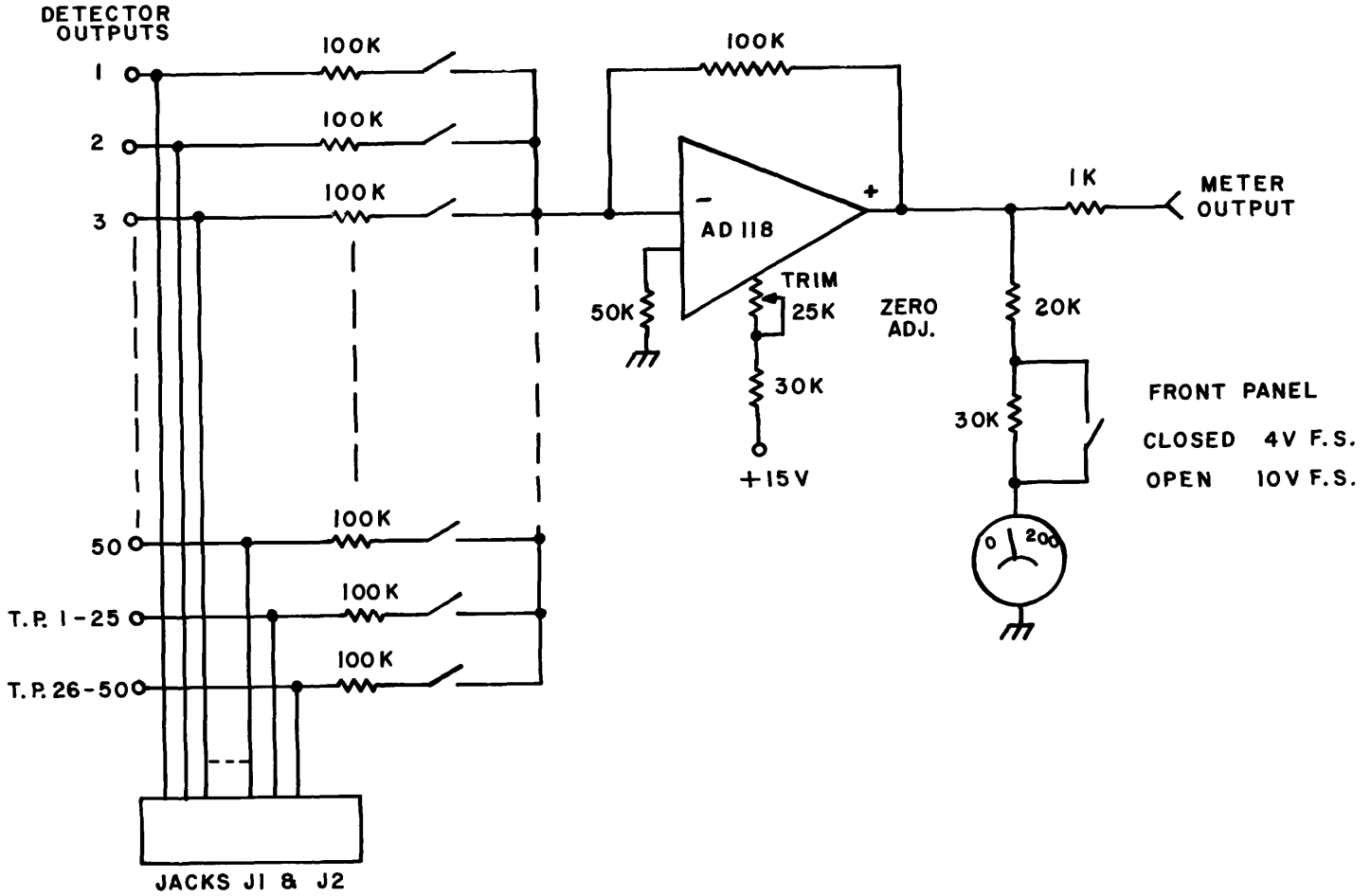
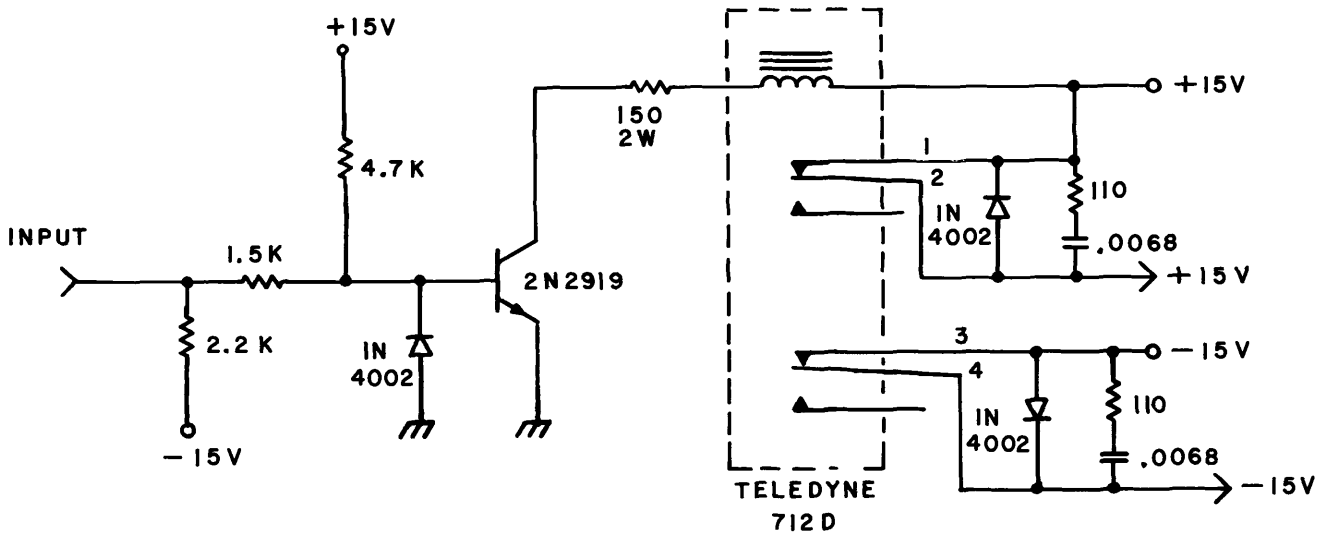


Figure 6 Meter amplifier circuit.



-6V OR OPEN CIRCUIT IS NORMAL RELAY ENERGIZED
0V OR SHORT CIRCUIT CHECKS ZEROS

Figure 7 Zero check relay circuit.

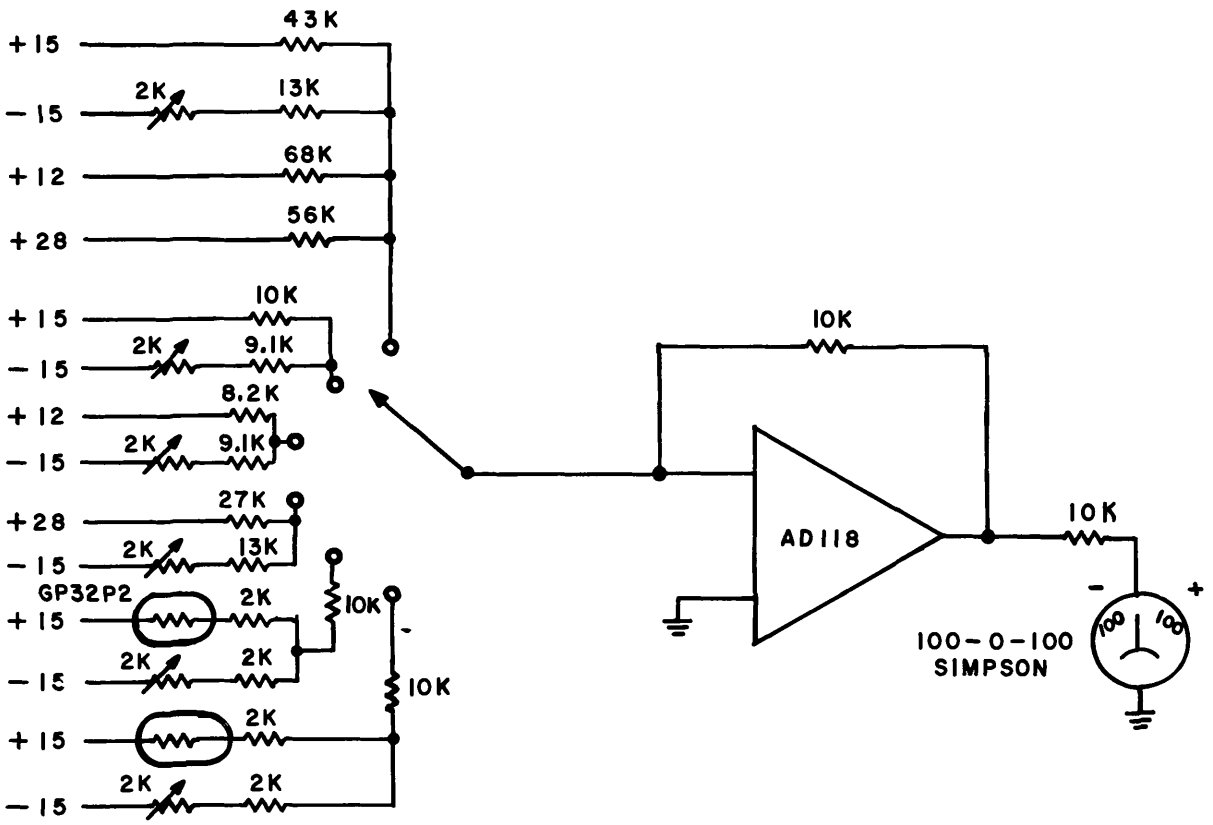


Figure 8 Power supply monitor circuit.

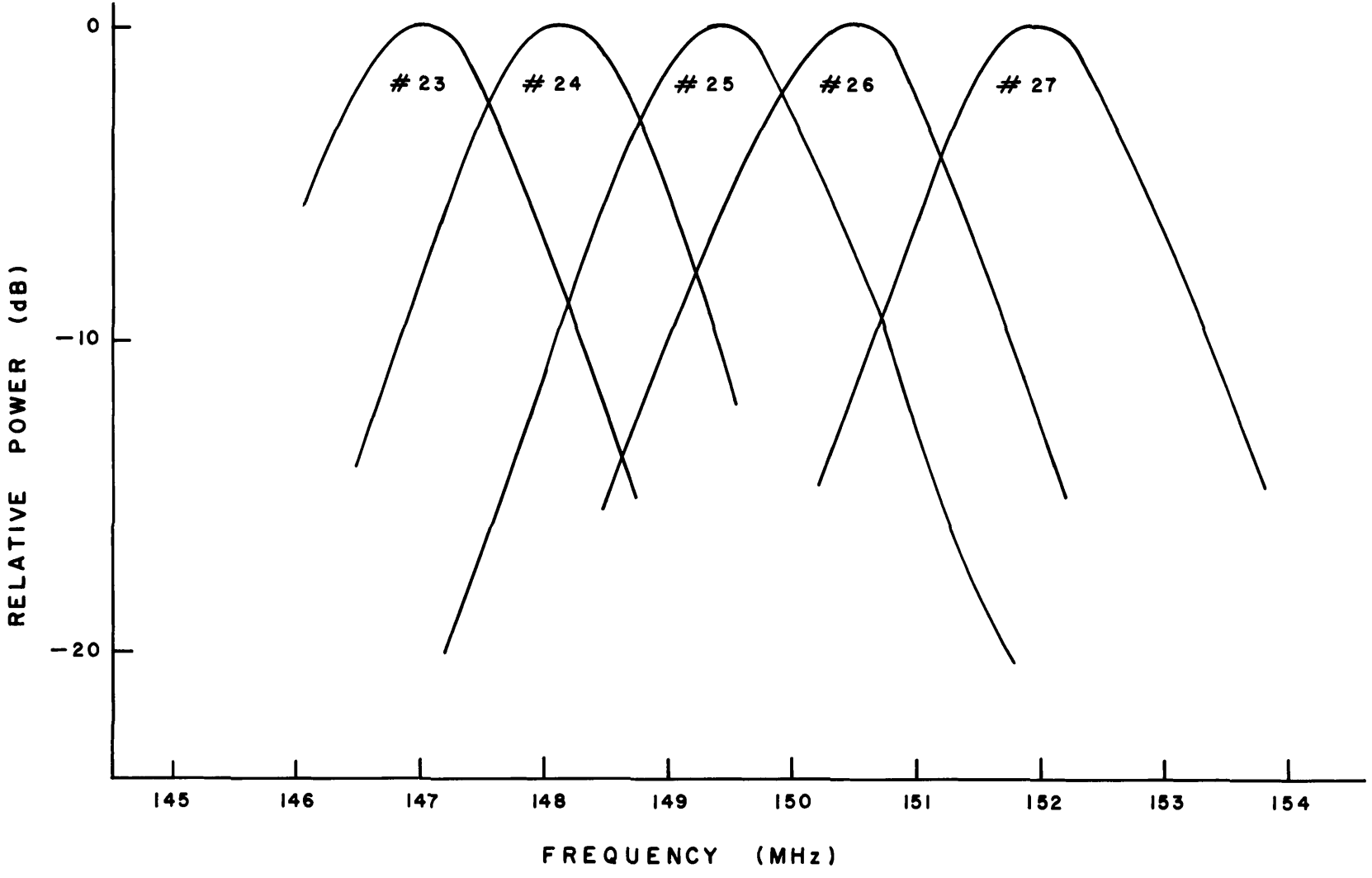


Figure 9 Band shapes of channels Nos. 23 to 27.