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NRAO STANDARD CLOCK DIVIDER AND DISPLAY

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A new standard clock has been completed comprising 4 small circuit cards, 2 power supplies, control switches, displays and chassis. The system keeps track of hours, minutes, seconds, tenths seconds, and hundredths seconds which are available on rear-mounted 56-pin Elco connectors in two formats:

1. TTL (0, +5), BCD on protected pin Elco.
2. 3-C (0, -6), BCD on exposed pin Elco.

The clock divider requires an external standard oscillator that may be either solar or sidereal 1 MHz, 2 V pp. A + or - trigger pulse of 6 volts may be applied to rear BNC connectors to provide sync when setting the clock. A day advance pulse is provided to advance the calendar system if one is used. (See Electronics Division Internal Report No. 120.) A switch selectable timing interrupt (100/50 ms) for the site computers is provided in the Elco's.

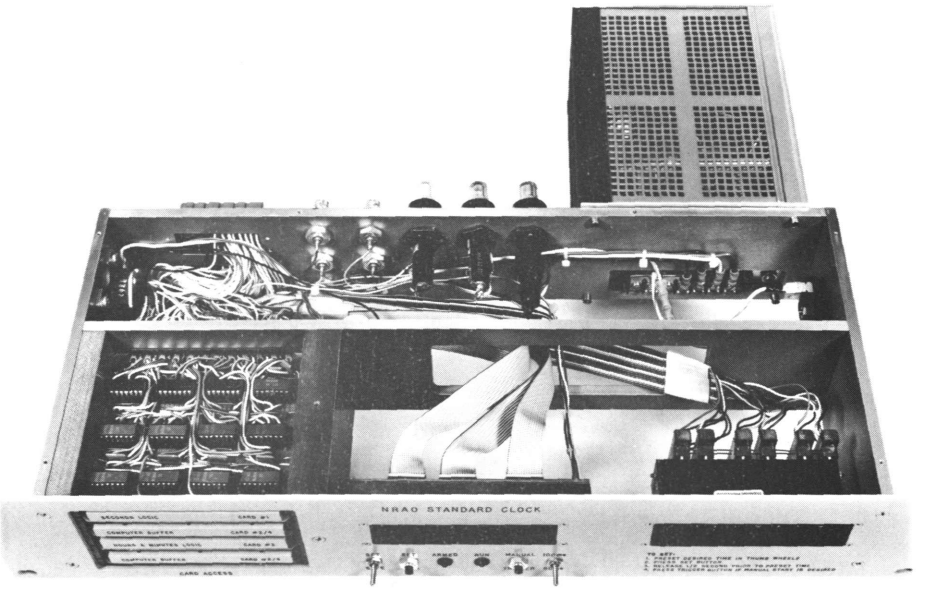
A picture of the front panel is presented showing the controls:

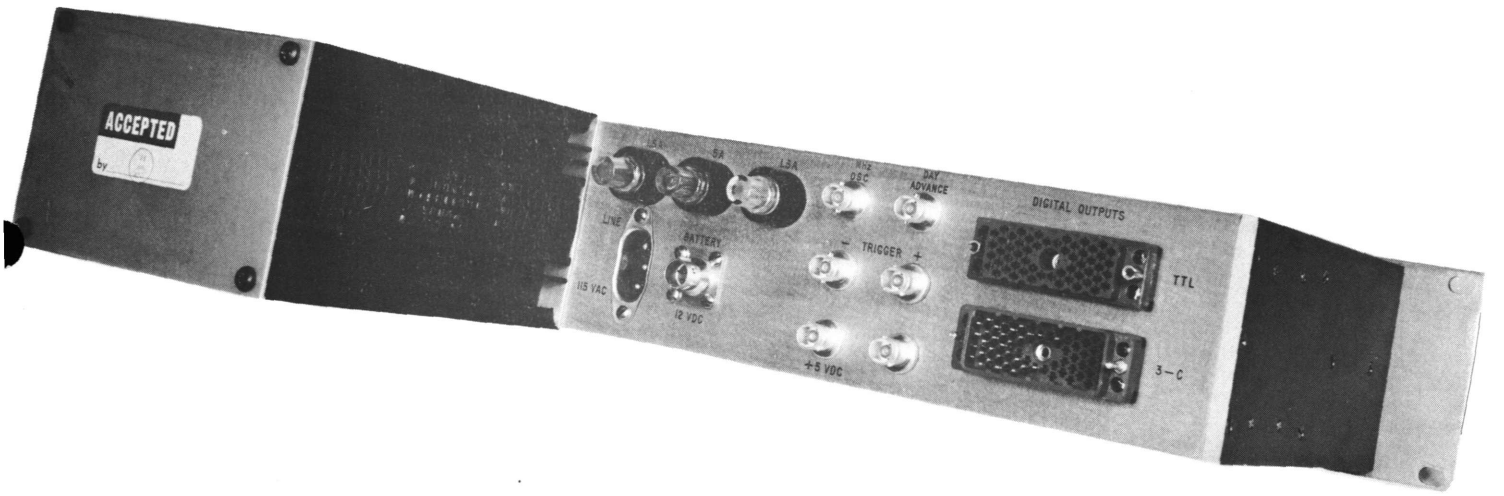
Decade LED displays provide the time readout. The circuit cards are accessible from the front panel. Several controls and display LED lamps are available for setting the clock.

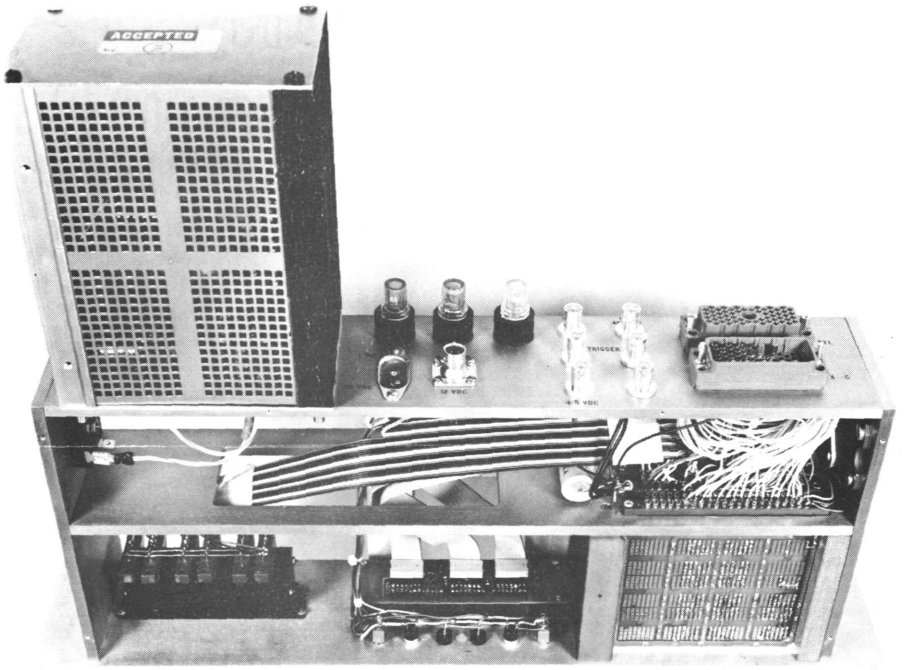
The clock may be preset with automatic sync as follows. The desired time is set into the thumbwheels. With a one second tick provided by most precision time bases connected to the proper trigger input and the set/safe switch to set, momentarily press and release the set arm push button about 1/2 second before the thumbwheel time setting. The red armed lamp will cycle on and off when the system is properly armed. The green run LED comes on when the system has been properly triggered. Manual trigger is accomplished with no external trigger attached when the manual trigger button is depressed thereby extinguishing the armed lamp and igniting the run lamp to commence counting time from the moment the button is pushed in.

The clock normally operates from a standard 115 V AC power line. A 12 V storage battery may be attached to the battery connector with pin 1 ground and pin 2 +12 V DC nominal. When the primary power fails, the battery will s upply power to the clock. About 1 1/2 amp current with a minimum of 9. 5 V DC and a maximum 30 V DC is required to power the system. When primary power returns, the battery will recharge at a rate of about 1 1/2 amps until a voltage limit set by adjusting the AC powered supply output to 13. 5 volts with the battery disconnected measure voltage at battery connector.

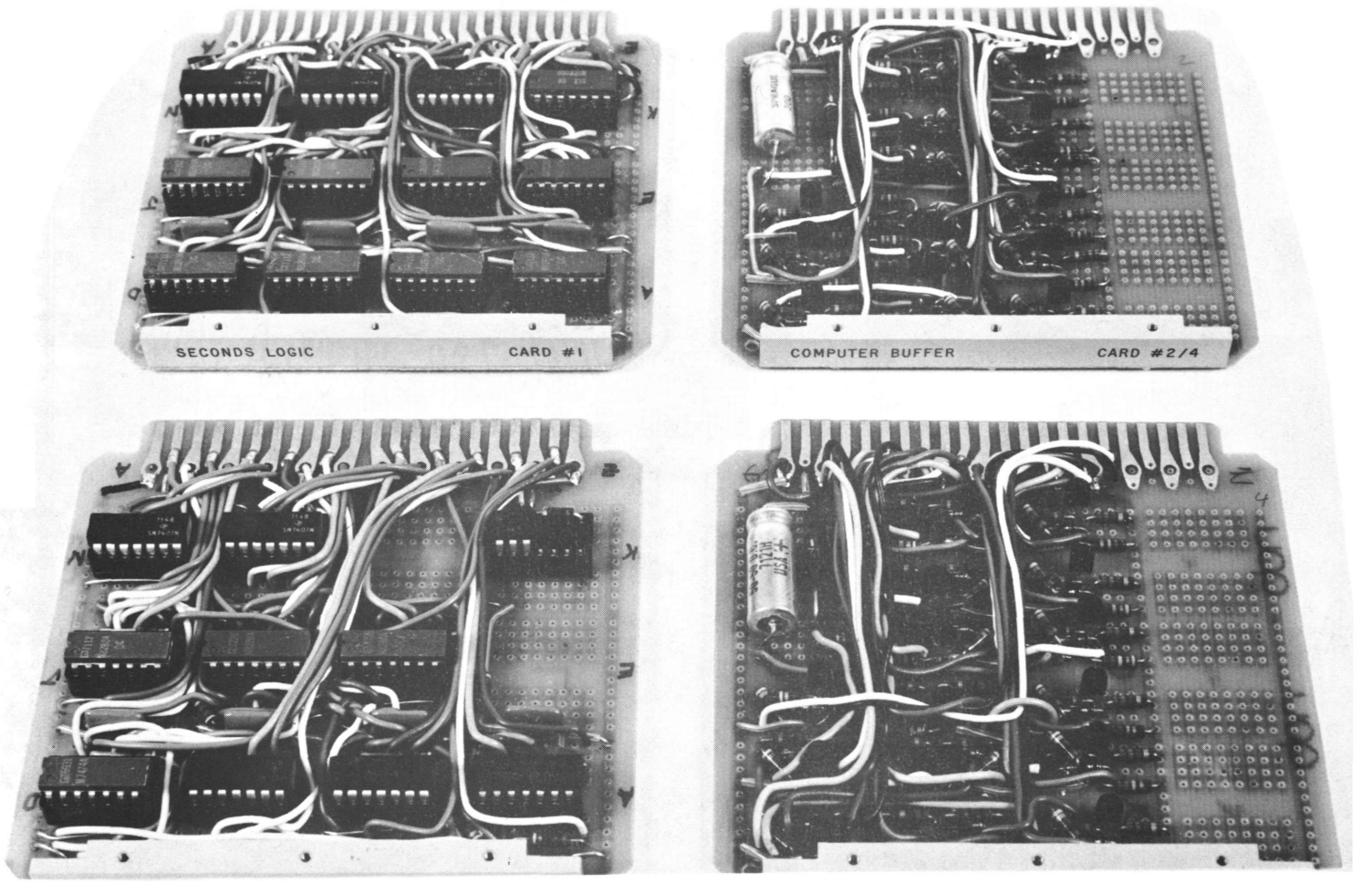
Three other pictures show the front and back views presenting the package in perspective.


NRAO STANDARD CLOCK

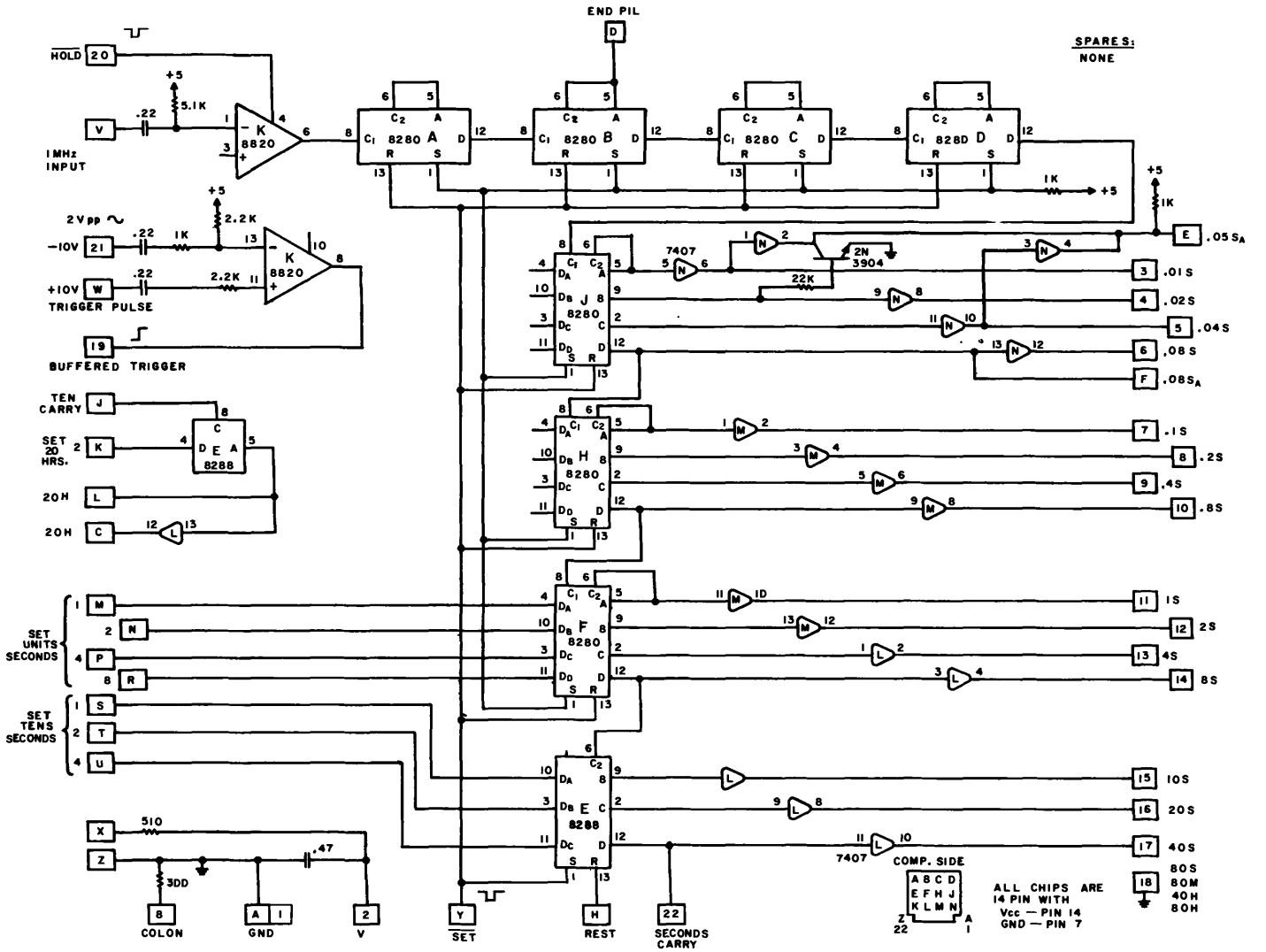

ACCEPTED
by
1SA
5A
LBA
1KHz OSC
DAY ADVANCE
DIGITAL OUTPUTS
LINE
BATTERY
TRIGGER
TTL
115 VAC
12 VDC
+5 VDC
3-C


ACCEPTED

The four circuit cards are shown below. Note that the cards 2 and 4 are identical and may be interchanged.



A schematic of the seconds logic card 1 is shown in Figure I.

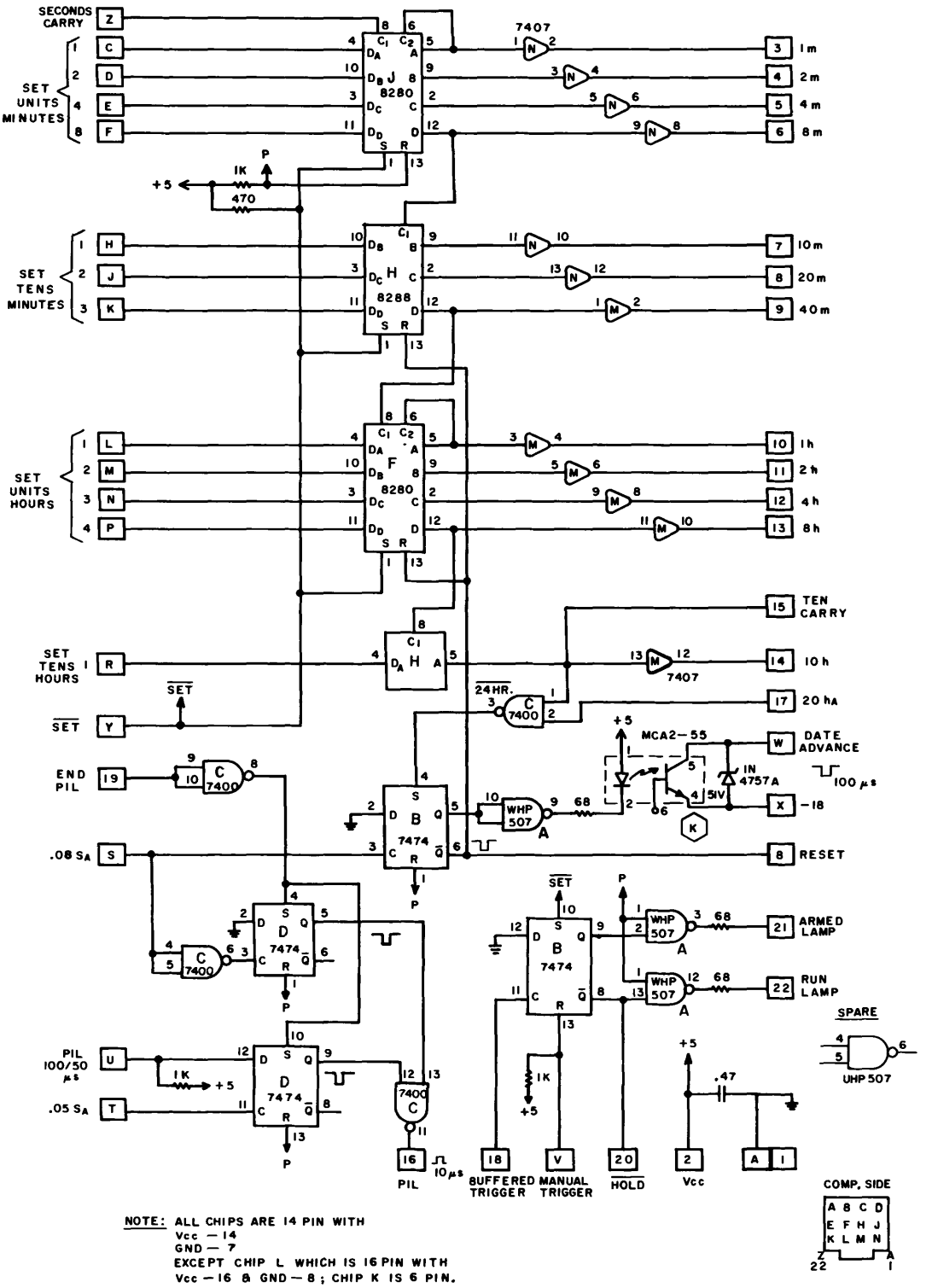


SECONDS AND FRACTIONAL SECONDS LOGIC CARD # 1

The 1 MHz reference input is at pin V AC coupled into the level shifter buffer chip K which is an 8820. The buffered output at pin 6 is divided by 8280 decade counters chips A, B, C and D, providing 100 Hz to the clock input terminal (pin 8) of chip J, which is the .01 seconds decade. The 10 Hz output of this decade is coupled to the 0.1 second decade (chip H) providing the BCD drive logic signals (via the non-inverting buffers, chip N) to the least signficant digit of the LED front panel display. Similarly the outputs of the higher order decades drive the respective digits of the display. Chip E is an 8288 which is a divide by 6 counter providing states 0-5 for the tens of seconds decade. The output of this chip provides the seconds carry (1 pulse/min) to the minutes counter on card 3 discussed later.

Pins 3 through 18 of card 1 also provide the TTL outputs to the rear panel Elco digital output connector. Pins M through U are connected to the thumbwheel switches providing the preset data.

Chip K, pin 8 provides the buffered trigger to card 3 containing the arm/trigger/hold logic. A schematic of card 3 is shown below.



NOTE: ALL CHIPS ARE 14 PIN WITH
Vcc — 14
GND — 7
EXCEPT CHIP L WHICH IS 16 PIN WITH
Vcc — 16 & GND — 8; CHIP K IS 6 PIN.

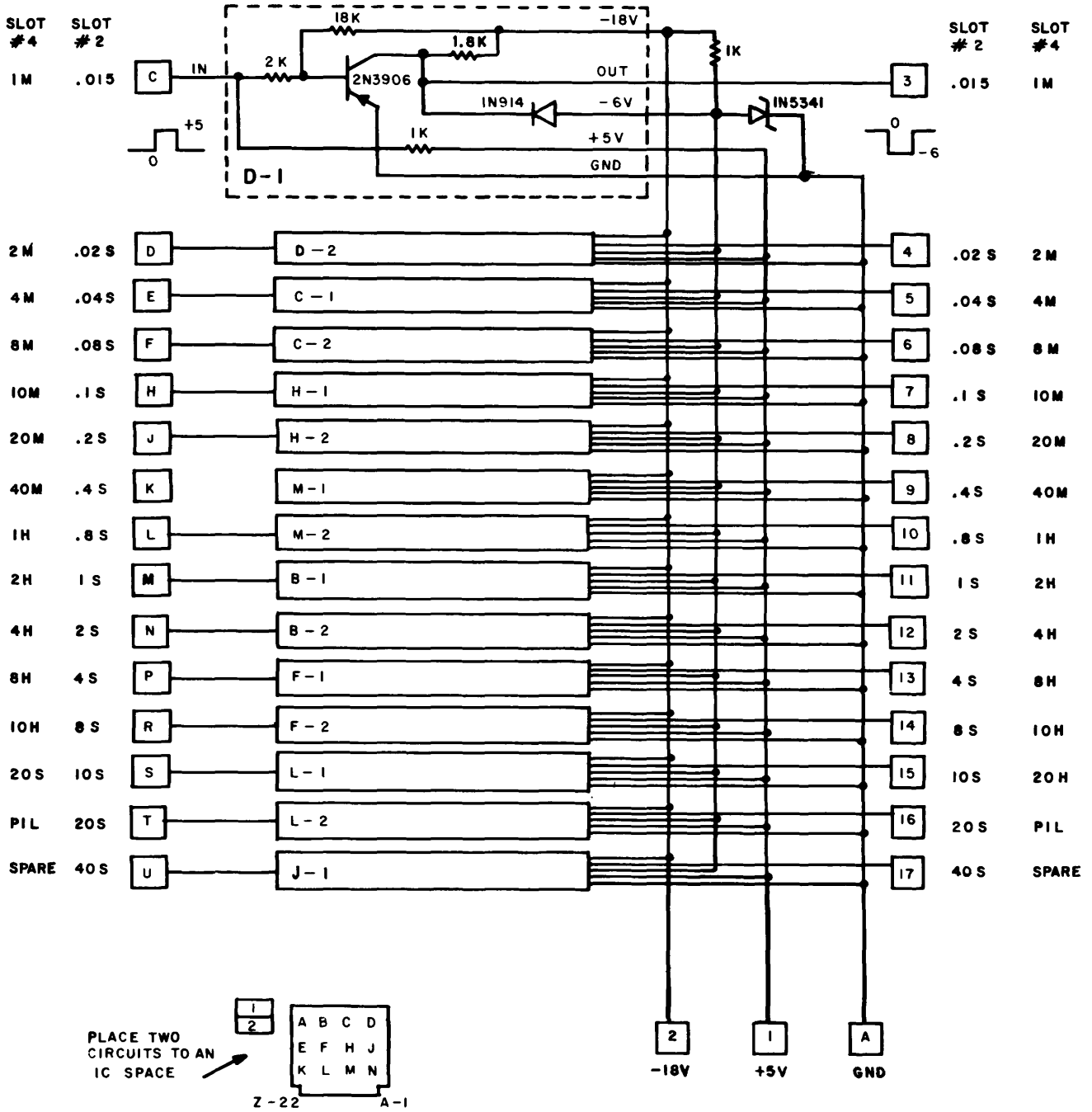
HOURS AND MINUTES LOGIC CARD # 3

Chips J, H, and F are the 1's and 10's of minutes and 1's of hours respectively. The 10's and 20's of hours comprises chip H of card 3 and chip E of card 1. Twenty-four hours is decoded by gate C-3 which sets flip-flop B-5 providing the reset pulse and day advance pulse via isolator slot K.

The run/armed logic comprises flip-flop B-9 and gates A-3 and A-12. $\overline{\text{Set}}$ provided by the set arm pushbutton sets the flip-flop thus lighting the red armed LED and applying the $\overline{\text{Hold}}$ signal to inhibit the time base buffer (chip K on card 1), thereby stopping the clock until the buffered trigger or manual trigger button resets the flip-flop B on card 3 to commence measuring time.

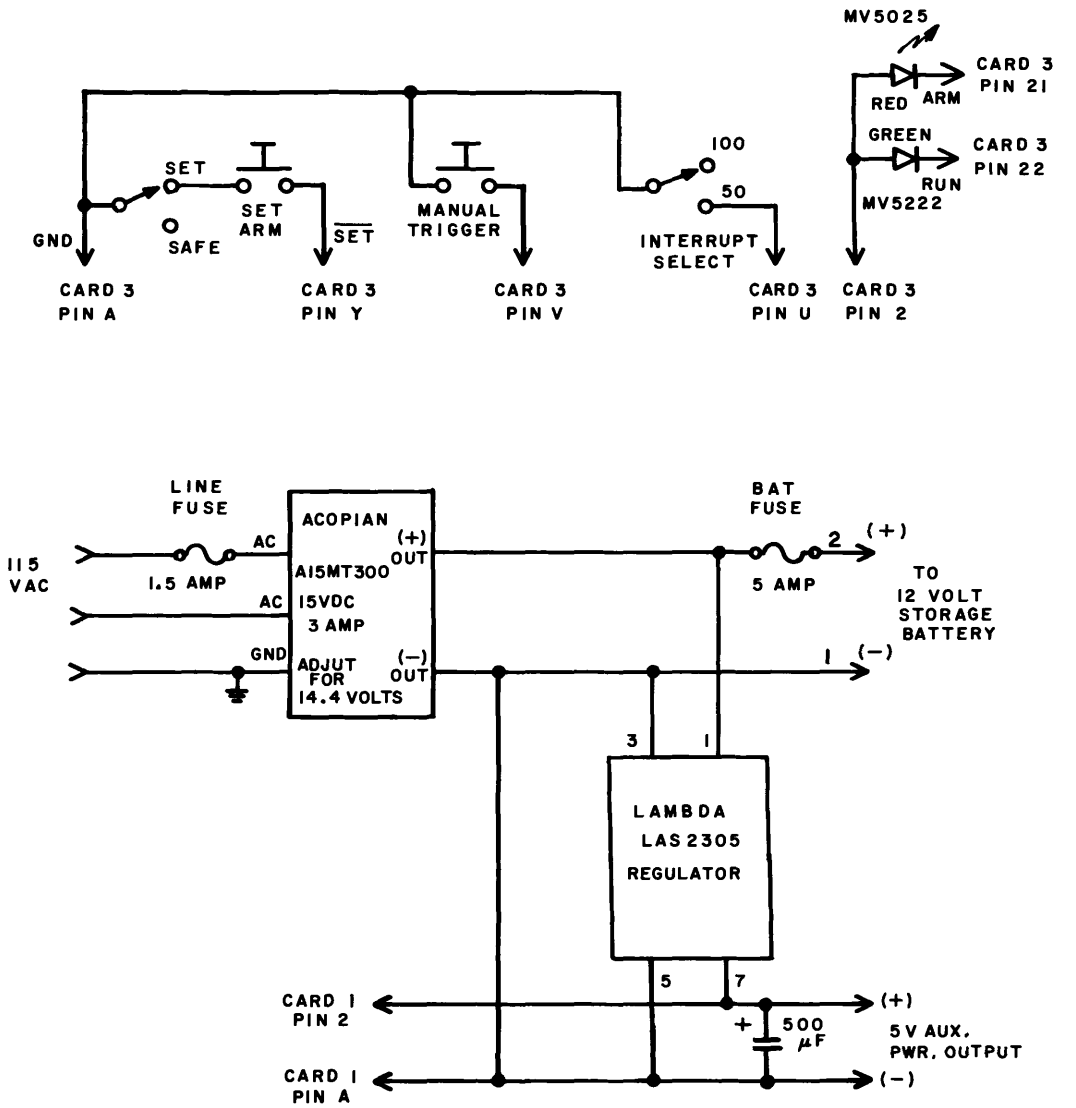
The PIL (interrupt logic) comprises chips C and D on card 3 providing the switch selectable 100/50 ms timing interrupt which is controlled by the PIL 100/50 ms signal present at flip-flop D-12. Flip-flop D-5 produces a pulse with each .08 S_A signal ending with the end PIL signal which occurs 10 μs after S_A. Likewise, flip-flop D-9 produces a negative 10 μs pulse with every .05 S_A signal. The pulses from the two flip-flops are logically ORed by NAND gate C to provide the PIL to the computer.

Cards 2/4, a schematic of which is shown below, are level shifting cards providing level shifting of the 0+5, TTL signals present at the digital output Elco (TTL) to 3-C, 0-6 logic levels which are then made available to the outside world at the 3-C digital output Elco connector. Power of -18 V from the computer is supplied through the Elco.



NRAO STANDARD TIME CLOCK
COMPUTER BUFFER CARD # 2/4
FIG.

The main frame circuits schematic is shown below showing the control switch circuits and power supply circuits. A Lambda hybrid regulator drops the battery/charger voltage to +5 V DC for the logic. The Acopian 15 volt/3 amp supply is adjusted to about 13.5 V DC for charging the battery if one is used. When power interrupts the battery will discharge until power resumes. The Acopian supply current limits at about 3 amps until a battery terminal voltage of about 13.5 volts results at which time the current tapers off to nearly zero current replacing only whatever current leaks due to self discharge. When adjusting the Acopian supply, the voltage must be measured at the battery connector.



MAIN FRAME CIRCUITS

Conclusion

The Acopian power supply has a current limit problem — when power fails and is resumed after batteries have discharged to nearly zero volts, a start up problem results, since the "fold back" current limiter does not supply enough current to bring power back up. A fix was installed comprising a 1N 1186 diode and 10 Ω/20 W resistor in series with the battery to limit the current to the battery during charging. In future designs a better AC power supply with less current limiting "fold back" may be employed.

The PIL of 50 or 100 ms does not provide a fast enough interrupt to the computer to read the .01 sec decade provided to the computer. Thus, a faster interrupt of about 10 ms should be considered.

Credits

Chassis Assembly and Wiring	Dick Skaggs
Circuit Card Assembly	Randall Shears Gary Beverage John Hubbard
Chassis Fabrication	Boyd Wright

BUSSED CARD INTERCONNECTIONS

A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y	Z

CARD 1 SLOT 1

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
		.01 s	.02 s	.04 s	.08 s	.1 s	.2 s	.4 s	.8 s	1 s	2 s	4 s	8 s	10 s	20 s	40 s					

A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y	Z

CARD 2/4 SLOT 2

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y	Z

CARD 3 SLOT 3

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
		1 m	2 m	4 m	8 m	10 m	20 m	40 m	1 h	2 h	4 h	8 h	10 h		PIL						

A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y	Z

CARD 2/4 SLOT 4

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

WIRE LIST (HARNESS)

Function	Origin		To	
$\overline{\text{Hold}}$ ----------	Card 3 - Pin	20	Card 1 - Pin	20
Reference Oscillator -----	BNC		1	V
Trigger Pulse, +10 V -----	BNC		1	W
Trigger Pulse, -10 V -----	BNC		1	21
Buffered Trigger ---------	Card 1 - Pin	19	3	18
Ten Carry ----------	3	15	1	J
20 ha ----------	1	L	3	17
$\overline{\text{Set}}$ ----------	1	Y	3	Y
Reset ----------	3	B	1	H
Seconds Carry ----------	1	22	3	Z
.08 S_A ----------	1	F	3	S
.05 S_A ----------	1	E	3	T
ENDPIL ----------	1	D	3	19
V_{CC} +5 ----------	1	2	2	1
			3	2
			4	1
Ground ----------	1	A, 1	2	A
			3	A, 1
			4	A
Date Advance ----------	3	W	BNC	
20 h ----------	1	C	Card 4 - Pin	S
Ground Lug ----------	1	A, 1	Lug	

WIRE LIST (THUMBWHEEL HARNESS)

Function	Origin	To
Unit Seconds	1	Card 1 Pin M
	2	1 N
	4	1 P
	8	1 R
Tens Seconds	1	1 S
	2	1 T
	4	1 U
Unit Minutes	1	Card 3 Pin C
	2	3 D
	4	3 E
	8	3 F
Tens Minutes	1	Card 3 Pin H
	2	3 J
	4	3 K
Unit Hours	1	Card 3 Pin L
	2	3 M
	4	3 N
	8	3 P
Tens Hours	1	Card 3 Pin R
	2	1 K
All Decades Bussed Together	X's	Card 1 Pin X
	Y's	1 Z

Ten Position, binary coded decimal, with separate common to not-true bits

Dial	Comms. X(●) & Y(○) Conn. to Terminals			
	1	2	4	8
0	○	○	○	○
1	●	○	○	○
2	○	●	○	○
3	●	●	○	○
4	○	○	●	○
5	●	○	●	○
6	○	●	●	○
7	●	●	●	○
8	○	○	○	●
9	●	○	○	●

Positive Logic
X = +5 thru
R = 510 Ω

Y = ⏚

WIRE LIST (TIME DISPLAY HARNESS - 3 AUGAT PLUGS)
AB, CD, EFH
(TWO WIRES ON ORIGIN PINS)

Function	To			Origin		
20 h	Augat AB	Pin	14 (Red)	Card 1	Pin	C
10 h			1	3		14
40 h			13	1		18
+5 volts			2	1		2
80 h			12	1		18
Colon			3	1		B
D. P.			11	1		X
Ground			4	1		1
2 h			10	Card 3	Pin	11
1 h			5	3		10
4 h			9	3		12
+5 volts			6	3		2
8 h			8	3		13
Ground			7	3		1
20 m	Augat CD	Pin	14 (Red)	3		8
10 m			1	3		7
40 m			13	3		9
+5 volts			2	3		2
80 m			12	1		18
Ground			3	1		1
2 m			11	3		4
1 m			4	3		3
4 m			10	3		5
+5 volts			5	3		2
8 m			9	3		6
+5 volts			6	3		2
2 s			8	1		12
Ground			7	1		1
4 s	Augat EFH	Pin	14 (Red)	1		13
1 s			1	1		11
8 s			13	1		10
Ground			2	1		1
D. P.			12	1		1
10 s			3	1		15
0. 2 s			11	1		8
0. 1 s			4	1		7
0. 4 s			10	1		9
40 s			5	1		17
0. 8 s			9	1		10
Ground			6	1		1
80 s			8	1		18
20 s			7	1		16

WIRE LIST (TTL OUTPUT - ELCO HARNESS (38 PIN ELCO) AND (PROTECTED PINS) (TWO WIRES ON ORIGIN PINS)

Function	Origin		To	
.01 s	Card 1	Pin 3	Elco Pin	A
.02 s	1	4		B
.04 s	1	5		C
.08 s	1	6		D
.1 s	1	7		E
.2 s	1	8		F
.4 s	1	9		H
.8 s	1	10		J
1 s	1	11		K
2 s	1	12		L
4 s	1	13		M
8 s	1	14		N
10 s	1	15		P
20 s	1	16		R
40 s	1	17		S
80 s	1	18		
1 m	3	3		T
2 m	3	4		U
4 m	3	5		V
8 m	3	6		W
10 m	3	7		X
20 m	3	8		Y
40 m	3	9		Z
80 m	1	18		
1 h	3	10		a
2 h	3	11		b
4 h	3	12		c
8 h	3	13		d
10 h	3	14		e
20 h	1	C		f
40 h	1	18		
80 h	1	18		
PIL	1	16		h
Spare	4	U		j
+5 volts	4	1		p

WIRE LIST (3-C LOGIC OUTPUT - ELCO HARNESS)
(38 PIN ELCO)
(EXPOSED PINS)

Function	Origin		To	
.01 s	Card 2	Pin 3	Elco Pin	A
.02 s		4		B
.04 s		5		C
.08 s		6		D
.1 s		7		E
.2 s		8		F
.4 s		9		H
.8 s		10		J
1 s		11		K
2 s		12		L
4 s		13		M
8 s		14		N
10 s		15		P
20 s		16		R
40 s		17		S
1 m	Card 4	Pin 3		T
2 m		4		U
4 m		5		V
8 m		6		W
10 m		7		X
20 m		8		Y
40 m		9		Z
1 h		10		a
2 h		11		b
4 h		12		c
8 h		13		d
10 h		14		e
20 h		15		f
PIL		16		h
Spare		17		j
-18 volts	Elco	Pin p	Card 2	Pin Z
			3	X
			4	2
Ground	Elco	Pin t	Card 4	A