NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

Electronics Division Internal Report No. 123

DDP-116 COMPUTER
I/O BUS LEVEL CONVERSION

Dwayne Schiebel

SEPTEMBER 1972

NUMBER OF COPIES: 150

DDP-116 COMPUTER I/O BUS LEVEL CONVERSION

Dwayne Schiebel

I. Introduction

As more equipment was added to the DDP-116 computer, it became apparent that the I/O bus should be converted to TTL levels and made available at an I/O connector. This would make all future additions easier in that no level conversions would have to be made. With this conversion the DDP-116 looks almost like an H316 except for some differences. The following report will describe each bus as it will be seen by the TTL world.

The system was built using Cambion wire wrap cards and installed in an adapted S-Pac chassis in the memory expansion rack. A total of 12 I/O connectors were installed. Six connectors are labeled input 1 thru 6 and six connectors are labeled output 1 thru 6. The 6 input connectors have available the input bus, DRL line, address bus, master clear, system normalize, reset ready line, and OCP command. The 6 output connectors have available the output bus, DRL line, address bus, master clear, system normalize, OTP pulse and OCP command. All optional signals such as PIL, ACK, DIL, DAL and ERL are available but will have to be connected to the I/O connector as needed.

Refer to the DDP-116 Interface Manual for all system timing.

Tables 1 thru 4 list the I/O connector pin assignments. Figures 1-5 are drawings of the level conversion system.

II. I/O Bus Description

1. Input Bus (INBXX-)

This bus must be driven by open collector gates. When the line is at ground the computer will see a logical one.

2. Address Bus (ADBXX-)

This bus is driven by 8H90's which have a fan out of 15. This means that no more than 15 new devices could be connected to the level conversion system. It should be cautioned here that some devices have already been connected to the conversion system on the back plane and it may not be possible to use all 12 I/O connectors. This bus will go to ground when a "one" is in the address.

3. Device Ready Line (DRLXX-)

This line must be driven by an open collector gate. A device must ground this line if it is addressed and ready to be serviced by the computer.

4. Master Clear (MSTCL-)

This line is driven by 8H90's. When "master clear" is pressed on the computer this line will go to ground.

5. System Normalize (NCO-)

This line is driven by 8H90's. This line will be at ground for about 100 milliseconds after power is turned on.

6. Reset Ready Line (RRL-)

This signal is driven by 8830's (transmission line driver). A driver is provided for each input connector. This line requires a twisted pair and the connector device should have an 8820 (transmission line receiver) on the device end. If the receiver is connected such that the + input is connected to RRL + then the output of the receiver will be as follows. The output of the receiver will go to zero to tell the device that the computer has taken the information on its input lines.

This signal is also provided single ended for use on the back plane. It will go to a zero when the data has been taken. This signal can be located at card 8, pin 20.

7. OCP Command (OCPXX-)

This signal is driven by 8830's. A driver is provided for each I/O connector. This signal should be connected by a twisted pair to an 8820 on the device end. If the + input of the 8820 is connected to OCP +, the output of the 8820 will go to ground when an OCP command is executed by the computer.

This signal is also provided single ended for use on the back plane. It will go to ground when an OCP command is executed. It can be located on card 8, pin 15.

8. Output Bus (OTBXX+)

This bus is driven by 8H90's and is connected to all 6 output connectors. The output bus will go positive when a one is output from the computer. It should be pointed out here that in a logical sense this is one place the DDP-116 and H316 differ. This system was built to match the H316.

9. OTP Pulse (OTPXX-)

This signal is driven by 8830's. A driver is provided for each output connector. This signal should be connected by a twisted pair to an 8820 in the device. If the + input of the 8820 is connected to OTP+, the output of the 8820 will go to ground when data is on the output bus.

This signal is also provided single ended for use on the back plane. It will go to ground when data is on the output bus. This signal can be located on card 8, pin 33.

III. Priority Interrupts

1. As the level conversion system was installed, eight additional interrupt lines were added and made available in the level converted form. These eight additional lines give the computer a total of sixteen lines. Sixteen lines are the maximum available without adding another logic block. This interrupt system differs from the H316 in that the interrupt must be stored in the connected device. The level converted signals are available on the back plane but must be connected to the desired I/O connector. The characteristics of the priority interrupt signals are listed below.

a. PIL09 - PIL16. These signals should be driven by 8830's at the device end. The + output of the 8830 should be connected to PILXX + via a twisted pair. The connected device should ground the input to the 8830 to interrupt the computer.

b. ACK09 - ACK16. These signals are driven by 8830's and should be connected via a twisted pair to an 8820 at the device end. If the + input of the 8820 is connected to ACKXX+, the 8820 output will go to ground when the interrupt has been acted upon. This signal should

be used to reset the interrupt. It should be pointed out here that this signal is not present in the H316 since the connected device does not have to store the interrupt.

IV. Direct Multiplexed Channel (DMC)

1. All unused DMC control lines have been level converted. These level converted signals are available on the back plane and must be wired to the desired I/O connector. Characteristics of these signals are listed below.

a. DIL02 - DIL08.

This signal must be driven by an 8830 in the peripheral device via twisted pair. The + output must go to DILXX+. If the input to the 8830 is a positive voltage (logical one) the computer will do a DMC transfer.

b. DAL02 - DAL08.

This signal is driven by an 8830. It should be connected to an 8820 in the connected device via a twisted pair. If DALXX+ is connected to the + input of the 8820, the output of the 8820 will go to ground to signal the device it has been recognized by the computer. The device should inhibit its DIL line when it receives its DAL.

c. End of Range Line (ERL-)

This line is used by all DMC channels. It has been level converted and is available on seven transmission line drivers. Seven channels are the maximum available number of channels on any of the three computers. This signal tells the device that its DMC computer locations are equal. If the + input of an 8820 is connected to ERL+, the output will go to ground when end of range is reached.

V. Conclusion

This system was designed to resemble a H316 computer as close as possible. The main difference is use of transmission line drivers and receivers. These were used on signals that could cause problems if it had a noise pick up problem.

The maximum number of devices that should be connected to this system is fifteen. Each device should only present one load to each line of the I/O bus. One other factor which could reduce the maximum number of connected devices would be cable capacitance. The address lines should show signs of problems due to loading first.

This system adds some delay as far as the DDP-116 is concerned. Signals coming from the computer have a maximum additional delay of about 70 nsec. Signals into the computer have a maximum additional delay of about 65 nsec.

The I/O connector is a 56 pin Elco with exposed pins. The keying for each connector is listed below.

		Big Pin	Little Pin
Output	1	1	1
	2	1	2
	3	1	3
	4	1	4
	5	1	5
	6	1	6
Input	1	2	1
	2	2	2
	3	2	3
	4	2	4
	5	2	5
	6	2	6

VI. Credits

Credit should be given to the following people for their help in construction of the system: R. Shears, R. Skaggs, J. Turner, and W. Vrable.

TABLE 1

Output 1-6

Signal Name	Pin	Q* Level	"1"	"0"
OTB 1	A	+ V	+ V	0 V
2	B			
3	C			
4	D			
5	E			
6	F			
7	H			
8	J			
9	K			
10	L			
11	M			
12	N			
13	P			
14	R			
15	S			
OTB 16	T	+ V	+ V	0 V
Unused	U	----------	Unused	----------
DRL	V	+ V	0 V	+ V
ADB 07	W	0 V	0 V	+ V
8	X			
9	Y			
10	Z			
11	a			
12	b			
13	c			
14	d			
15	e			
ADB 16	f	0 V	0 V	+ V
MSTCL	h	+ V	0 V	+ V
NCO	j	+ V	0 V	+ V
OTP +	k	+ V	0 V	+ V
OTP -	l			
OCP +	m	+ V	0 V	+ V
OCP -	n			
Ground	MM			
Ground	NN			

All other pins spare.

* Q Level = Quiescent Level

TABLE 2

Input 1-6

Signal Name	Pin	Q Level	"1"	"0"
INB 01	A	+ V	0 V	+ V
2	B			
3	C			
4	D			
5	E			
6	F			
7	H			
8	J			
9	K			
10	L			
11	M			
12	N			
13	P			
14	R			
15	S			
INB 16	T	+ V	0 V	+ V
Unused	U	----------	Unused	----------
DRL	V	+ V	0 V	+ V
ADB 7	W	+ V	0 V	+ V
8	X			
9	Y			
10	Z			
11	a			
12	b			
13	c			
14	d			
15	e			
ADB 16	f	+ V	0 V	+ V
MSTCL	h	+ V	0 V	+ V
NCO	j	+ V	0 V	+ V
RRL +	k	+ V	0 V	+ V
RRL -	l			
OCP +	m	+ V	0 V	+ V
OCP -	n			
Ground	MM			
Ground	NN			

All other pins spare.

TABLE 3

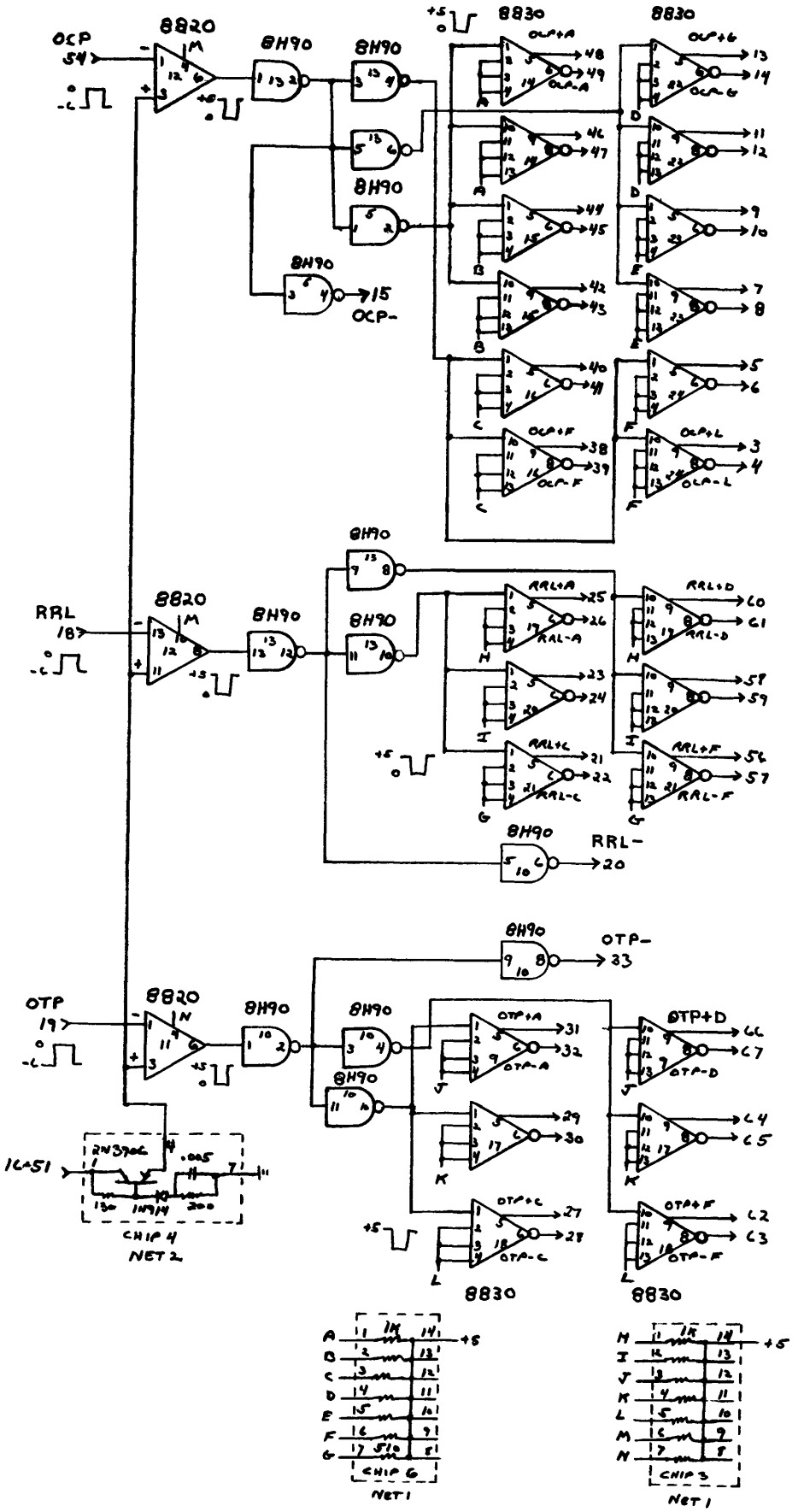
Option Signals from Computer

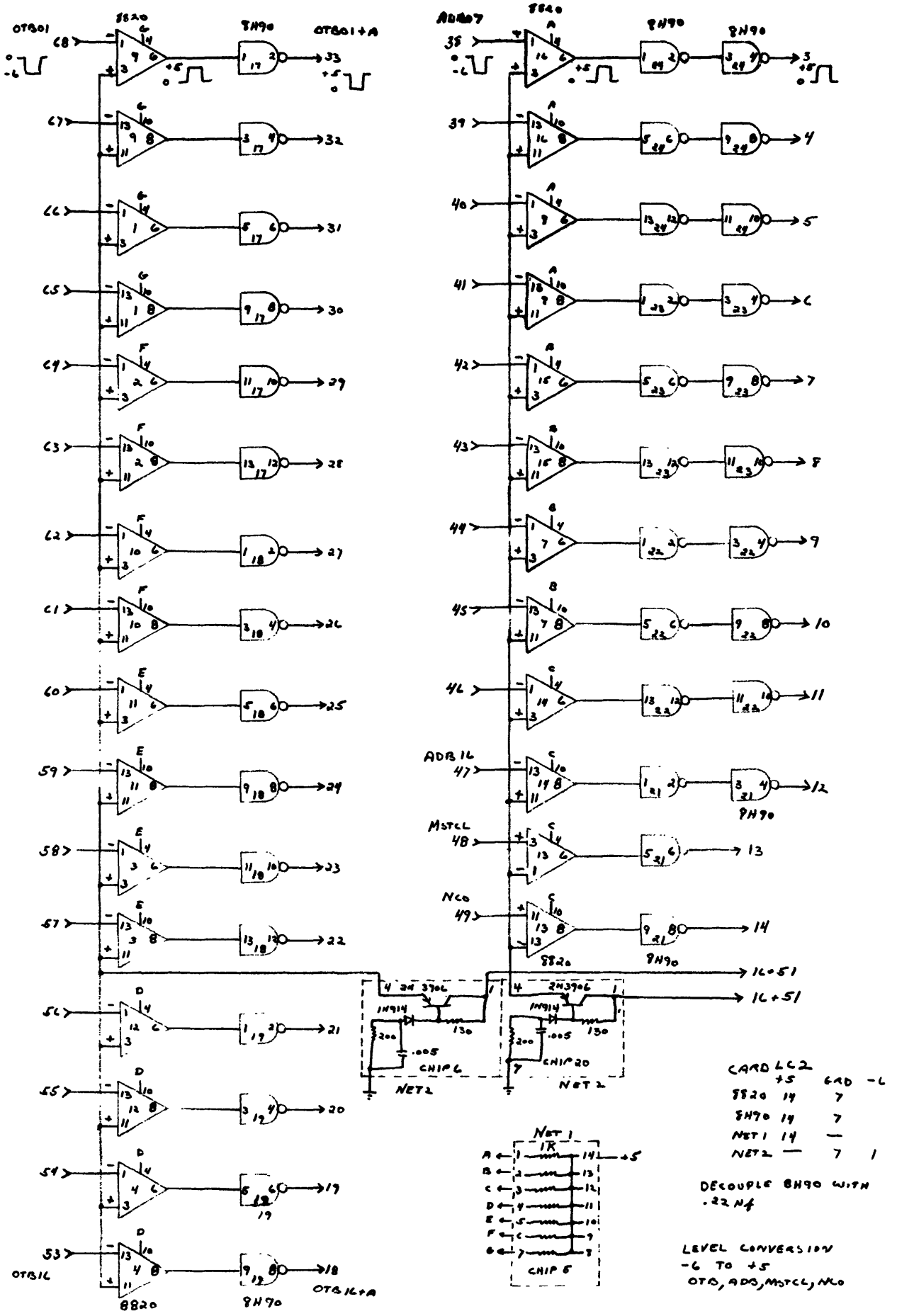
Signal Name	Location	Q Level	"1"	"0"
ACK 09 +	10-66	+ V	0 V	+ V
-	10-67			
ACK 10 +	10-31	+ V	0 V	+ V
-	10-32			
ACK 11 +	10-63	+ V	0 V	+ V
-	10-64			
ACK 12 +	10-28	+ V	0 V	+ V
-	10-29			
ACK 13 +	10-60	+ V	0 V	+ V
-	10-61			
ACK 14 +	10-25	+ V	0 V	+ V
-	10-26			
ACK 15 +	10-57	+ V	0 V	+ V
-	10-58			
ACK 16 +	10-23	+ V	0 V	+ V
-	10-24			
DAL 02 +	10-12	+ V	0 V	+ V
-	10-13			
DAL 03 +	10-44	+ V	0 V	+ V
-	10-45			
DAL 04 +	10-9	+ V	0 V	+ V
-	10-10			
DAL 05 +	10-41	+ V	0 V	+ V
-	10-42			
DAL 06 +	10-6	+ V	0 V	+ V
-	10-7			
DAL 07 +	10-38	+ V	0 V	+ V
-	10-39			
DAL 08 +	10-3	+ V	0 V	+ V
-	10-4			
ERL +	10-47	+ V	0 V	+ V
-	10-48			
ERL +	10-49	+ V	0 V	+ V
-	10-50			
ERL +	10-17	+ V	0 V	+ V
-	10-18			
ERL +	10-52	+ V	0 V	+ V
-	10-53			
ERL +	10-19	+ V	0 V	+ V
-	10-20			
ERL +	10-54	+ V	0 V	+ V
-	10-55			
ERL +	10-21	+ V	0 V	+ V
-	10-22			

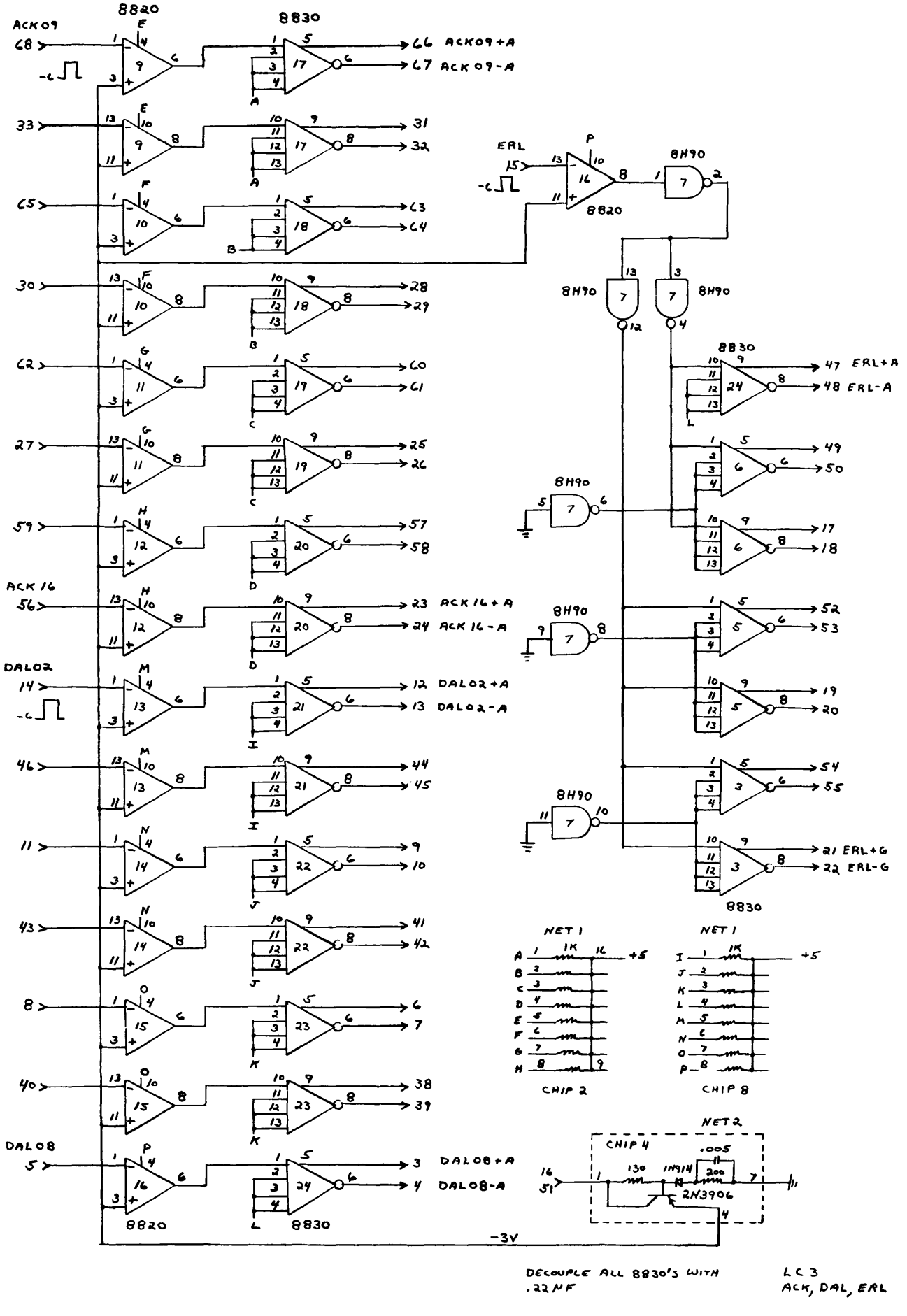
TABLE 4

Option Signals to Computer

Signal Name		Location	Q Level	"1"	"0"
PIL 09	+	13-38	+ V	0 V	+ V
	-	13-3			
PIL 10	+	13-39	+ V	0 V	+ V
	-	13-4			
PIL 11	+	13-40	+ V	0 V	+ V
	-	13-5			
PIL 12	+	13-41	+ V	0 V	+ V
	-	13-6			
PIL 13	+	13-42	+ V	0 V	+ V
	-	13-7			
PIL 14	+	13-43	+ V	0 V	+ V
	-	13-8			
PIL 15	+	13-44	+ V	0 V	+ V
	-	13-9			
PIL 16	+	13-45	+ V	0 V	+ V
	-	13-10			
DIL 01	+	13-54	0 V	+ V	0 V
	-	13-19			
DIL 03	+	13-55	0 V	+ V	0 V
	-	13-20			
DIL 04	+	13-56	0 V	+ V	0 V
	-	13-21			
DIL 05	+	13-57	0 V	+ V	0 V
	-	13-22			
DIL 06	+	13-58	0 V	+ V	0 V
	-	13-23			
DIL 07	+	13-59	0 V	+ V	0 V
	-	13-24			
DIL 08	+	13-60	0 V	+ V	0 V
	-	13-25			

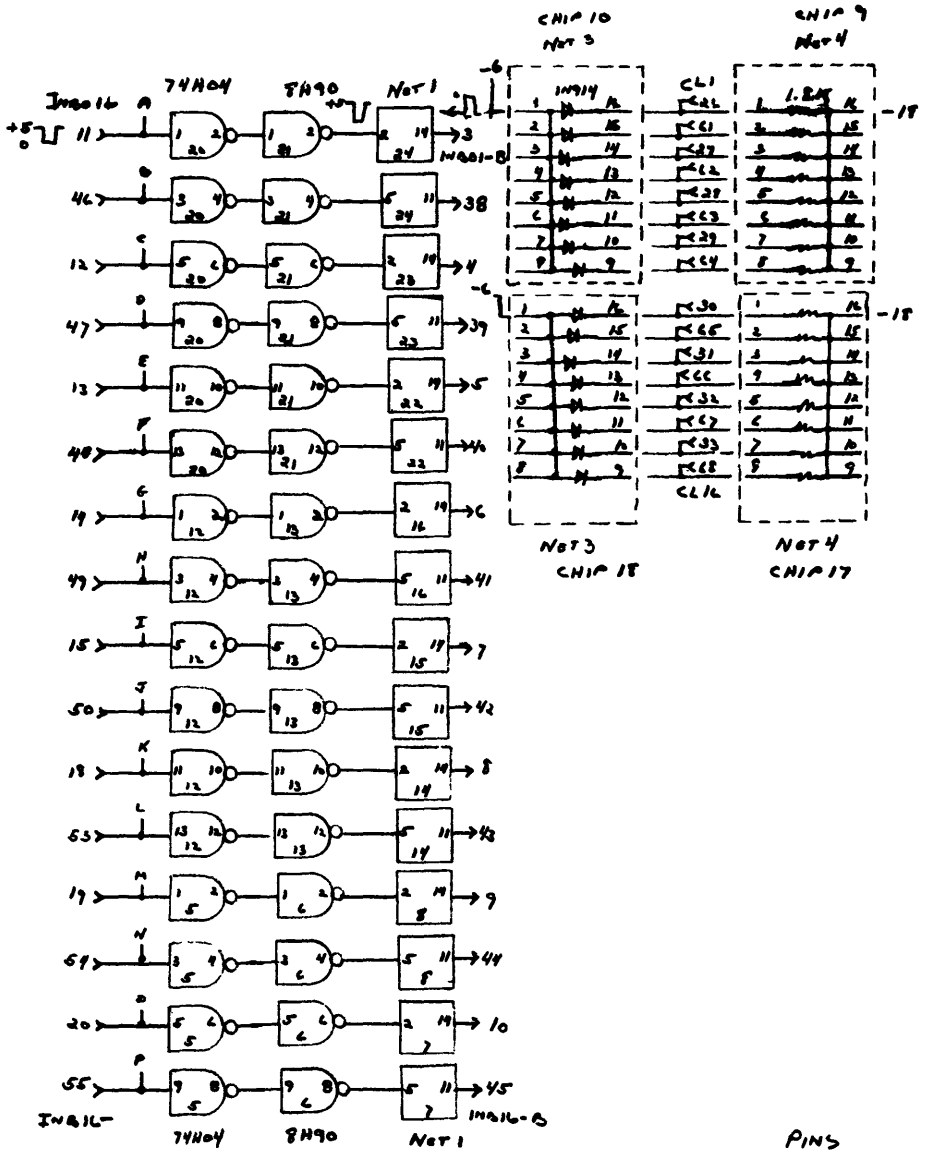

OCP
54
8820
M
8H90
8H90
8830
8830
OCP+A
OCP+6
OCP-A
OCP-G
8H90
8H90
8H90
OCP-
15
RRL
18
8820
M
8H90
8H90
RRL+A
RRL+D
RRL-A
RRL-D
RRL+C
RRL+F
RRL-C
RRL-F
8H90
RRL-
20
OTP
19
8820
N
8H90
8H90
8H90
OTP-
33
OTP+A
OTP+D
OTP-A
OTP-D
OTP+C
OTP+F
OTP-C
OTP-F
8830
8830
1C451
2N3906
.005
1K
300
CHIP 4
NET 2
CHIP 6
NET 1
CHIP 3
NET 1
+5
GND
-6
CARD LC1
.22 DECOUPLEING ON
8830
8820 14 7
8830 14 7
8H90 14 7
NET 1 14 —
NET 2 — 7 1
LEVEL CONVERSION
-6 TO +5
OCP, RRL, + OTP

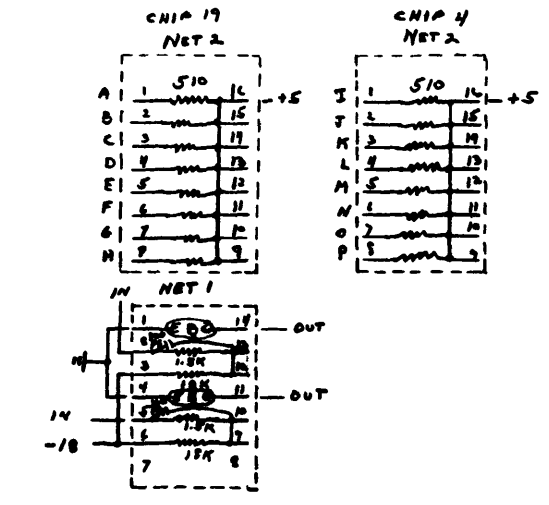

OTBO1
8820
8H90
OTBO1+A
ADB07
8H90
8H90
68
67
66
65
64
63
62
61
60
59
58
57
56
55
54
53
OTB1L
8820
8H90
OTB1L+A
35
39
40
41
42
43
44
45
46
ADB 1L
47
MSTCL
48
NCO
49
8820
8H90
1L+5
1L+5
2N3906
1N914
200
.005
130
CHIP 6
CHIP 20
NET 2
NET 2
NET 1
1K
CHIP 6
+5
CARD LC2
+5 GND -6
8820 14 7
8H90 14 7
NET 1 14 —
NET 2 — 7 1
DECOUPLE 8H90 WITH .22 Mf
LEVEL CONVERSION
-6 TO +5
OTB, ADB, MSTCL, NCO



DECOUPLE ALL 8830'S WITH .22 NF

LC 3
ACK, DAL, ERL



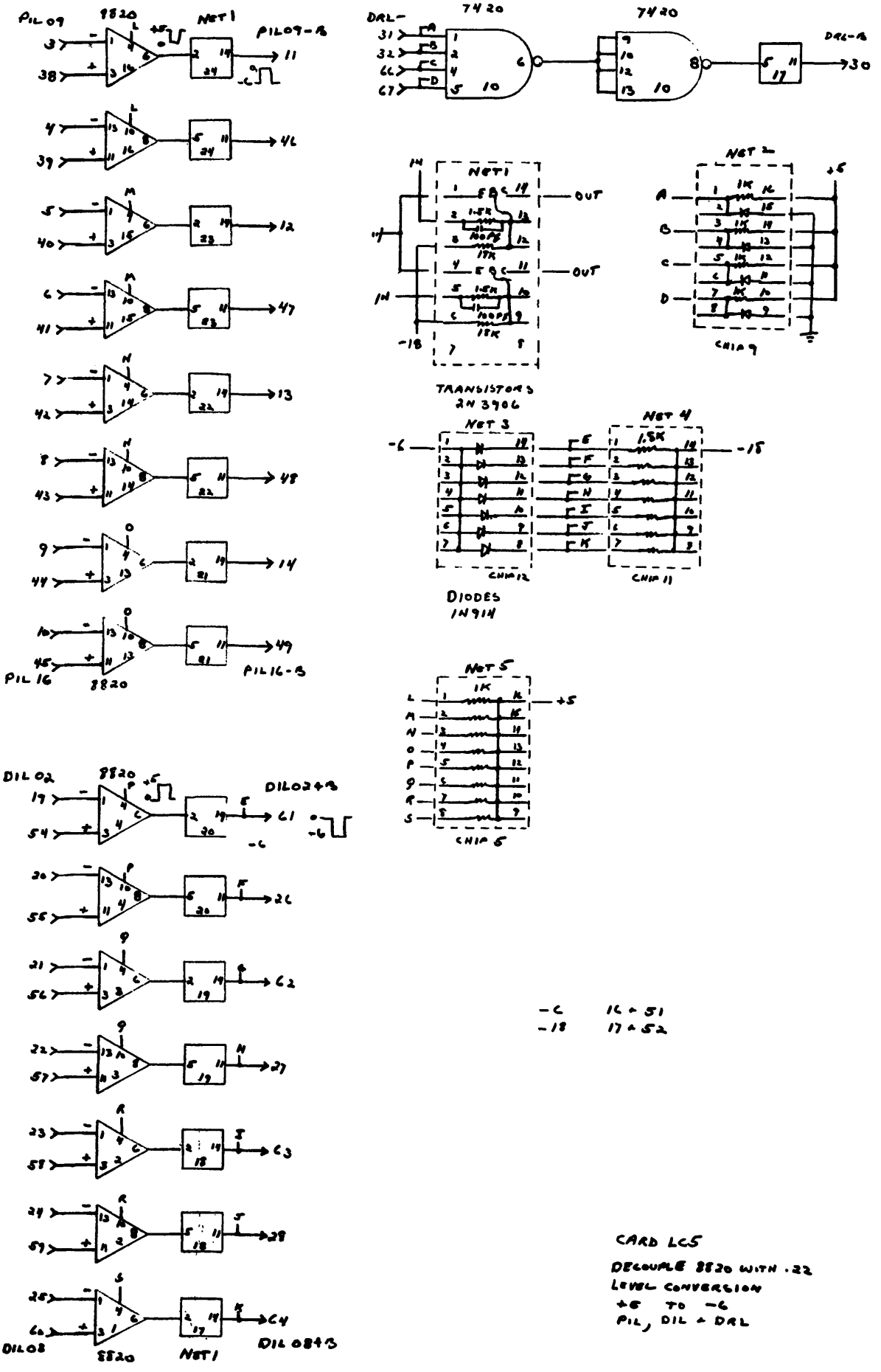


CARD LC4

DECOUPLE 74H04 & 8H90 WITH .22 Mf

	+5	GND	-18	-L
74H04	14	7	—	—
8H90	14	7	—	—
NET 1	—	1+4	6+3	
NET 2	16	—	—	—
NET 3	—	—	—	1
NET 4	—	—	16	—

LEVEL CONVERSION
+5 TO -6
INS
COLLECTOR LOADS FOR
ACK+DAL


PIL09
8820
NET1
PIL09-B
DRL-
7420
7420
DRL-B
TRANSISTORS
2N3906
NET 2
NET 3
NET 4
DIODES
1N914
NET 5
CHIP 5
CHIP 7
CHIP 11
CHIP 12
PIL16
8820
PIL16-B
DIL02
8820
DIL02+B
DIL08
8820
NET1
DIL08+B
-C 1C ~ 51
-18 17 ~ 52
CARD LC5
DECOUPLE 8820 WITH .22
LEVEL CONVERSION
+5 TO -6
PIL, DIL ~ DRL

mm Wave guide

Couplers & Filters

Equalizers.

mm RF System

mm IF System