NATIONAL RADIO ASTRONOMY OBSERVATORY
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TOTAL POWER INTEGRATOR FOR VLBI MARK II TERMINAL

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LIST OF FIGURES

INTRODUCTION

A total power integrator was developed for Mark II terminals using a voltage to frequency converter and a binary converter as integrator. The integrator takes independent samples and has a time constant of 1 second. Linearity is excellent. Temperature drift is low enough for Mark II use and if needed can be improved by selecting operational amplifiers with lower drift and resistors with better stability. The integrator does not overflow or underflow when input voltages are excessive.

SPECIFICATIONS

Input amplitude:	0 to +2V
Input impedance:	100K ohms
Saturation of input amplifier:	±2.5V
Output:	12 binary bits
	Low true TTL level
	Sink 0.4 mA
	0 volts In → 0 count Out
	+2 volts In → 4095 count Out
Integration time:	1 second
External timing signal:	1second positive pulse
Linearity:	<0.003% of measured value
Temperature drift:	0.01% per °C estimated
Supply voltage:	+15 VDC 7 mA -15 VDC 43 mA +5 VDC 210 mA
	All voltages ±0.5V
Supply voltage rejection:	+15V: 0.06% per volt
	-15V: 0.01% per volt

CIRCUIT DESCRIPTION

Total power input is first amplified and inverted by a 747 operational amplifier having a gain of -5.4. The output voltage ranging from 0 to -13.2V is converted into a current of 0 to -0.125 mA. This current is then compared to the pulsed current output pin 1 of RM4151 averaged by capacitor 50 nF. The output of the comparator is applied to a VCO (pin 7 of RM4151). The output of the VCO is counted by a 4040 12 bit binary counter. Every second the count is latched into three 4 bit 4042 latches and then the counter is reset for

the next integration. An overflow circuit of three 74C20 gates detects a count of 4095 and inhibits further counts. The counter therefore does not overflow.

CALIBRATION

1) Apply +2V at input, connect counter at TP1. Adjust full scale trim for 4095 Hz.
2) Apply +10 mV at input, adjust zero trim for 20 Hz
3) Go back to 1).

CONCLUSIONS

The linearity of the converter is excellent as shown in Figure 3. The measured variations are probably a result of the accuracy of the measurement set up of 0.002% and temperature drift of the circuit during measurement. We believe the linearity is better than shown in Figure 3. No measurement of temperature drift was attempted. It is primarily caused by temperature drift of the resistors and the 10 nF capacitor and secondarily by voltage offset drift of the 747 operational amplifier. Both can be improved by selecting more stable components.

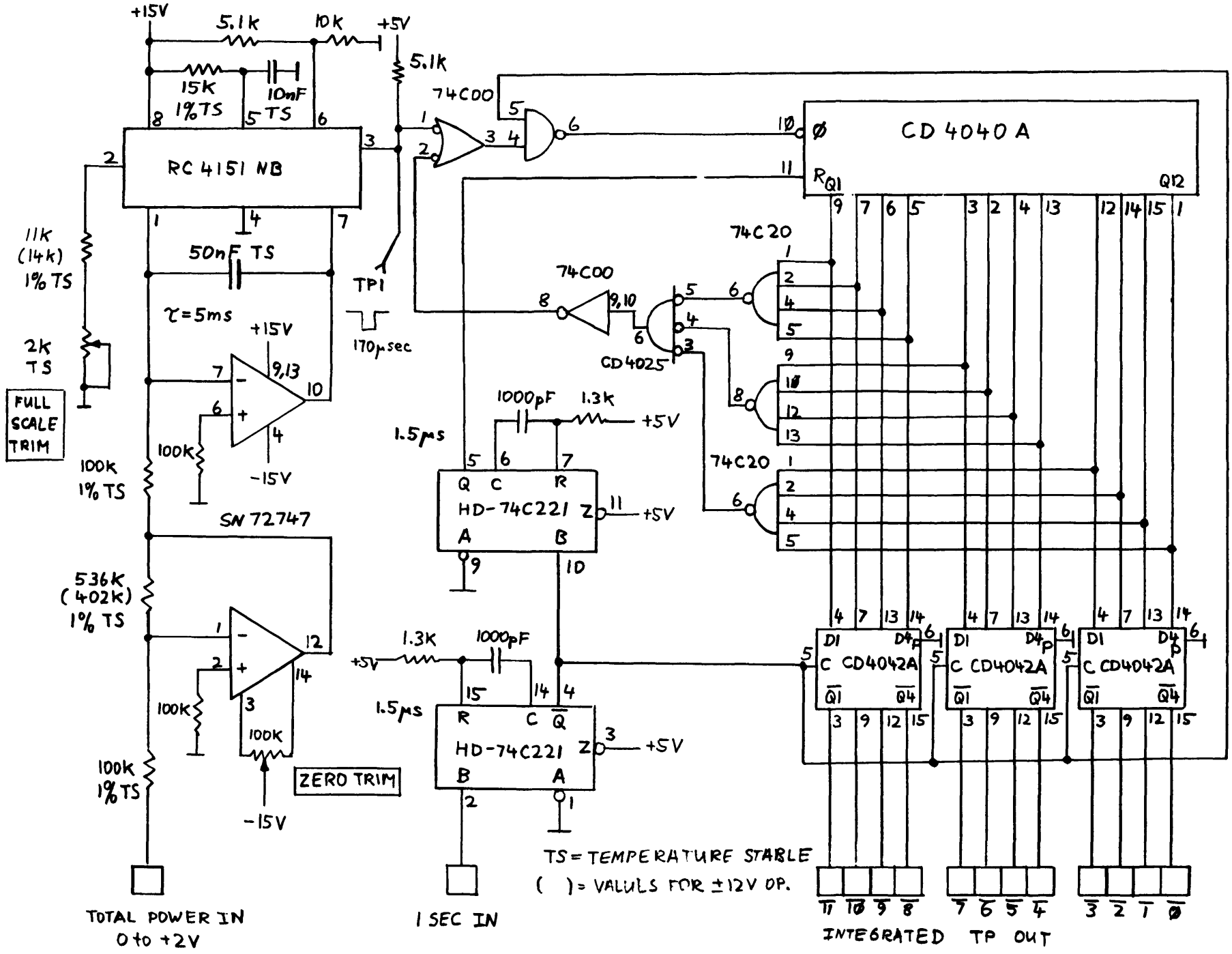


FIGURE 1: CIRCUIT TOTAL POWER INTEGRATOR

BW	τ	$(B\tau)^{-\frac{1}{2}}$	$3(B\tau)^{-\frac{1}{2}}$
		%	%
2 MHz	10 ms	0.7	2.1
2 MHz	5 ms	1	3
2 MHz	1 ms	1.8	5.4
15 kHz	10 ms	8	24
15 kHz	5 ms	11.5	34.6
15 kHz	1 ms	15	45

BW	$(B\tau)^{-\frac{1}{2}}$ τ=5 ms	$(B\tau)^{-\frac{1}{2}}$ τ=1 sec
	%	%
2 MHz	1.0	0.07
1 MHz	1.4	0.10
500 kHz	2.0	0.14
250 kHz	2.8	0.20
125 kHz	4.0	0.28
62 kHz	5.6	0.40
31 kHz	8.0	0.56
15 kHz	11.3	0.80

Figure 2. S/N as function of τ and BW

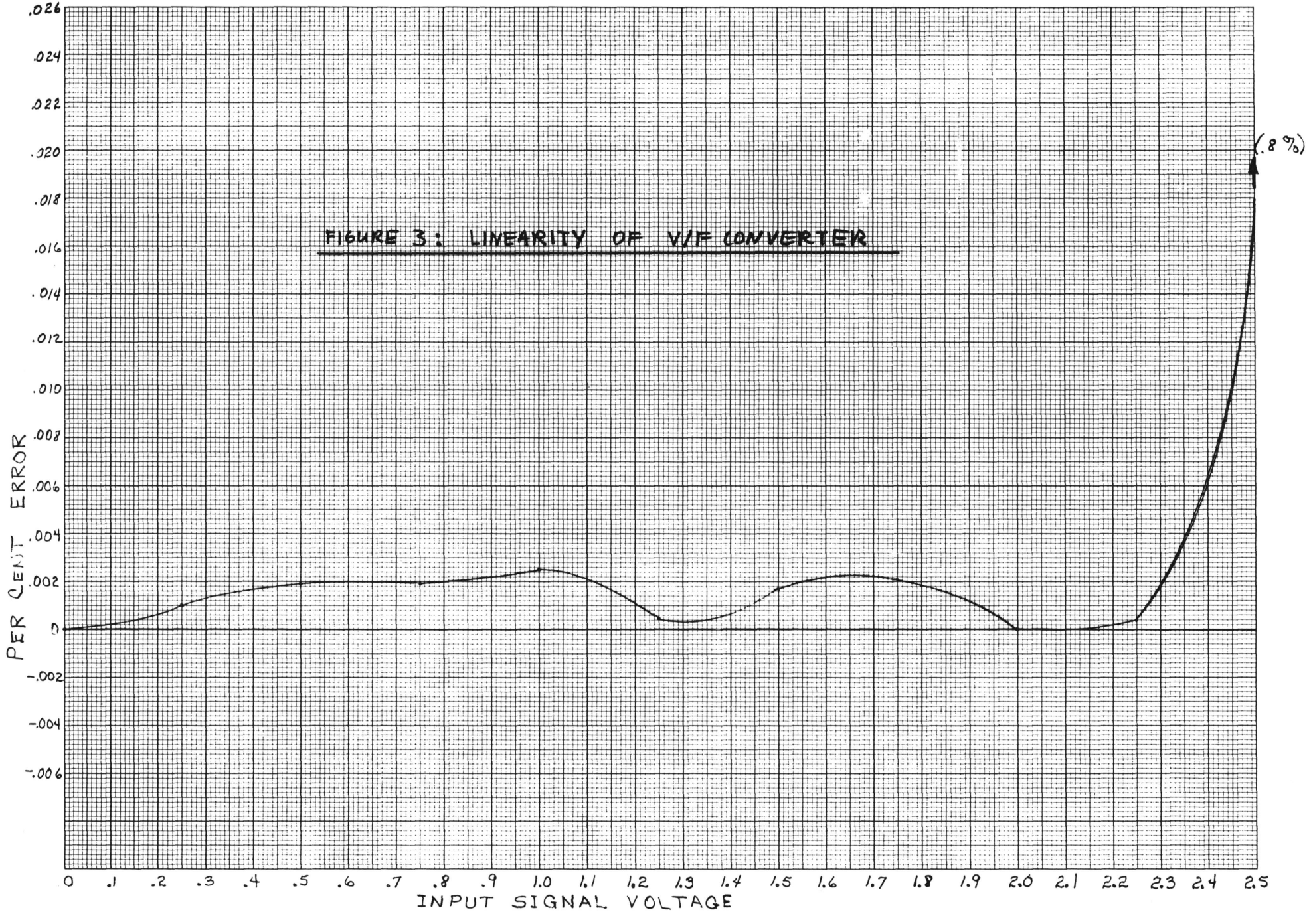


FIGURE 3: LINEARITY OF V/F CONVERTER

CD4040A Types

COS/MOS 12-Stage Ripple-Carry Binary Counter/Divider

The RCA-CD4040A consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all-0's state is accomplished by a high-level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered.

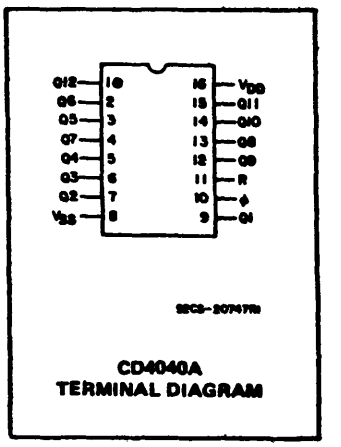
The CD4040A-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D,F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation . . . 5 MHz (typ.) input pulse rate at $V_{DD} - V_{SS} = 10$ V
- Low output impedance . . . 750 Ω (typ.) at $V_{DD} - V_{SS} = 10$ V and $V_{DS} = 0.5$ V
- Common reset
- Fully static operation
- All 12 buffered outputs available
- Low-power TTL compatible
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Control counters



CD4040A
TERMINAL DIAGRAM

RECOMMENDED OPERATING CONDITONS at $T_A = 25^oC$, Except as Noted:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges :

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Min.	D,F,K,H Packages Max.	E,Y Packages Min.	E,Y Packages Max.	UNITS
Supply Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W	5	400	–	500	–	ns
	10	110	–	125	–	
Input-Pulse Frequency, f_ϕ	5	dc	1	dc	0.9	MHz
	10	dc	3.5	dc	3.25	
Input-Pulse Rise or Fall Time, $t_{r\phi}, t_{f\phi}$	5	15	–	15	–	μs
	10	15	–	15	–	
Reset Pulse Width, t_W	5	1000	–	1250	–	ns
	10	500	–	600	–	

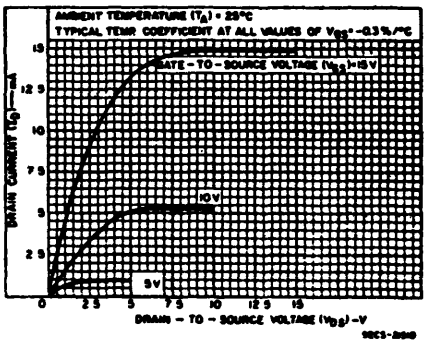


Fig.2 – Typical output n-channel drain characteristics.

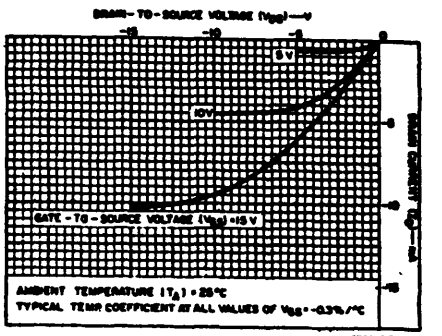


Fig.3 – Typical output p-channel drain characteristics.

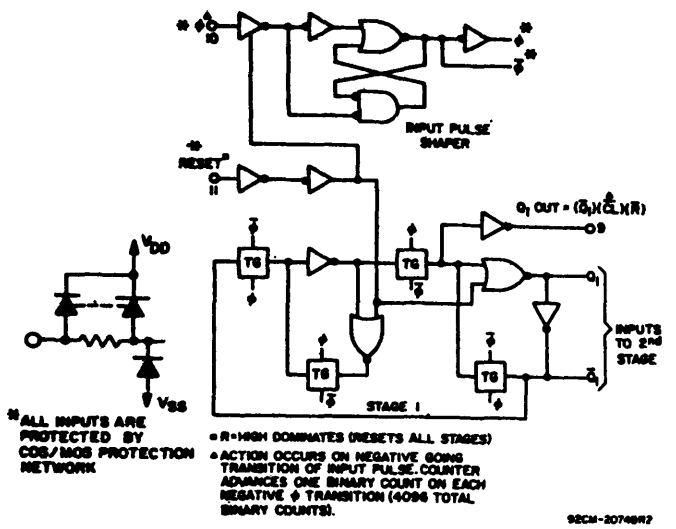


Fig.1 – Logic diagram of CD4040A input pulse shaper and 1 of 12 stages.

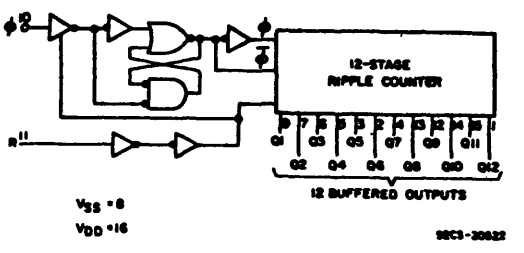


Fig.4 – Functional diagram.

CD4040A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

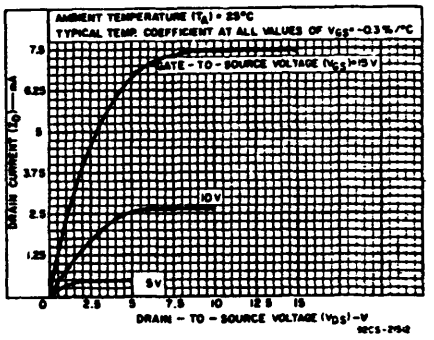


Fig.5 – Minimum output n-channel drain characteristics.

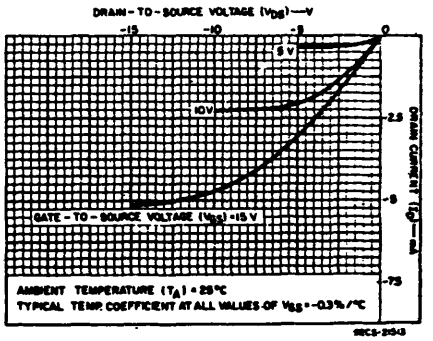


Fig.6 – Minimum output p-channel drain characteristics.

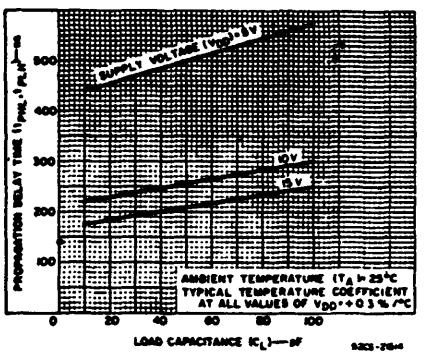


Fig.7 – Typical propagation delay time vs. load capacitance (per stage).

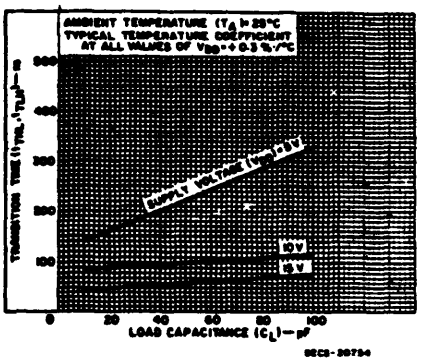


Fig.8 – Typical transition time vs. load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink).	0.5	–	5	0.22	0.36	0.145	0.102	0.21	0.36	0.08	0.056	mA
I_DN Min.	0.5	–	10	0.44	0.75	0.4	0.250	0.42	0.75	0.2	0.14	
P-Channel (Source):	4.5	–	5	−0.15	−0.25	−0.1	−0.07	−0.45	−0.25	−0.06	−0.04	
I_DP Min.	9.5	–	10	−0.03	−0.5	−0.25	−0.175	−0.29	−0.5	−0.15	−0.1	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

CD4040A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

Characteristic	Test Conditions	LIMITS						Units
		D,F,K,H Packages			E,Y Packages			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input-Pulse Operation								
Propagation Delay Time, t_{PLH}, t_{PHL}●	5	–	450	900	–	450	950	ns
	10	–	225	450	–	225	475	
Transition Time, t_{THL}, t_{TLH}	5	–	150	300	–	150	350	ns
	10	–	75	150	–	75	175	
Maximum Input-Pulse Frequency, f_ϕ	5	1	1.75	–	0.9	1.75	–	MHz
	10	3.5	5	–	3.25	5	–	
Minimum Input-Pulse Width, t_W	f=100 kHZ 5	–	200	400	–	200	500	ns
	10	–	75	110	–	75	125	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$▲	5	–	–	15	–	–	15	μs
	10	–	–	7.5	–	–	7.5	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
Reset Operation								
Propagation Delay Time, t_{PHL}*	5	–	500	1000	–	500	1250	ns
	10	–	250	500	–	250	600	
Minimum Reset Pulse Width, t_W	5	–	500	1000	–	500	1250	ns
	10	–	250	500	–	250	600	

● Measured from the 50% level of the negative clock edge to the 50% level of either the positive or negative edge of the Q1 output (pin 9); or measured from the negative edge of Q1 through Q11 outputs to the positive or negative edge of the next higher output.

▲ Maximum input rise or fall time for functional operation.

* Measured from the positive edge of the reset pulse to the negative edge of any output (Q1 to Q12).

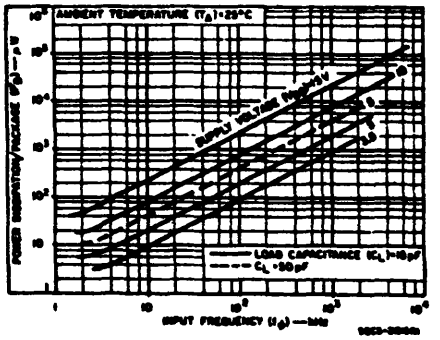


Fig. 9 – Typical dissipation characteristics.

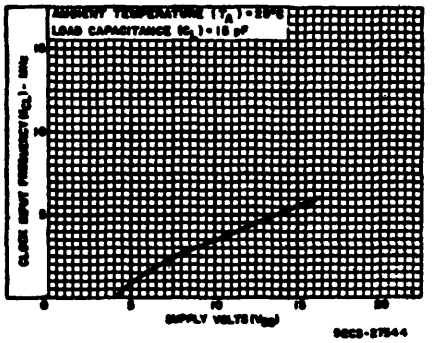


Fig. 10 – Typical input-pulse frequency vs. supply voltage.

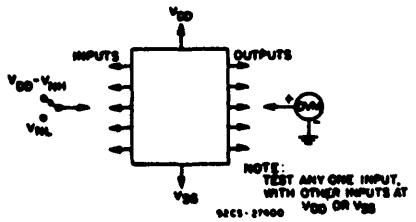


Fig. 11 – Noise-immunity test circuit.

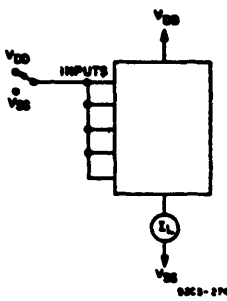


Fig. 12 – Quiescent-device-current test circuit.

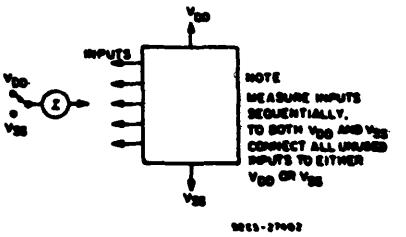


Fig. 13 – Input-leakage-current test circuit.

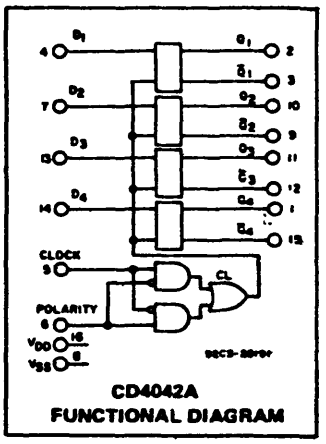
CD4042A Types

COS/MOS Quad Clocked "D" Latch

The RCA-CD4042A types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the *n*- and p-channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

The CD4042A types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4042A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
  PACKAGE TYPES E,Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
  FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

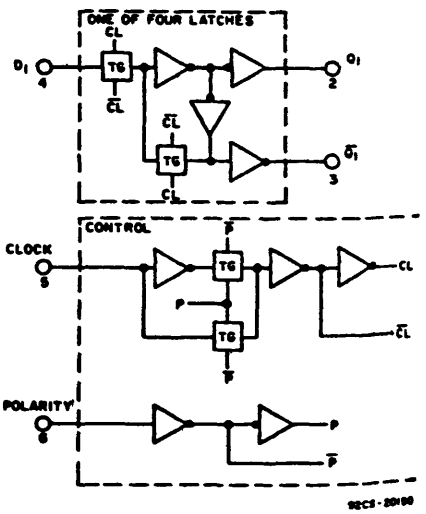
CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Data In to Q	5	150	300	150	400	ns
	10	75	150	75	200	
Data In to $\overline{Q}$	5	250	500	250	600	ns
	10	100	200	100	250	
Clock to Q	5	300	600	300	750	ns
	10	125	250	125	300	
Clock to $\overline{Q}$	5	400	800	400	1000	ns
	10	175	350	175	400	
Transition Time: t_{THL}, t_{TLH}	5	100	200	100	300	ns
	10	50	100	50	150	
Minimum Clock Pulse Width, t_W	5	175	250	175	350	ns
	10	60	120	60	175	
Minimum Hold Time, t_H	5	150	300	150	350	ns
	10	60	120	60	150	
Minimum Setup Time, t_S	5	0	50	0	50	ns
	10	0	30	0	30	
Minimum Clock Rise or Fall Time: t_r, t_f	5	Not rise or fall time sensitive.				μs
	10					
Input Capacitance, C_I (Any Input)	–	5	–	5	–	pF

Features:

- Clock polarity control
- Q and $\overline{Q}$ outputs
- Common clock
- Low power TTL compatible
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperatun range)

Applications:

- Buffer storage
- Holding register
- General digital logic



CLOCK	POLARITY	Q
0	0	D
↗	0	LATCH
1	1	D
↘	1	LATCH

Fig. 1 – Logic block diagram & truth table.

CD4042A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	12	3	12	V
Clock Pulse Width, t_W	5 10	350 175	– –	250 120	– –	ns
Setup Time, t_S	5 10	50 30	– –	50 30	– –	ns
Hold Time, t_H	5 10	350 150	– –	300 120	– –	ns
Clock Rise or Fall Time: t_r, t_f	5 10	Not rise or fall time sensitive.				μs

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				*E,Y Packages*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25		+125	−40	+25		+85	
					Typ.	Limit			Typ.	Limit		
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_{DN} Min.	0.5	–	5	0.5	1	0.4	0.27	0.24	1	0.2	0.18	mA
	0.5	–	10	1.25	2	1	0.7	0.6	2	0.5	0.45	
p-Channel (Source), I_{DP} Min.	4.5	–	5	-0.45	-1	-0.35	-0.25	-0.2	-1	-0.175	-0.15	
	9.5	–	10	-1.15	-2	-0.9	-0.6	-0.34	-2	-0.45	-0.4	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	$\pm 10^{-5}$ Typ.; 1 Max.								μA

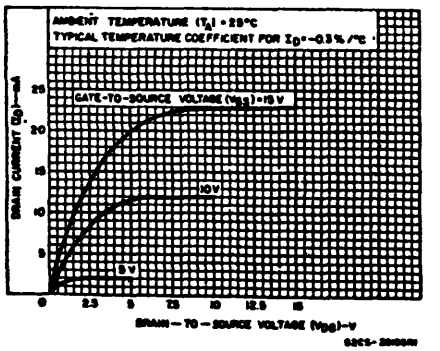


Fig. 2 – Typical output n-channel drain characteristics.

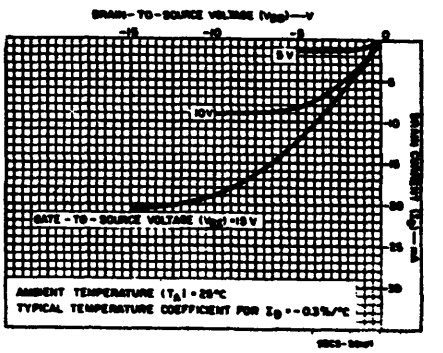


Fig. 3 – Typical output p-channel drain characteristics.

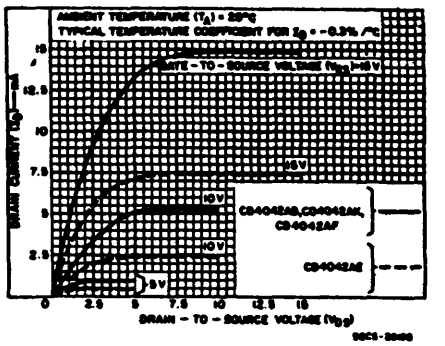


Fig. 4 – Minimum n-channel drain characteristics.

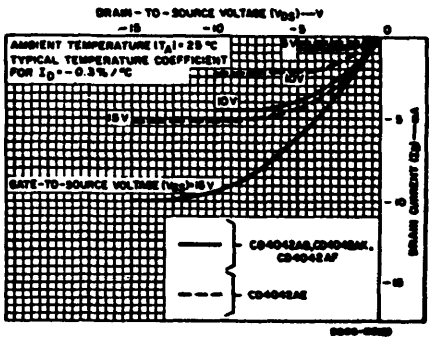


Fig. 5 – Minimum p-channel drain characteristics.

CD4042A Types

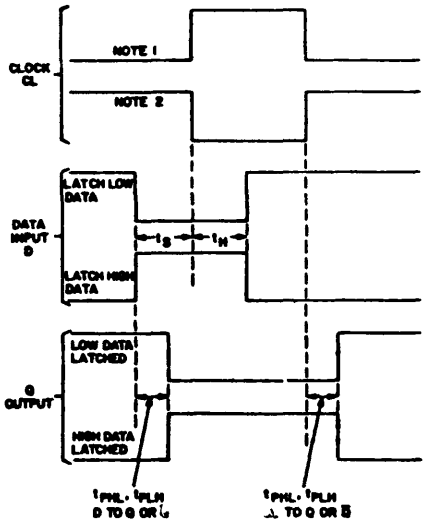


Fig. 6 – Dynamic test parameters.

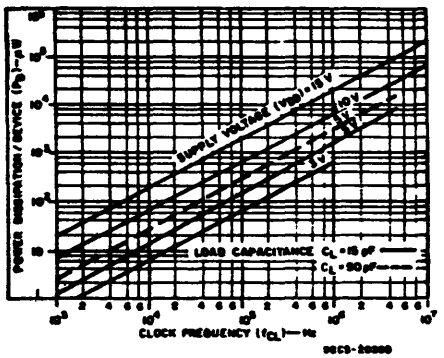


Fig. 11 – Typical dissipation characteristics.

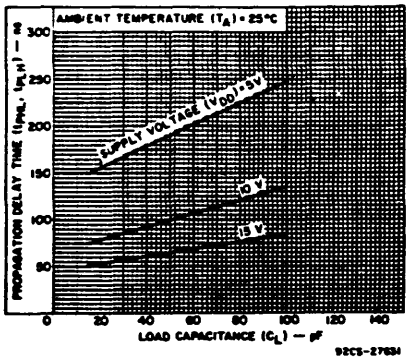


Fig. 7 – Typical propagation delay time vs. load capacitance– data to Q.

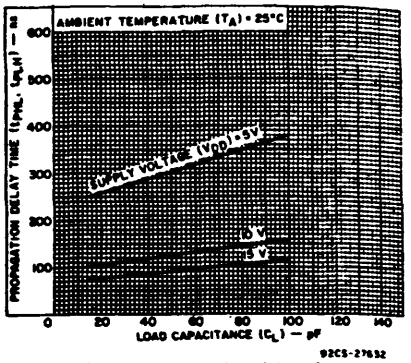


Fig. 8 – Typical propagation delay time vs. load capacitance – data to $\overline{Q}$.

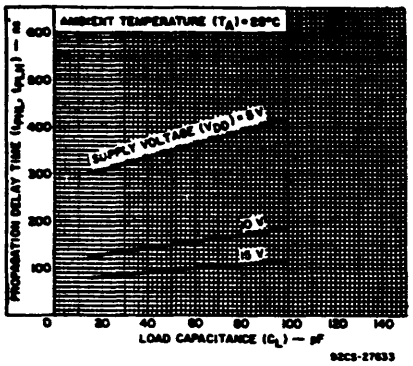


Fig. 9 – Typical propagation delay time vs. load capacitance – clock to Q.

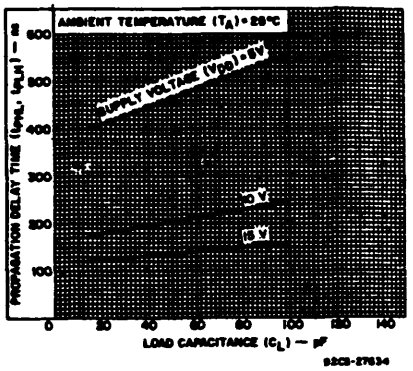


Fig. 10 – Typical propagation delay time vs. load capacitance – clock to $\overline{Q}$.

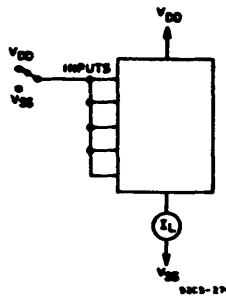


Fig. 12 – Quiescent device current test circuit.

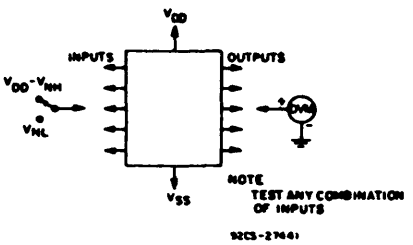


Fig. 13– Noise immunity test circuit.

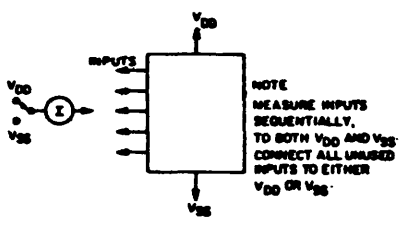


Fig. 14 – Input leakage current test circuit.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C221/HD-74C221

Dual Monostable Multivibrator

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V to 15V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP
- LOW POWER T^2L COMPATIBLE — DRIVE 2 LT^2L LOAD

Description

The HD54C221/HD74C221 dual monostable multivibrators is monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input, and a clear input.

Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components C_{EXT} and R_{EXT}. The pulse width is stable over a wide range of temperature and V_{CC}. Pulse stability will be limited by the accuracy of external timing components. The R_{EXT} ranges from 10k to 100k. Throughout these ranges the pulse width is approximately defined by the relationship $t_{W(OUT)} \approx C_{EXT} R_{EXT}$.

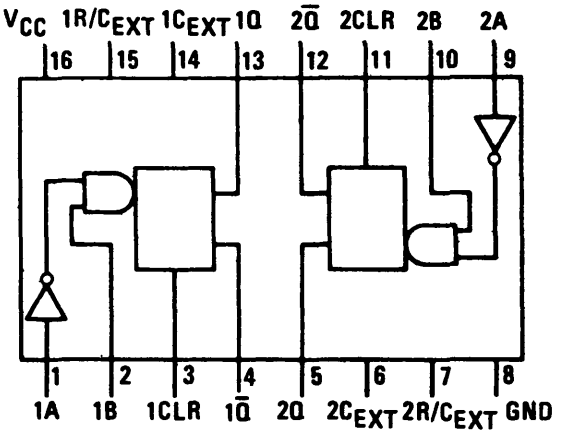
Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Connection Diagram

DUAL-IN-LINE PACKAGE



Truth Table

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H = High Level

L = Low Level

↑ = Transition from Low to High

↓ = Transition from High to Low

⎍ = One High Level Pulse

⎎ = One Low Level Pulse

X = Irrelevant

ABSOLUTE MAXIMUM RATINGS

Voltage at any Pin		-0.3V to V_{CC} +0.3V	Package Dissipation	500mW
Operating Temperature Range	HD-54C221	-55°C to +125°C	Operating V_{CC} Range	4.5V to 15V
	HD-74C221	-40°C to +85°C	Absolute Maximum V_{CC}	16V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS Min/Max limits apply across temperature range, unless otherwise noted.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	**CMOS TO CMOS**						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10 A V_{CC} = 10V, I_O = -10 A
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10 A V_{CC} = 10V, I_O = +10 A
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	A	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		A	V_{CC} = 15V, V_{IN} = 0V
				0.05	300	A	V_{CC} = 15V, $R_{Ext.}$ = ∞ Q1, Q2 = Logic 0 (Note 3)
	Supply Current	I_{CC}		15		mA	V_{CC} = 15V, Q1 = Logic 1 Q2 = Logic 0
				2			V_{CC} = 5.0V, Q1 = Logic 1 Q2 = Logic 0
	CMOS/LPTTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC}-1.5			V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8 0.8	V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4 2.4			V V	54C, V_{CC} = 4.5V, I_O = -360 A 74C, V_{CC} = 4.75V, I_O = -360 A
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4 0.4	V V	54C, V_{CC} = 4.5V, I_O = 360 A 74C, V_{CC} = 4.75V, I_O = 360 A
	OUTPUT DRIVE						
	Output Source Current (P-Channel)	I_{Source}	-1.75	3.3		mA	V_{CC} = 5.0V, V_{Out} = 0V T_A = 25°C
	Output Source Current (P-Channel)	I_{Source}	-8.0	-15		mA	V_{CC} = 10V, V_{Out} = 0V T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	1.75	3.6		mA	V_{CC} = 5.0V, V_{Out} = V_{CC} T_A = 25°C
	Output Sink Current	I_{Sink}	8.0	16		mA	V_{CC} = 10V, V_{Out} = V_{CC} T_A = 25°C

Specifications

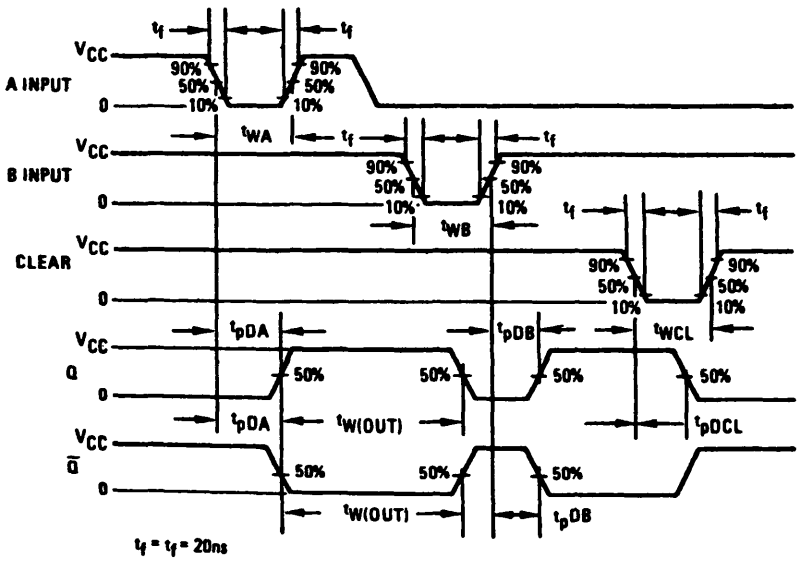
ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $C_L = 50pF$, Unless Otherwise Specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
A.C.	Propagation Delay From Trigger Input (A,B) to Output Q, $\overline{Q}$	$t_{PD\ A,B}$		250 120	500 250	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay from Clear Input (CL) to Output Q, $\overline{Q}$	$t_{DP\ CL}$		250 120	500 250	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Minimum Trigger Input (A,B) Pulse Width	$t_{w(A,B)}$	150 70	65 30		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Minimum Clear Input (CL) Pulse Width	$t_{w(CL)}$	150 70	65 30		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Q or $\overline{Q}$ Output Pulse Width	$t_{w(Out)}$	250 250 250 9.3 9 8.5 900 900 900		12.3 11 10.5 1200 1100 1100	ns ns ns s s s s s s	V_{CC} = 5.0V, R = 10K V_{CC} = 10V, C = 0pF V_{CC} = 15V V_{CC} = 5.0V, R = 10K V_{CC} = 10V, C = 1000pF V_{CC} = 15V V_{CC} = 5.0V, R = 10K V_{CC} = 10V, C = 0.1 F V_{CC} = 15V
	Output Duty Cycle				90 95	% %	R = 10K, C = 1000pF R = 10K, C = 0.1 F
	Input Capacitance	C_{IN}		25 5		pF pF	R/C_{Ext} Input Any Other Input

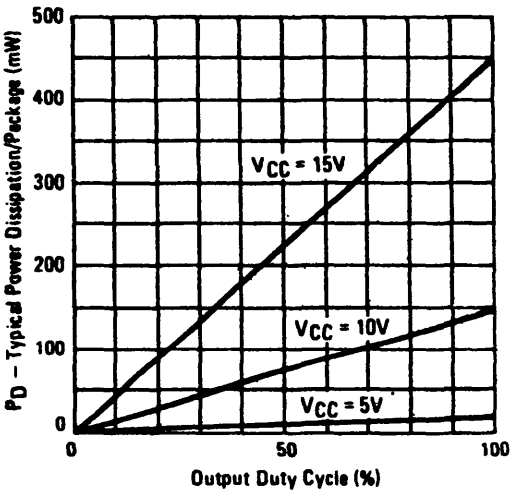
NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodic testing.
3. In standby (Q = Logic 0) the power dissipated equals the leakage current plus V_{CC}/R_{Ext}.

Switching Time Waveforms



Typical Characteristics

TYPICAL POWER DISSIPATION PER PACKAGE



NOTE: Power shown is measured with both one shots switching together and R_{EXT} = 100K.

GENERAL DESCRIPTION

The RC4151 and RM4151 provide a simple low-cost method of A/D conversion. They have all the inherent advantages of the voltage-to-frequency conversion technique. The output of RC4151/RM4151 is a series of pulses of constant duration. The frequency of the pulses is proportional to the applied input voltage. These converters are designed for use in a wide range of data conversion and remote sensing applications.

DESIGN FEATURES

- Single Supply Operation (+8V to +22V)
- Pulse Output Compatible With All Logic Forms
- Programmable Scale Factor (K)
- Linearity ±0.05% typical—precision mode
- Temperature stability ±100% ppm/°C typical
- High Noise Rejection
- Inherent Monotonicity
- Easily Transmittable Output
- Simple Full Scale Trim
- Single-Ended Input, Referenced to Ground
- Also Provides Frequency-to-Voltage Conversion

SCHEMATIC DIAGRAM

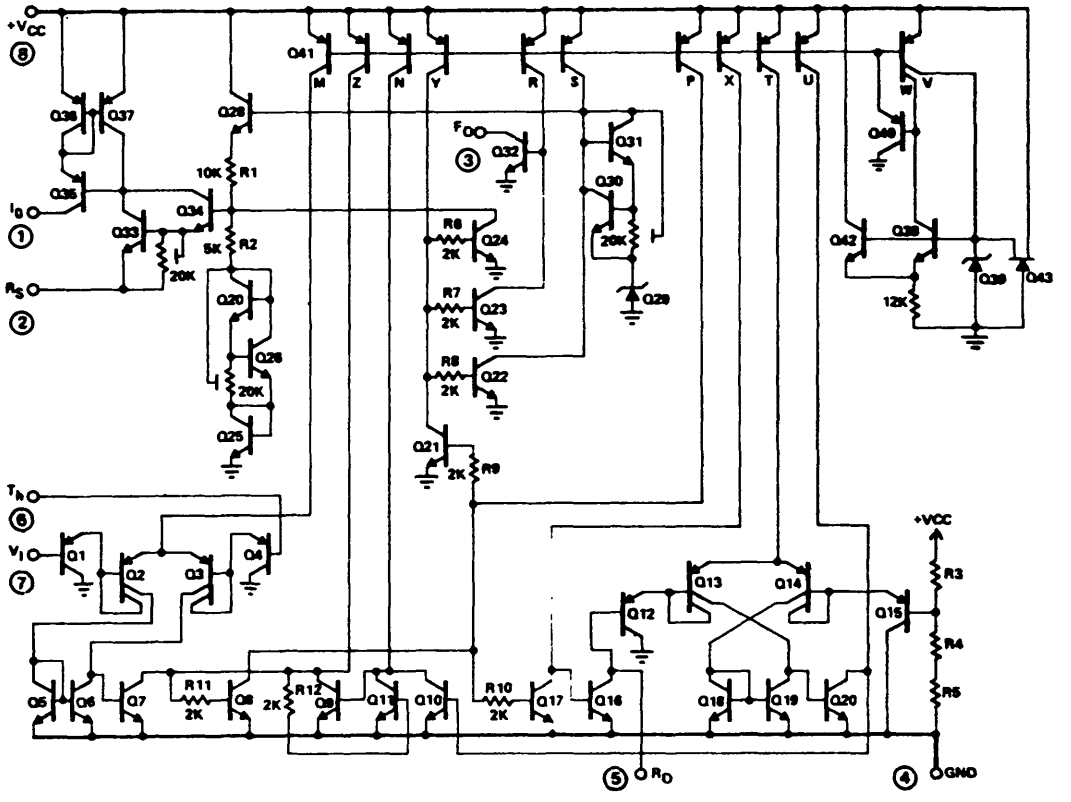
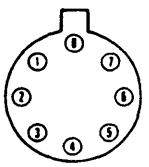


Figure 1

CONNECTION INFORMATION

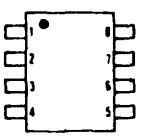
TE (TO-99) METAL CAN
(Top View)



Order Part Nos.: RC4151T, RM4151T

NOTE. PIN 4 CONNECTED TO CASE

NB MINIATURE
DUAL-IN-LINE
(Top View)



Order Part Nos RC4151NB, RV4151NB

PIN	FUNCTION
1	CURRENT SOURCE
2	SCALE FACTOR
3	LOGIC OUTPUT
4	GROUND
5	ONE-SHOT R, C
6	THRESHOLD
7	INPUT VOLTAGE
8	V_{CC}

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	+8.0 to +22V
Output Sink Current	20mA
Internal Power Dissipation	500mW
Input Voltage	-0.2V to +V_{CC}
Output Short Circuit to Ground	Continuous

Storage Temperature Range	
RM4151	-65°C to +150°C
RV4151	-55°C to +125°C
RC4151	-55°C to +125°C
Operating Temperature Range	
RM4151	-55°C to +125°C
RV4151	-40°C to +85°C
RC4151	0°C to +70°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15V, T_A = +25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	8V < V_{CC} < 15V	2.0	3.5	6.0	mA
	15V < V_{CC} < 22V	2.0	4.5	7.5	mA
Conversion Accuracy Scale Factor	Circuit Figure 3, V_I = 10V R_S = 14.0k	0.90	1.00	1.10	kHz/V
Drift with Temperature	Circuit Figure 3, V_I = 10V	–	±100	–	ppM/°C
Drift with V_{CC}	Circuit Figure 3, V_I = 1.0V 8V < V_{CC} < 18V	–	0.2	1.0	%/V
Input Comparator Offset Voltage		–	5	10	mV
Offset Current		–	±50	±100	nA
Input Bias Current		–	-100	-300	nA
Common Mode Range (Note 1)		0	0 to V_{CC}-2	V_{CC} -3.0	V
One-Shot Threshold Voltage, Pin 5		0.63	.667	0.70	x V_{CC}
Input Bias Current, Pin 5		–	-100	-500	nA
Reset V_{SAT}	Pin 5, I = 2.2mA	–	0.15	0.50	V
Current Source Output Current (R_S = 14.0kΩ)	Pin 1, Figure 2, V = 0	–	138.7	–	μA
Change with Voltage	Pin 1, V = 0V to V = 10V	–	1.0	2.5	μA
Off Leakage	Pin 1, V = 0V	–	1	50.0	nA
Reference Voltage	Pin 2, Figure 2	1.70	1.9	2.08	V
Logic Output V_{SAT}	Pin 3, I = 3.0mA	–	0.15	0.50	V
V_{SAT}	Pin 3, I = 2.0mA	–	0.10	0.30	V
Off Leakage		–	.1	1.0	μA

Note 1: Input Common Mode Range includes ground.

PRINCIPLE OF OPERATION

Single Supply Mode Voltage-to-Frequency Conversion

In this application the RC4151/RM4151 functions as a stand-alone voltage to frequency converter operating on a single positive power supply. Refer to Figure 2, the simplified block diagram. The RC/RM4151 contains a voltage comparator, a one-shot, and a precision switched current source. The voltage comparator compares a positive input voltage applied at pin 7 to the voltage at pin 6. If the input voltage is higher, the comparator will fire the one-shot. The output of the one-shot is connected to both the logic output and the precision switched current source. During the one-shot period, T, the logic output will go low and the current source will turn on with current I. At the end of the one-shot period the logic output will go high and the current source will shut off. At this time the current source has injected an amount of charge $Q = I_O T$ into the network R_B–C_B. If this charge has not increased the voltage V_B such that $V_B > V_I$, the comparator again fires the one-shot and the current source injects another lump of charge, Q, into the R_B–C_B network. This process continues until $V_B > V_I$. When this condition is achieved the current source remains off and the voltage V_B decays until V_B is again equal to V_I. This completes one cycle. The VFC will now run in a steady state mode. The current source dumps lumps of charge into the capacitor C_B at a rate fast enough to keep $V_B \geq V_I$. Since the discharge rate of capacitor C_B is proportional to V_B/R_B, the frequency at which the system runs will be proportional to the input voltage.

The 4151 VFC is easy to use and apply if you understand the operation of it through the block diagram, Figure 2. Many users, though, have expressed the desire to understand the workings of the internal circuitry. Figure 1 shows the schematic of the 4151. The circuit can be divided into five sections: the internal biasing network, input comparator, one-shot, voltage reference, and the output current source.

The internal biasing network is composed of Q39-Q43. The N-channel FET Q43 supplies the initial current for zener diode Q39. The NPN transistor Q38 senses the zener voltage to derive the current reference for the multiple collector current source Q41. This special PNP transistor provides active pull-up for all of the other sections of the 4151.

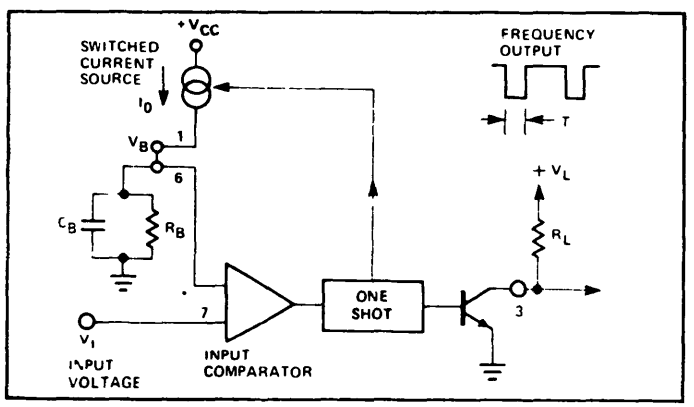


Figure 2. Simplified Block Diagram, Single Supply Mode

The input comparator section is composed of Q1-Q7. Lateral PNP transistors Q1-Q4 form the special ground-sensing input which is necessary for VFC operation at low input voltages. NPN transistors Q5 and Q6 convert the differential signal to drive the second gain stage Q7. If the voltage on input pin 7 is less than that on threshold pin 6, the comparator will be off and the collector of Q7 will be in the high state. As soon as the voltage on pin 7 exceeds the voltage on pin 6, the collector of Q7 will go low and trigger the one-shot.

The one-shot is made from a voltage comparator and an R-S latch. Transistors Q12-Q15 and Q18-Q20 form the comparator, while Q8-Q11 and Q16-Q17 make up the R-S latch. One latch output, open-collector reset transistor Q16, is connected to a comparator input and to the terminal, pin 5. Timing resistor R_O is tied externally from pin 5 to $+V_{CC}$ and timing capacitor C_O is tied from pin 5 to ground. The other comparator input is tied to a voltage divider R_3-R_5 which sets the comparator threshold voltage at 0.667 V_{CC}. One-shot operation is initiated when the collector of Q7 goes low and sets the latch. This causes Q16 to turn off, releasing the voltage at pin 5 to charge exponentially towards $+V_{CC}$ through R_O. As soon as this voltage reaches 0.667 V_{CC}, comparator output Q20 will go high causing Q10 to reset the latch. When the latch is reset, Q16 will discharge C_O to ground. The one-shot has now completed its function of creating a pulse of period $T = 1.1\ R_O\ C_O$ at the latch output, Q21. This pulse is buffered through Q23 to drive the open-collector logic circuit transistor Q32. During the one-shot period the logic output will be in the low state. The one-shot output is also used to switch the reference voltage by Q22 and Q24. The low T.C. reference voltage is derived from the combination of a 5.5V zener diode with resistor and diode level shift networks. A stable 1.89 volts is developed at pin 2, the emitter of Q33.

Connecting the external current-setting resistor $R_S = 14.0\Omega$ from pin 2 to ground gives 135μA from the collectors of Q33 and Q34. This current is reflected in the precision current mirror Q35-Q37 and produces the output current I_O at pin 1. When the R-S latch is reset, Q22 and Q24 will hold the reference voltage off, pin 2 will be at 0V, and the current will be off. During the one-shot period T, the latch will be set, the voltage of pin 2 will go to 1.89V, and the output current will be switched on.

TYPICAL APPLICATIONS

Single Supply Voltage-to-Frequency Converter

Figure 3 shows the simplest type of VFC that can be made with the 4151. Input voltage range is from 0 to +10V, and output frequency is from 0 to 10kHz. Full scale frequency can be tuned by adjusting R_S, the output current set resistor. This circuit has the advantage of being simple and low in cost, but it suffers from inaccuracy due to a number of error sources. Linearity error is typically 1%. A frequency offset will also be introduced by the input comparator offset voltage. Also, response time for this circuit is limited by the passive integration network R_B C_B. For the component values shown in Figure 3, response time for a step change input from 0 to +10V will be 135msec. For applications which require fast response time and high accuracy, use the circuits of Figure 4 and 5.

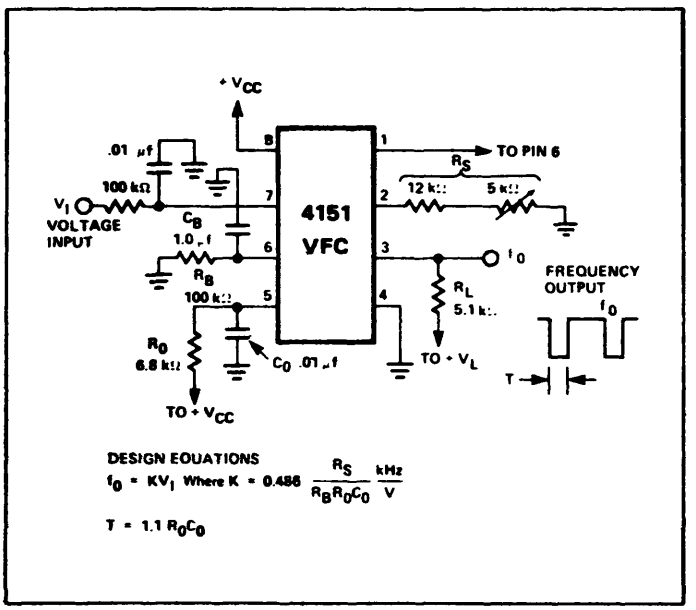


Figure 3. Single Supply Voltage-to-Frequency Converter

Precision VFC with Single Supply Voltage

For applications which requrie a VFC which will operate from a single positive supply with positive input voltage, the circuit of Figure 4 will give greatly improved linearity, frequency offset, and response time. Here, an active integrator using one section of the RC3403A quad ground-sensing op-amp has replaced the R_B-C_B network in Figure 3. Linearity error for this circuit is due only to the 4151 current source output conductance. Frequency offset is due only to the op-amp input offset and can be nulled to zero by adjusting R_B. This technique uses the op-amp bias current to develop the null voltage, so an op-amp with stable bias current, like the RC3403A, is required.

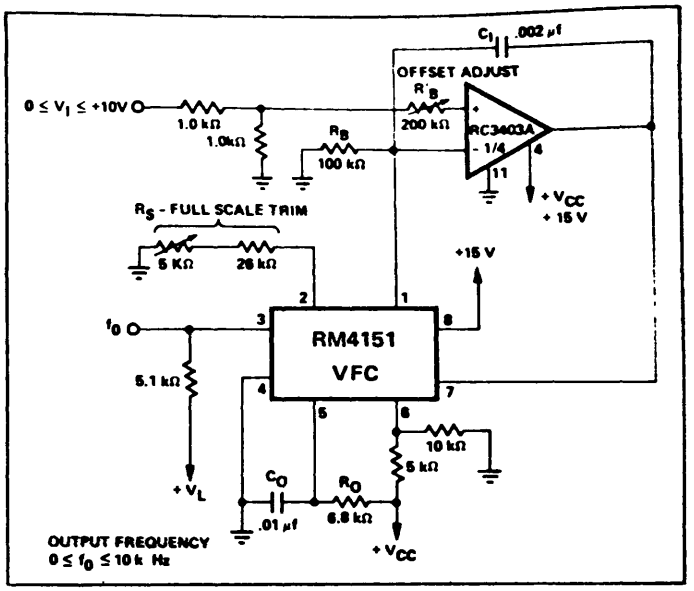


Figure 4. Precision Voltage-to-Frequency Converter Single Supply

Precision Voltage-to-Frequency Converter

In this application (Figure 5) the 4151 VFC is used with an operational amplifier integrator to provide typical linearity of 0.05% over the range of 0 to −10V. Offset is adjustable to zero. Unlike many VFC designs which lose linearity below 10mV, this circuit retains linearity over the full range of input voltage, all the way to 0V.

Trim the full scale adjust pot at V_I = −10V for an output frequency of 10kHz. The offset adjust pot should be set for 10Hz with an input voltage of −10mV.

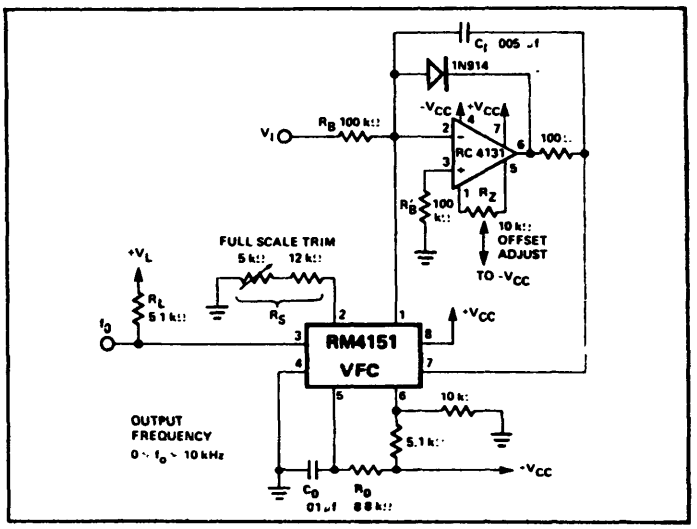


Figure 5. Precision Voltage-to-Frequency Converter

The 4131 operational amplifier integrator improves linearity of this circuit over that of Figure 3 by holding the output of the source, Pin 1, at a constant 0V. Therefore linearity error due to the current source output conductance is eliminated. The diode connected around the op-amp prevents the voltage at 4151 pin 7 from going below 0. Use a low-leakage diode here, since any leakage will degrade the accuracy. This circuit can be operated from a single positive supply if an RC3403A ground-sensing op-amp is used for the integrator. In this case, the diode can be left out. Note that even though the circuit itself will operate from a single supply, the input voltage is necessarily negative. For operation above 10kHz, bypass 4151 pin 6 with 0.01μf.

Comparison of Voltage-to-Frequency Applications Circuits

Table 1 compares the VFC applications circuits for typical linearity, frequency offset, response time for a step input from 0 to 10 volts, sign of input voltage, and whether the circuit will operate from a single positive supply or split supplies.

Table 1

	Figure 3	Figure 4	Figure 5
Linearity	1%	0.2%	0.05%
Frequency Offset	+10Hz	0	0
Response Time	135msec	10μsec	10μsec
Input Voltage	+	+	-
Single Supply	yes	yes	yes
Split Supply	–	–	yes

Frequency-to-Voltage Conversion

The 4151 can be used as a frequency-to-voltage converter. Figure 6 shows the single-supply FVC configuration. With no signal applied, the resistor bias networks tied to pins 6 and 7 hold the input comparator in the off state. A negative going pulse applied to pin 6 (or positive pulse to pin 7) will cause the comparator to fire the one-shot. For proper operation, pulse width must be less than the period of the one-shot, $T = 1.1\ R_O\ C_O$. For a 5V p-p square-wave input the differentiator network formed by the input coupling capacitor and the resistor bias network will provide pulses which correctly trigger the one-shot. An external voltage comparator such as the 311 or 339 can be used to "square-up" sinusoidal input signals before they are applied to the 4151. Also, the component values for the input signal differentiator and bias network can be altered to accommodate square waves with different amplitudes and frequencies. The passive integrator network $R_B\ C_B$ filters the current pulses from the pin 1 output. For less output ripple, increase the value of C_B.

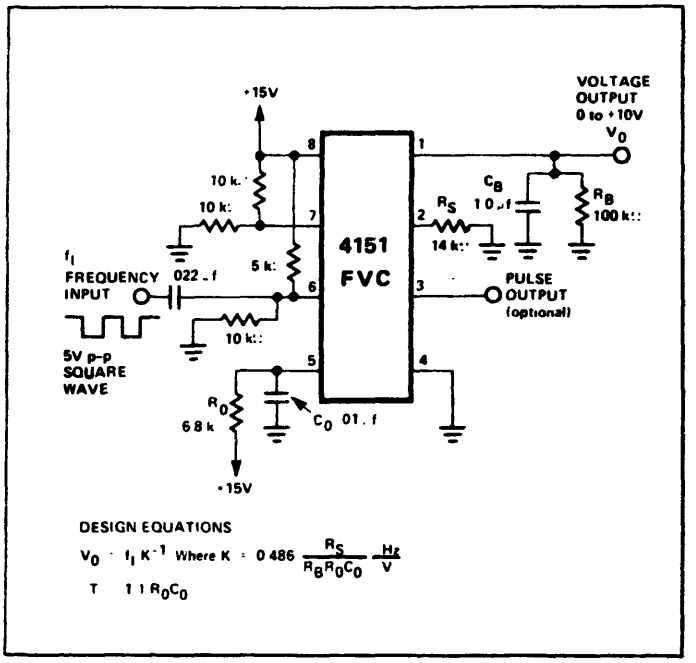


Figure 6. Single Supply Frequency-to-Voltage Converter

For increased accuracy and linearity, use an operational amplifier integrator as shown in Figure 7, the precision FVC configuration. Trim the offset to give –10mV out with 10Hz in and trim the full scale adjust for –10V out with 10kHz in. Input signal conditioning for this circuit is necessary just as for the single supply mode, and scale factor can be programmed by the choice of component values. A tradeoff exists between output ripple and response time, through the choice of integration capacitor C_I. If $C_I = 0.1\mu f$ the ripple will be about 100mV. Response time constant $\tau_R = R_B\ C_I$. For $R_B = 100k\Omega$ and $C_I = 0.1\mu f$, $\tau_R = 10msec$.

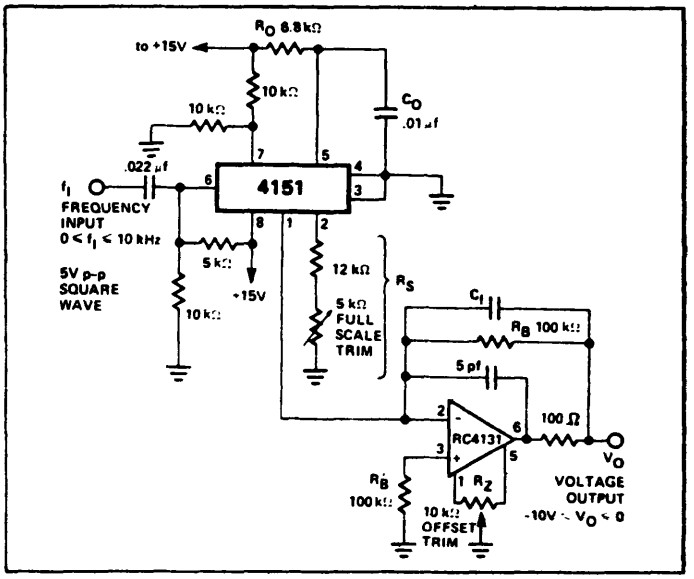


Figure 7. Precision Frequency-to-Voltage Converter

PRECAUTIONS

1. The voltage applied to comparator input pins 6 and 7 should not be allowed to go below ground by more than 0.3 volt.
2. Pins 3 and 5 are open-collector outputs. Shorts between these pins and $+V_{CC}$ can cause overheating and eventual destruction.
3. Reference voltage terminal pin 2 is connected to the emitter of an NPN transistor and is held at approximately 1.9 volts. This terminal should be protected from accidental shorts to ground or supply voltages. Permanent damage may occur if current in pin 2 exceeds 5mA.
4. Avoid stray coupling between 4151 pins 5 and 7, which could cause false triggering. For the circuit of Figure 3, bypass pin 7 to ground with at least 0.01μf. If false triggering is experienced with the precision mode circuits, bypass pin 6 to ground with at least 0.01μf. This is necessary for operation above 10kHz.

PROGRAMMING THE 4151

The 4151 can be programmed to operate with a full scale frequency anywhere from 1.0Hz to 100kHz. In the case of the VFC configuration, nearly any full scale input voltage from 1.0V and up can be tolerated if proper scaling is employed. Here is how to determine component values for any desired full scale frequency.

1. Set $R_S = 14k\Omega$ or use a 12k resistor and 5k pot as shown in the figures. (The only exception to this is Figure 5.)
2. Set $T = 1.1\ R_OC_O = 0.75\left[\frac{1}{fo}\right]$ where fo is the desired full scale frequency. For optimum performance make $6.8k\Omega < R_O < 680k\Omega$ and $0.001\mu f < C_O < 1.0\mu f$.
3. a) For the circuit of Figure 3 make $C_B = 10^{-2}\left[\frac{1}{fo}\right]$ Farads.

   Smaller values of C_B will give faster response time, but will also increase frequency offset and nonlinearity.

   b) For the active integrator circuits make

   $$C_I = 5 \times 10^{-5}\left[\frac{1}{fo}\right] \text{ Farads.}$$

   The op-amp integrator must have a slew rate of at least $135 \times 10^{-6}\left[\frac{1}{C_I}\right]$ volts per second where the value of C_I is again give in Farads.
4. a) For the circuits of Figure 3 and 4 keep the values of R_B and R_B' as shown and use an input attenuator to give the desired full scale input voltage.

   b) For the precision mode circuit of Figure 5, set $R_B = \frac{V_{IO}}{100\mu A}$ where V_{IO} is the full scale input voltage. Alternately the op-amp inverting input (summing node) can be used as a current input with full scale input current $I_{IO} = -100\mu A$.
5. For the FVCs, pick the value of C_B or C_I to give the optimum tradeoff between response time and output ripple for the particular application.

DESIGN EXAMPLE

I. Design a precision VFC (from Figure 5) with fo = 100kHz and $V_{IO} = -10V$.

1. Set $R_S = 14.0k\Omega$.
2. $T = 0.75\left[\frac{1}{10^{-5}}\right] = 7.5\mu sec$

   Let $R_O = 6.8k\Omega$ and $C_O = 0.001\mu f$.
3. $C_I = 5 \times 10^{-5}\left[\frac{1}{10^{-5}}\right] = 500pf.$

   Op-amp slew rate must be at least

   $SR = 135 \times 10^{-6}\left[\frac{1}{500pf}\right] = 0.27\mu sec$
4. $R_B = \frac{10V}{100\mu A} = 100k\Omega.$

II. Design a precision VFC with fo = 1Hz and $V_{IO} = -10V$.

1. Let $R_S = 14.0k\Omega$.
2. $T = 0.75\left[\frac{1}{1}\right] = 0.75$ sec.

   Let $R_O = 680k\Omega$ and $C_O = 1.0\mu f$.
3. $C_I = 5 \times 10^{-5}\left[\frac{1}{1}\right] F = 50\mu f.$
4. $R_B = 100k\Omega.$

III. Design a single supply FVC to operate with a supply voltage of 9V and full scale input frequency fo = 83.3Hz. The output voltage must reach at least 0.63 of its final value in 200msec. Determine the output ripple.

1. Set $R_S = 14.0k\Omega$.
2. $T = 0.75\left[\frac{1}{83.3}\right] = 9msec$

   Let $R_O = 82k\Omega$ and $C_O = 0.1\mu f$.
3. Since this FVC must operate from 8.0V, we shall make the full scale output voltage at pin 6 equal to 5.0V.
4. $R_B = \frac{5V}{100\mu A} = 50k\Omega.$
5. Output response time constant is $\tau_R \leq 200msec$

   Therefore $C_B \leq \frac{\tau_R}{R_B} = \frac{200 \times 10^{-3}}{50 \times 10^3} = 4\mu f.$

   Worst case ripple voltage is:

   $$V_R = \frac{9mS \times 135\mu A}{4\mu f} = 304mV.$$

IV. Design an opto-isolated VFC with high linearity which accepts a full scale input voltage of +10V. See Figure 8 for the final design. This circuit uses the precision mode VFC configuration for maximum linearity. The RC3403A quad op-amp provides the functions of inverter, integrator, regulator, and LED driver.

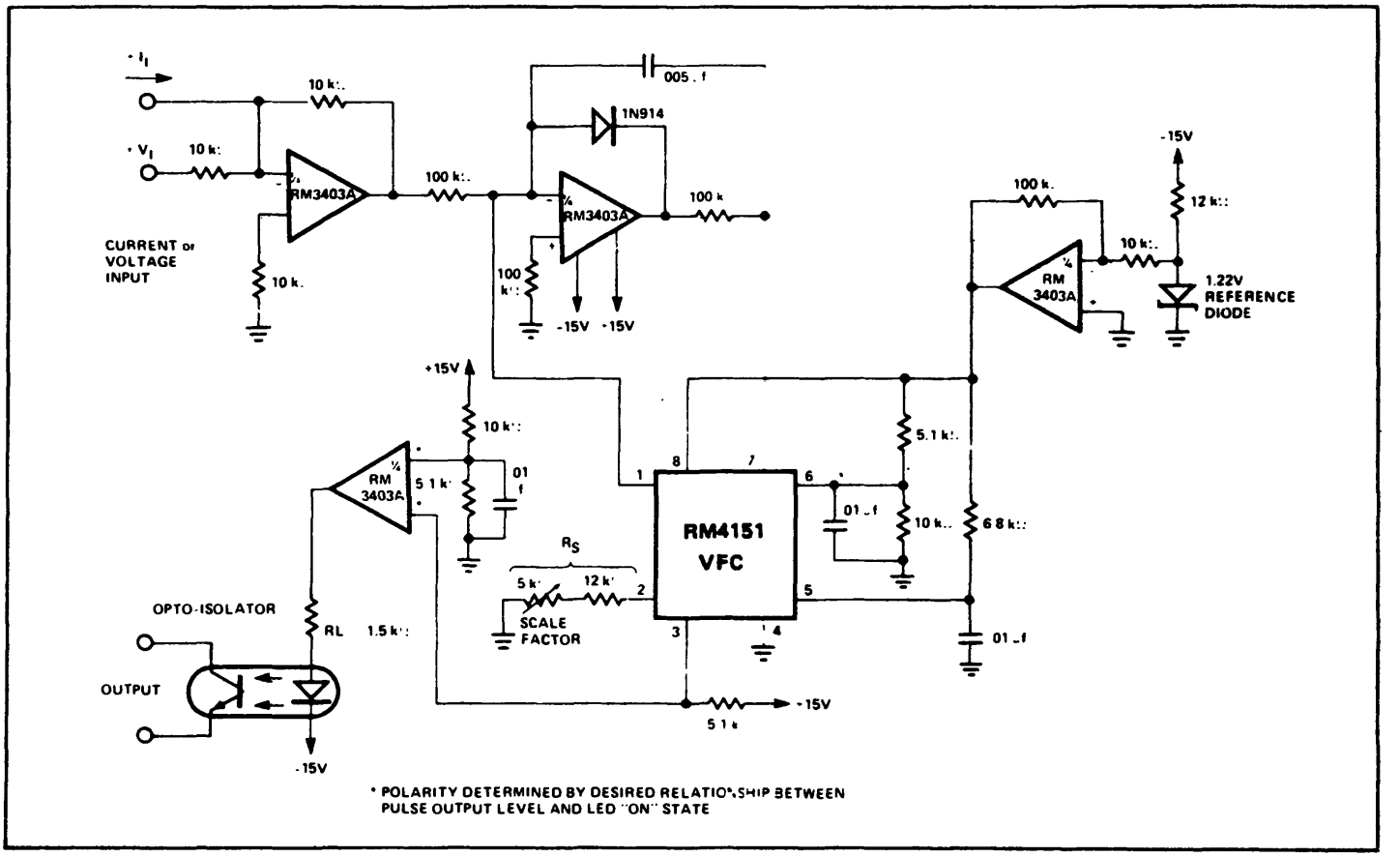


Figure 8. Opto-Isolated VFC

TYPES SN52747, SN72747 DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7311446, FEBRUARY 1971—REVISED SEPTEMBER 1973

- No frequency Compensation Required
- Low Power Consumption
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- No Latch-up
- Designed to be Interchangeable with Fairchild μA747 and μA747C

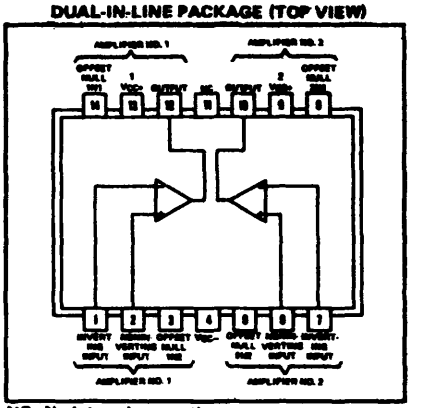
description

The SN52747 and SN72747 are dual general-purpose operational amplifiers featuring offset-voltage null capability. Each half is electrically similar to SN52741/SN72741.

The high common-mode input voltage range and the absence of latch-up make the amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 3.

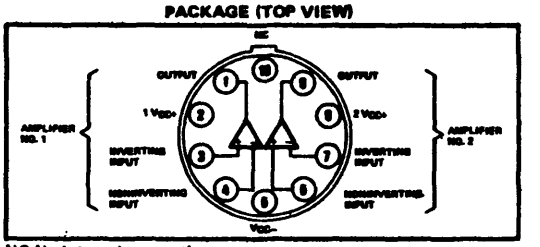
The SN52747 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72747 is characterized for operation from 0°C to 70°C.

FA FLAT PACKAGE OR J, JA, OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



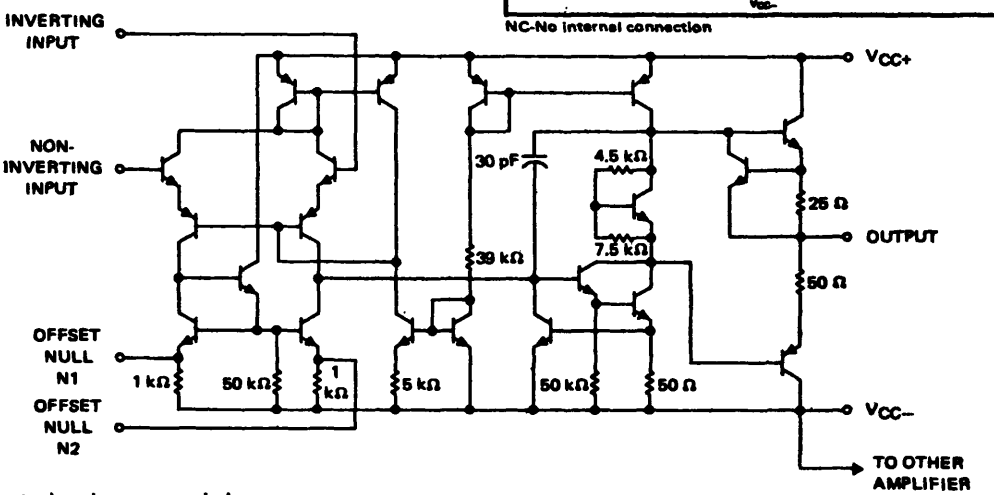
NC—No internal connection

L PLUG-IN PACKAGE (TOP VIEW)



NC-No internal connection

schematic (each amplifier)



Component values shown are nominal.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52747	SN72747	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage any input, (see Notes 1 and 3)		±15	±15	V
Voltage between any offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	Each amplifier	500	500	mW
	Total package	See Figure 2		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	FA, J, JA, or L package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52747 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature and for total package ratings, refer to Dissipation Derating Curve, Figure 2.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SN52747			SN72747			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S ≤ 10 kΩ	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		R_L ≥ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		R_L ≥ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	50,000	200,000		50,000	200,000		
			Full range	25,000			25,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	R_S ≤ 10 kΩ	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (each amplifier)	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Power dissipation (each amplifier)	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	
V_{o1}/V_{o2}	Channel separation		25°C		120			120		dB

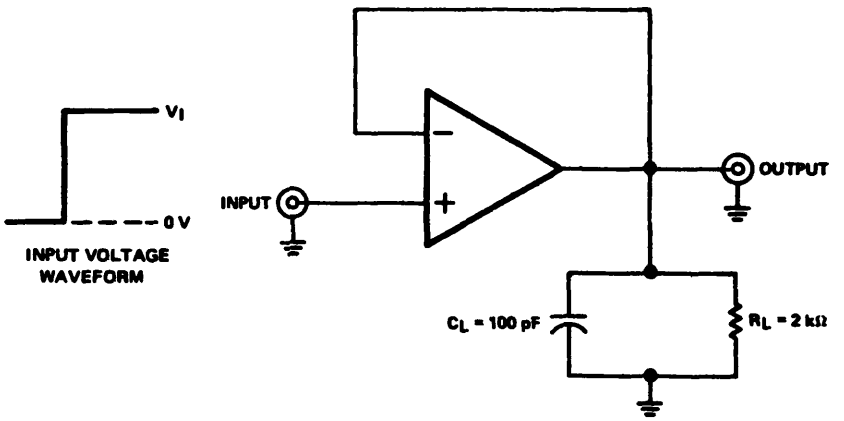
† All characteristics are specified under open-loop operation. Full range for SN52747 is −55°C to 125°C and for SN72747 is 0°C to 70°C.
NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

For definitions of terms, see the SN52741/SN72741 data sheet, page 4-69.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN52747			SN72747			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3			0.3		μs
	Overshoot			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/μs

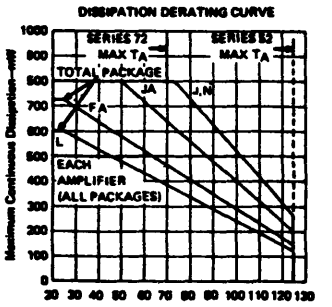
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

FIGURE 1—RISE TIME, OVERSHOOT, AND SLEW RATE

THERMAL INFORMATION



PKG	DERATE	FROM (TOT PKG)	FROM (EACH AMP)
L	4.8 mW/°C	25°C	45°C
FA	5.8 mW/°C	25°C	64°C
JA	6.8 mW/°C	50°C	87°C
J, N	10.4 mW/°C	73°C	102°C

FIGURE 2

TYPICAL APPLICATION DATA

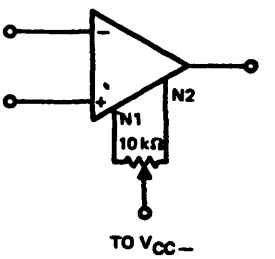


FIGURE 3—INPUT OFFSET VOLTAGE NULL CIRCUIT

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TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

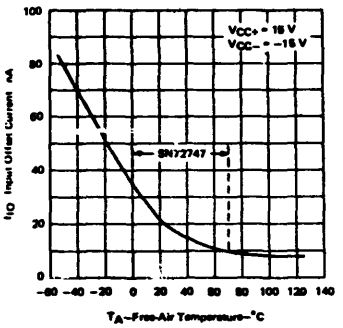

FIGURE 4

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

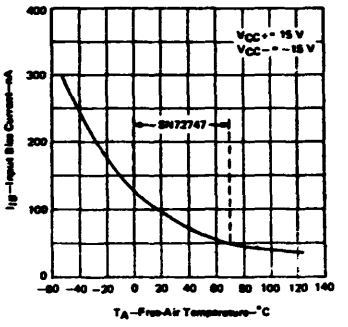

FIGURE 5

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

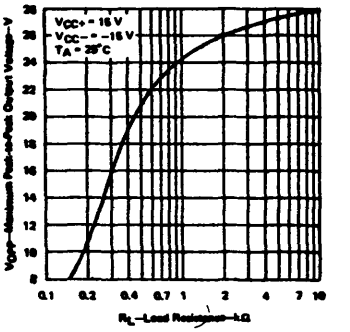

FIGURE 6

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

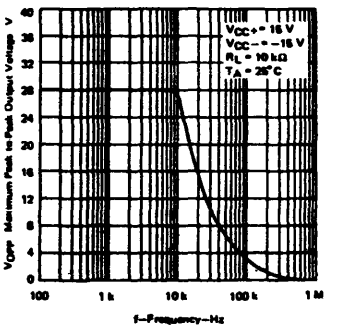

FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

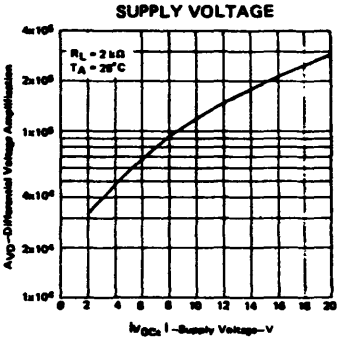

FIGURE 8

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

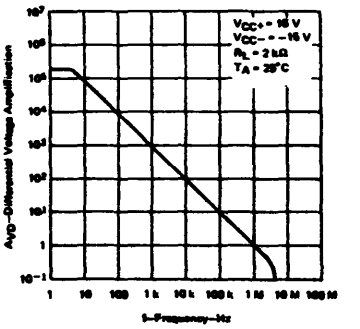

FIGURE 9

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

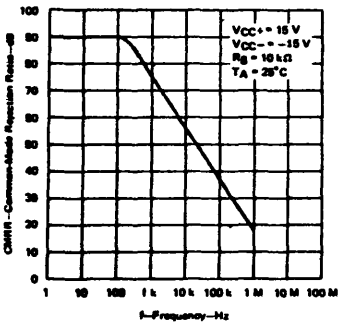

FIGURE 10

OUTPUT VOLTAGE
vs
ELAPSED TIME

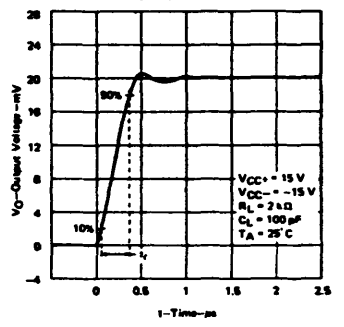

FIGURE 11

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

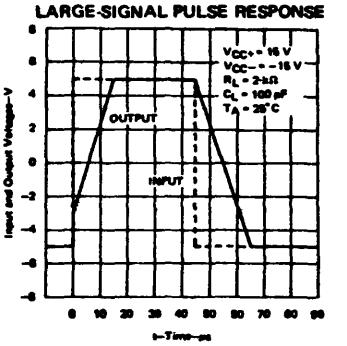

FIGURE 12

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