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NEW TAPE DRIVE FOR 300-FOOT TELESCOPE

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I. INTRODUCTION

After around 15 years of service it became apparent that it was time to retire our Control Data Corporation 556 BPI tape drive. In addition to a persistent pinch roller problem, spare parts were getting expensive to buy.

After looking at several tape drives it was decided to buy a Tandberg TDI 1050 tape transport. This drive can record at 1600 CPI phase encode or 800 CPI NRZI, with a tape speed of 25 IPS. A slow tape speed was selected to avoid timing problems with the DDP 116. The old tape drive could transfer a 16-bit word of data in 120 μ sec, and this new drive takes 50 μ sec.

In addition to the advantage of a modern tape drive, tapes recorded on this drive can be read on the Modcomp tape drives.

II. PROGRAMMING

As far as our observing programs are concerned, there is no difference between the old and new drive. There are some differences between commands available on the new drive and the commands for the old drive. These are listed below.

OCP 14/OCP 414	Read/write BCD. These commands are no longer available.
OCP 114/OCP 514	Read/write binary 2 character/word. These commands are no longer available.
OCP 314	Set DMC mode. This command is not necessary.
OCP 714	Reset DMC end of transmission interrupt. This command is not used.
SKS 14	Skip if the TCU is ready. This SKS function is not implemented.
SKS 414	Skip if the TCU is not interrupting. This SKS function is not available since the tape unit is on dedicated interrupt line 5.

INA 14/INA 1014 Input from TCU. The new tape drive is built for DMC transfers only.

OTA 14 Output to TCU. DMC transfers only.

As in the old tape drive, the new tape drive is connected to DMC Channel 1 (LOC 10 and 11) and to priority interrupt line 5 (LOC 34).

There is one new command:

OCP 414 Erase 3.7 inches of tape. This command can be used to erase tape.

III. ELECTRONICS

Modern day tape drives make life easy for the designer in that a lot of the work such as parity generation, spacing forward and reverse and writing end of files is accomplished by a formatter which can be purchased with the tape drive.

The logic built by NRAO can be divided into two parts: Buffers and address decode located in the DDP 116 and control electronics located in the tape drive rack.

The buffer and address decoder is contained on two Cambion cards located in the DDP 116 under the level conversion system. The first card, located in Slot 1, decodes the address (14) and sends a "selected" signal to the control electronics. This address can be selected by a dip switch. Address bits 7-10 are buffered and sent to the control logic. In addition to the address buss, the output buss (OTB), MSTCL, ERL, RRL, and OCP are also buffered and sent to the control logic. Data ready (DRL) is received by this card and sent to the level conversion system. The second card contains input buffers which gate the input data with a device acknowledge line (DAL) and applies this data to the input buss of the level conversion system. Also contained on this card is the circuitry necessary for two modes of DMC/PIL operation. The first mode was for test using DMC Channel 7 and priority interrupt line 7. The second

mode is for normal operation using DMC Channel 1 and priority interrupt line 5. The priority interrupt lines and DMC Channel 1 lines had to be converted to negative logic (0/-6).

The control electronics is contained in a "Shalloway" chassis located under the tape drive. All of the logic necessary to control the tape drive is contained on two large "Shalloway" wire-wrap cards. Card 1 controls the data flow to and from the tape unit. Card 2 decodes the address and generates the necessary control signals for the tape drive.

Detailed Logic Card 1.

The heart of this card is five integrated circuits called a FIFO (first in first out). The rest of the circuitry is for controlling data in or out of the FIFO.

The top half of the logic on page 1 of Card 1 contains logic associated with DMC transfers. In brief, when input ready (write) or output ready (read) goes high, a request (DIL) is sent to the computer to transfer data. The 25 μ sec one shot slows the transfer so that the drive will not hog the computer's time. When writing the FIFO is filled as soon as the write command is issued. This results in 64 DIL's being issued immediately; then a delay of around 17 ms until the tape drive is up to speed; then more transfers begin. The logic at the bottom of the page keeps track of data in the FIFO during a write. If less than 8 words remain in the FIFO and data is still being transferred, the 25 μ sec. Delay is eliminated.

The buffer (6B, 6C, 7C) on page 2 stores the 116 output data to avoid any timing conflict with the FIFO. The logic at the bottom of the page is used to control requesting more data during a write. This logic also generates a last word (LASTWD) signal which enters a FIFO as data. Last word is used to inform the formatter that this is the last word of data during a write.

Page 3 of Card 1 contains a buffer at the top of the page. This buffer is used to unpack the data from the tape drive during a read. The logic at the bottom of the page controls the loading of the buffer and the shifting of read data into the FIFO. Another circuit detects the condition of the FIFO being full and trying to load another word of data into it. This gives an OFER (overflow) indication. This overflow would result in a parity error to the computer.

The FIFO's are located on page 4. A 2 line to 1 line switch controls the input data to the FIFO. The data originates from the buffer on page 2 for a write and from the buffer on page 3 during a read. The logic in the lower left part of page 4 controls shift in (SI) and shift out (SO) as determined by the write mode. The lower right hand logic on page 4 applies the output data during a write eight bits at a time to the formatter. The upper right side of the page contains buffers (7408) for driving the input lines (INB) of the 116 buffer cards.

The last page of logic drawings for Card 1 contains a small amount of logic. The top flip flop is used to select which eight bits should be applied to the formatter during a write. The next flip flop is used to detect the condition of the tape unit requesting data and the FIFO being empty. This will cause an error condition UFER (Underflow). This error will be seen as a parity error by the computer. Two ports were provided for connection of a logic analyzer. The port at location 11F is the data out of the FIFO. At location 10G three clocks are provided shift in, shift out, and parity. Parity could also be used as a qualifier.

Detailed Logic Card 2.

On page 1 of the logic drawings for Card 2 the logic at the top of the page decodes the address as selected by address bits 7-10, if the tape unit

address is selected. The bottom of the page controls the DRL (data ready) line. If the DRL line is low, the computer program will skip the instruction after the SKS instruction.

The top portion of the logic on page 2 generates the appropriate five signals to control the operation of the tape drive. The table below lists the expected status of each line for all control commands. It should be noted that FGO- is the initiate command and that the rewind command is FREW-. The rewind command is not processed by the formatter.

<u>Command</u>	<u>FREV-</u>	<u>FWRT-</u>	<u>FWFM-</u>	<u>FEKASE-</u>	<u>FEDIT-</u>
OCP 214	H	H	H	H	H
OCP 414	H	L	L	L	H
OCP 614	H	L	L	H	H
OCP 1014	H	L	H	H	H
OCP 1114	H	H	H	L	H
OCP 1214	H	H	L	L	H
OCP 1514	L	H	H	L	H
OCP 1614	L	H	L	L	H

The bottom half of the drawing contains logic for generating the parity indication for the computer.

There are five dip switches located on this drawing; their use is listed below:

- Sw 1 Enable write even though tape is write protected.
- Sw 5 Selects the formatter address. (Open is address 0.)
- Sw 6 & 7 Selects tape unit address. (Open is tape unit 0.)
- Sw 8 Selects the read threshold. (Closed is extra low threshold.)

The last page of logic drawings for Card 2 contain logic to select the read or write mode. It should be noted that there are two write modes. Both modes are set when the write command (OCP 1014) is issued. The termination of the write modes is different. Write 1 will reset when the computer has output its last word (EOR). Write will reset when the tape unit has received the last

word from the FIFO. The middle of the page contains the logic to generate an interrupt (PIL 5) to the computer. This interrupt will be generated when the formatter goes not busy or at the end of a rewind. At the bottom of the page is the write monitor. This is used to give the operator an audible indication that data is being written on tape.

IV. TEST FIXTURE

It seemed that it would be advantageous to be able to test this system before going on the telescope. It was decided to use the HP 9825 calculator to accomplish this objective. Although the 9825 is easy to program, it has the disadvantage of being slow. This test fixture overcomes this problem and makes the 9825 look like a DDP 116 as far as the tape unit control electronics was concerned.

The logic drawings for three cards at the end of this report contain the logic necessary to make the 9825 look like a DDP 116. The main part of this logic is the 1024 x 16 bit random access memory. The rest of the logic is concerned with controlling the memory, generating 116 type I/O signals and the necessary handshake signals for the 9825.

The procedure to write tape is to load the memory from the calculator, then write from the memory to the tape unit control electronics. Read is the opposite transfer data from the control electronics to the memory, then from the memory to the calculator.

Three calculator programs were written to test the tape drive system. The first program is all operator controlled commands. In addition to being able to execute all commands, the operator can control what to write on tape and can dump on the display or printer what is read from tape. The second program is automatic. It executes all commands and tests for their proper execution.

The third program writes different data on tape and reads the data back comparing it with the data it wanted to write on the tape. This program can be made to continue this process until it reaches the end of tape.

This test fixture would also be useful for writing nine track tapes with a maximum record length of 1024 words from the 9825. Anyone interested in this should contact the digital lab in Green Bank for programming details.

V. CONCLUSION

Being able to purchase a formatter made the design of NRAO Electronics fairly simple.

Since this type of drive would be cheap as compared with a modern day version of the CDC drive, how well this drive holds up under 24 hours a day, seven days a week operation remains to be seen.

VI. CREDITS

Credit should be given to Ron Weimer for help in design of the electronic J. Turner and W. Vrable for construction of the electronics, the Machine Shop for construction of the chassis, and all the people involved in publishing this report.

MEMONIC LIST

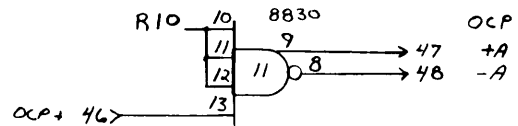
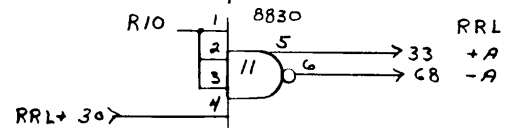
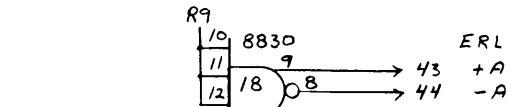
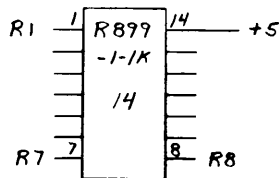
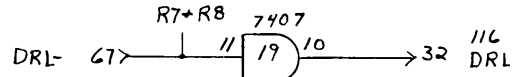
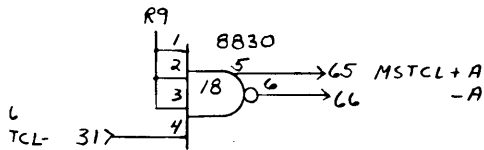
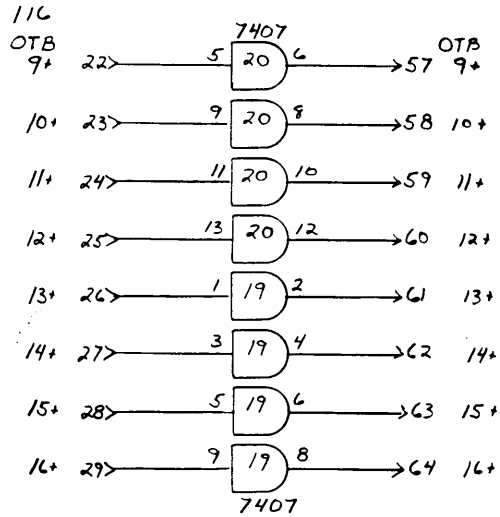
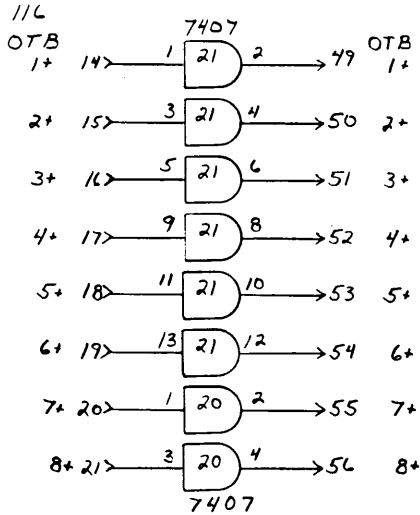
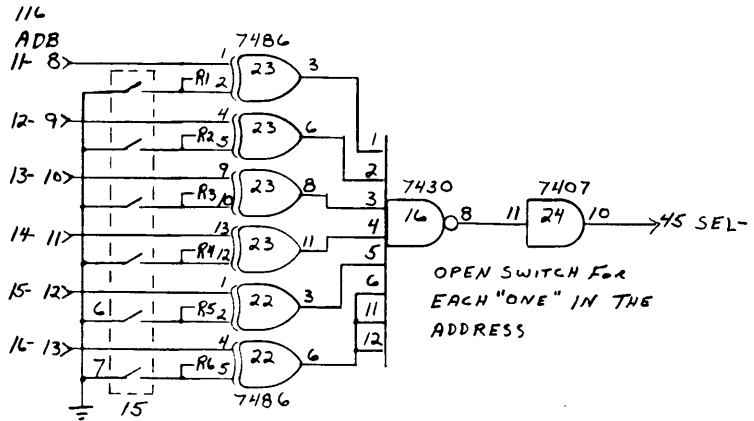
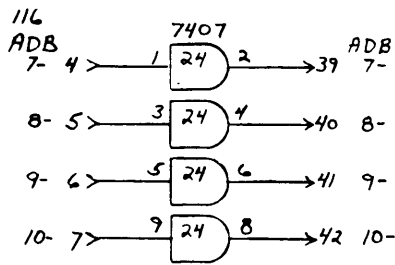
ACK	Acknowledge Priority Interrupt
ADBx	116 Address Buss
ADx	Decoded Address
DAL	Device Acknowledge Line
DIL	Device Interrupt Line
DRL	Data Ready Line
ENDIL	Enable DIL
EOT	End of Tape
ERL	End of Range Line
ERRST	Manual Reset of Local Error Indicato
FBY	Formatter Busy
FCCGID	Check Character Gate/ID Burst Detect
FCER	Formatter Corrected Error Detected
FDBY	Data Busy
FDWDS	Demand Write Data Strobe
FERASE	Erase Mode
FFAD	Formatter Address
FFBY	Formatter Busy
FFEN	Formatter Enable (Reset Formatter)
FFMK	File Mark Indication from Formatter
FFPT	File Protected
FGO	Initiate Command
FHER	Formatter Detected Hard Error
FLDP	Formatter Detected Load Point
FLWD	Last Word Indication to Formatter
FNRZ	NRZI Status from Formatter
FONL	Tape Unit On Line
FRDX	Read Data Lines
FREV	Reverse Mode
FSTR	Read Data Strobe
FRWD	Tape Unit Rewinding
FTAD	Transport Address

MEMONIC LIST (CONTINUED):

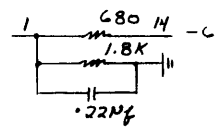
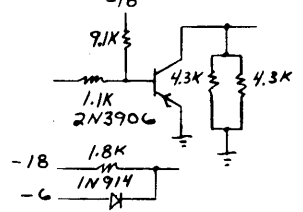
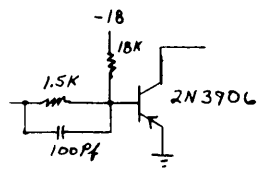
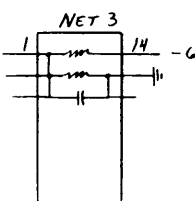
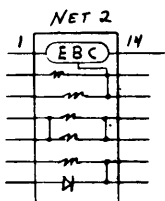
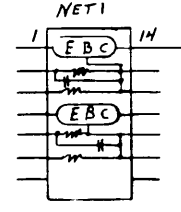
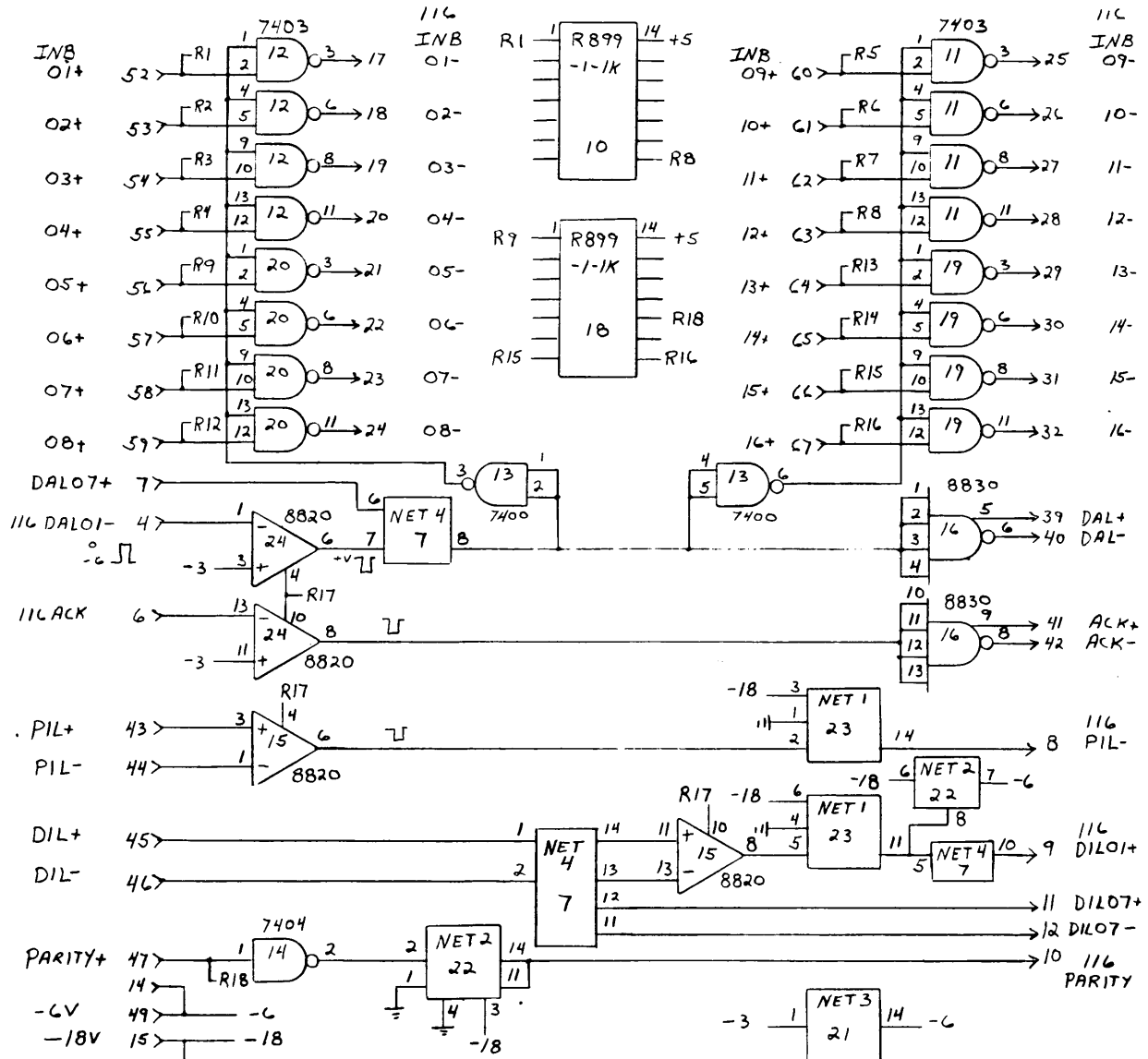
FTHR2	Read Threshold
FWDX	Write Data Lines to Formatter
FWFM	Write File Mark
FWRT	Write Mode
GORD	Read OCP
GOWR	Write OCP
INBXX	Input Data to 116
INHB	Inhibit Automatic Reset of Loc
IRX	Input Ready of FIFO
LASTWD	Last Word from 116
LLOWER	Load Lower Buffer (Read)
LOAD	Load Write Buffer
LUPPER	Load Upper Buffer (Read)
MSTCL	Master Clear
NRZ	NRZI Selected
OCP	Output Control Pulse from 116
OFER	Overflow Error
OR X	FIFO Output Ready
OTBXX	DDP 116 Output BUss
PARITY	Parity Indication for 116
PIL	Priority Interrupt Line
RDBXX	Read Data Buffer
SEL	Tape Address is Selected in 11
SIRD	Shift In (FIFO) Read
SIWR	Shift In (FIFO) Write
SORD	Shift Out (FIFO) Read
SOWR	Shift Out (FIFO) Write
UFER	Underflow Error
WRBXX	Write Data Buffer

LIST OF DRAWINGS

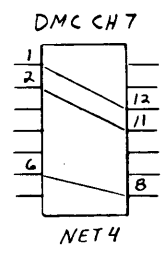
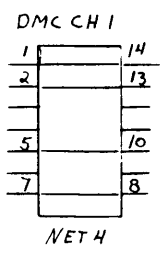
<u>Name</u>	<u>Page</u>
Address Deocde (116 Interface)	11
INB Buffer (116 Interface)	12
Control Logic (Card 1)	13-17
Control Logic (Card 2)	18-20
Front Panel	21
Memory Control (Test Fixture)	22
116/9825 Control (Test Fixture)	23-24
Memory (Test Fixture)	25-26



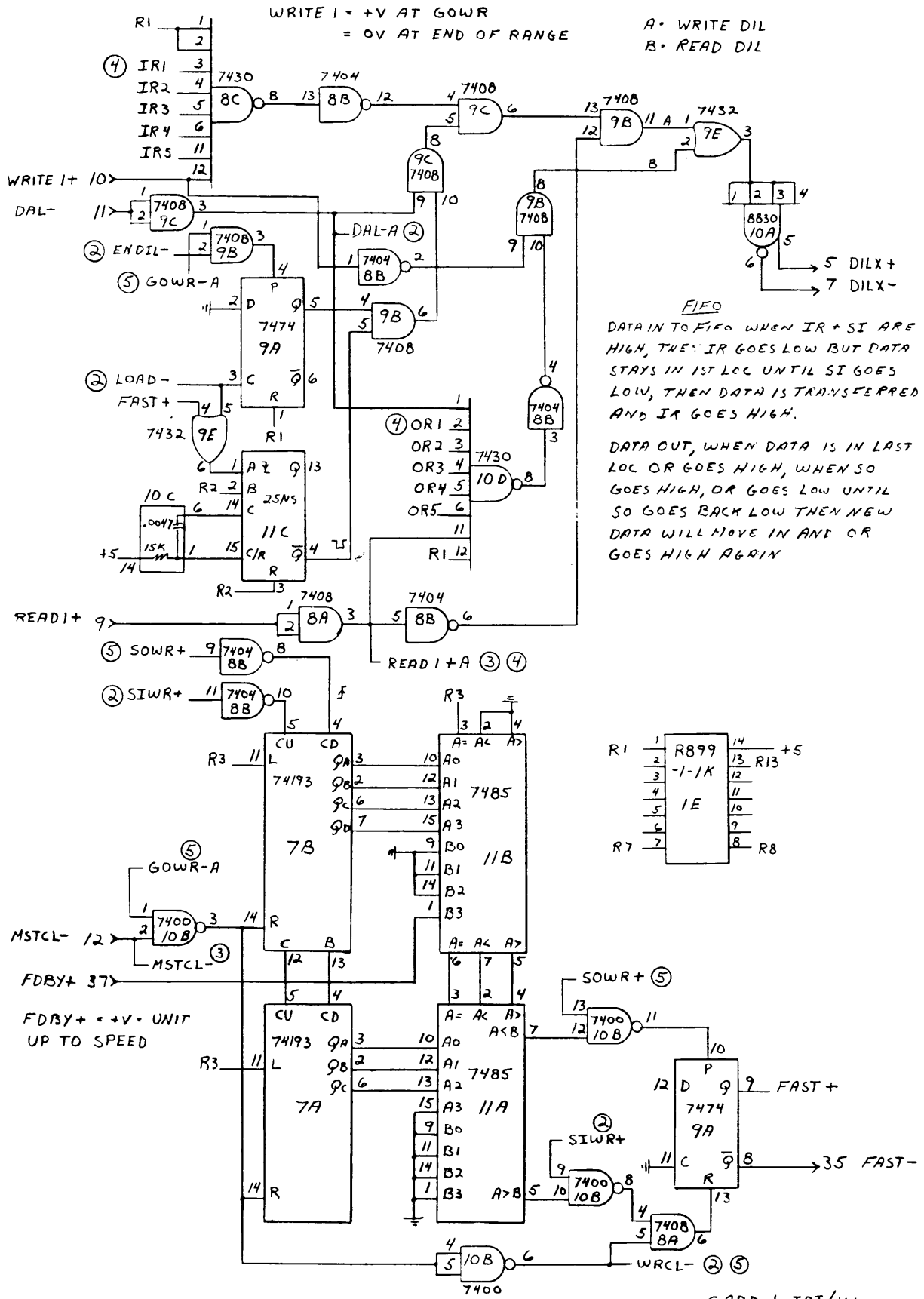
CARD 1
 300' IDT TAPE DRIVE
 116 INTERFACE
 ADB, OTB, MSTCL, DRL
 PAGE 1 OF 1



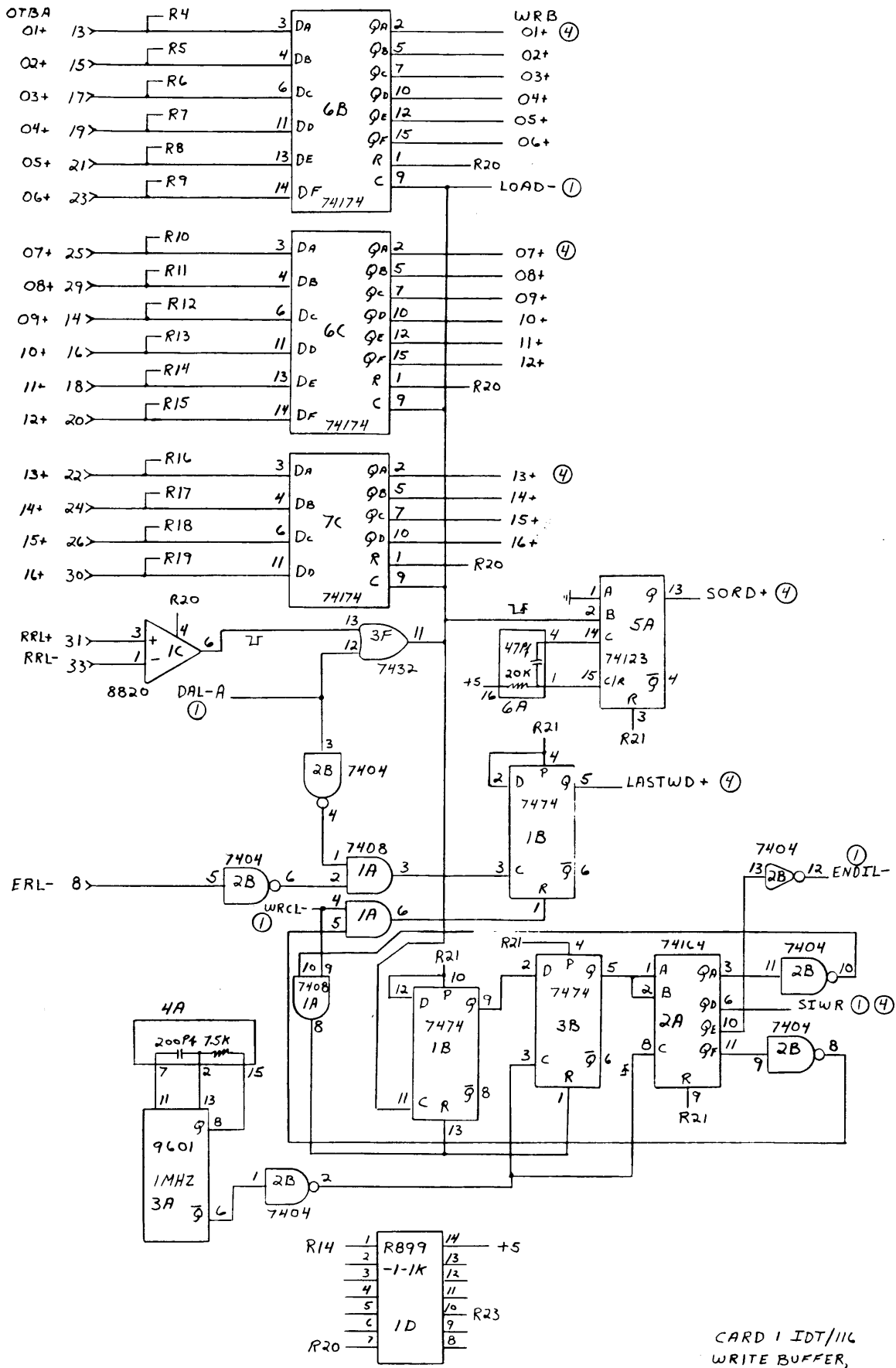
ALL RESISTORS 1/4 W



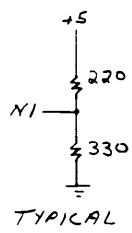
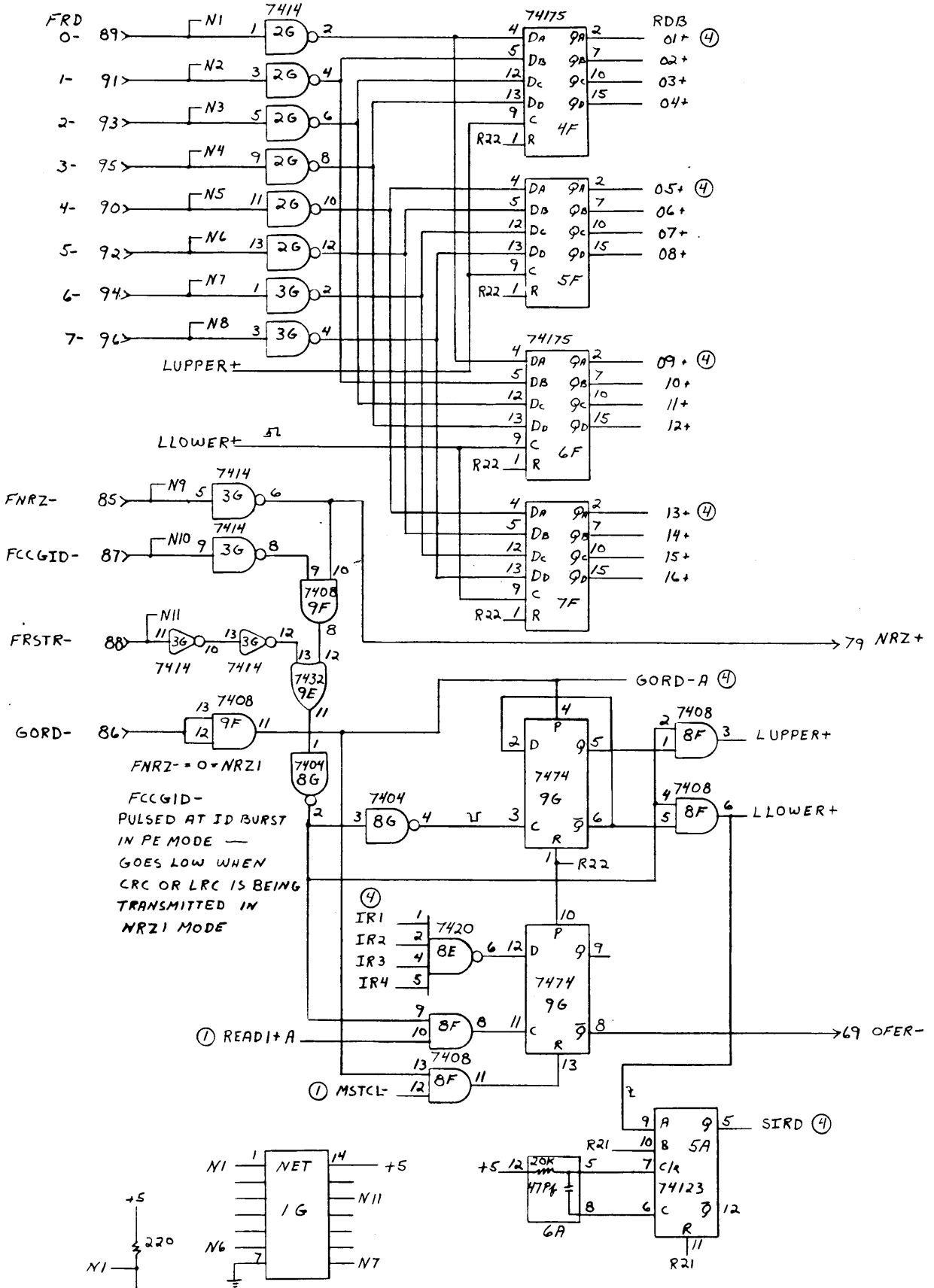
CARD 2
 300' IDT TAPE DRIVE
 INB, DIL, DAL, PIL, ACK
 116 INTERFACE
 PAGE 1 OF 1



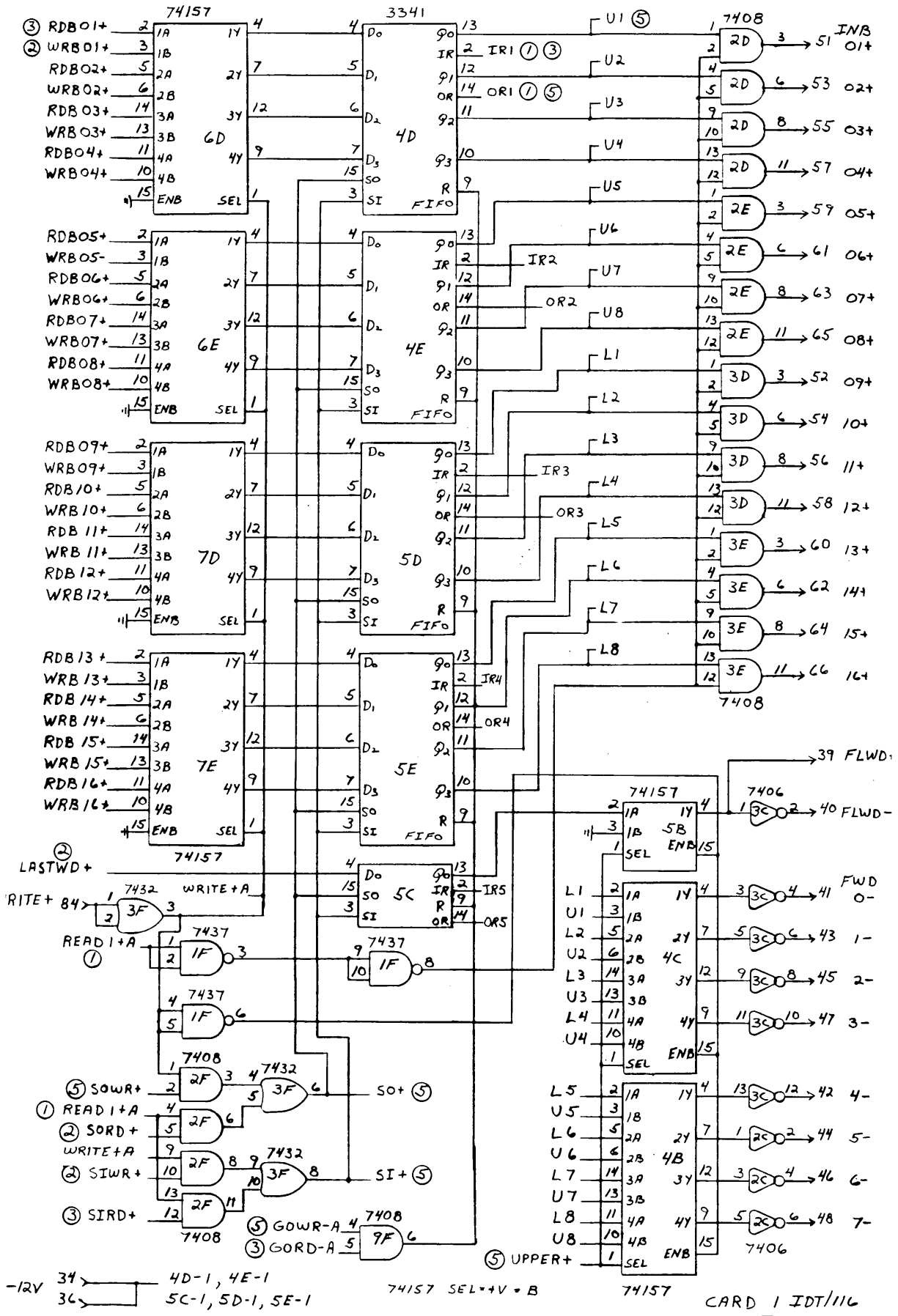
CARD 1 IDT/116
116 DMC DIL
PAGE 1 OF 5



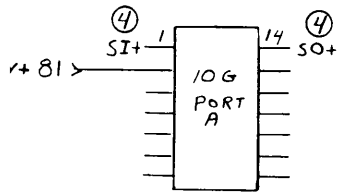
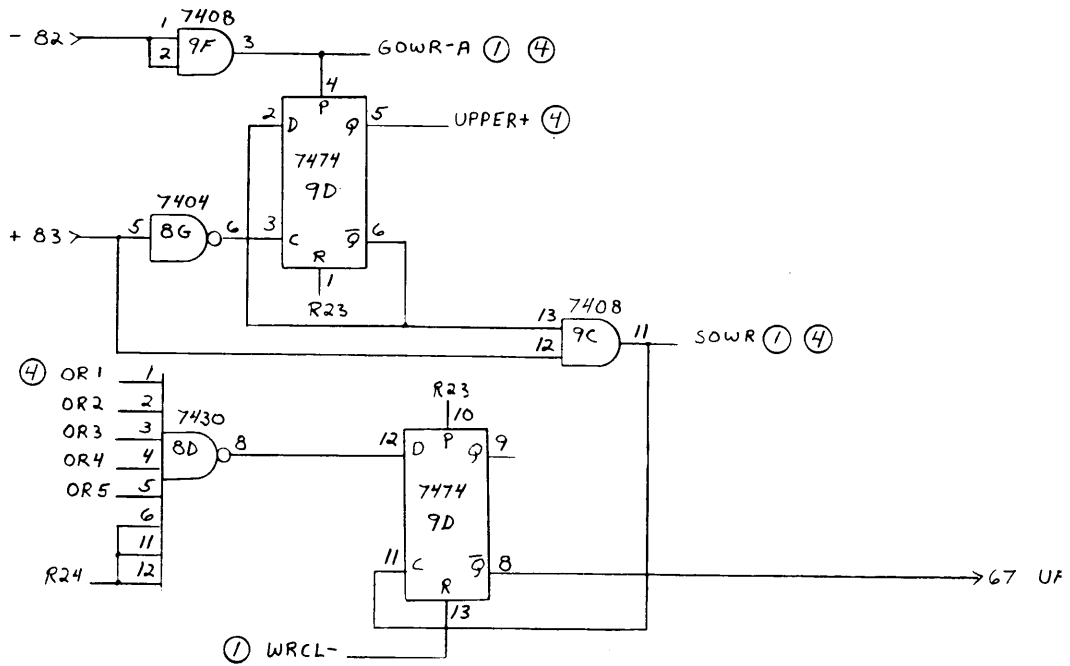
CARD 1 IDT/116
 WRITE BUFFER,
 LAST WORD, SHIFT OUT A
 SHIFT IN WRITE
 PAGE 2 OF 5 14



CARD 1 IDT/116
READ BUFFER +
CONTROL, SHIFT IN READ
PAGE 3 OF 5

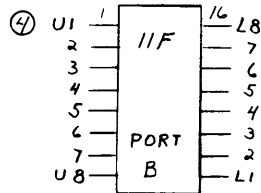


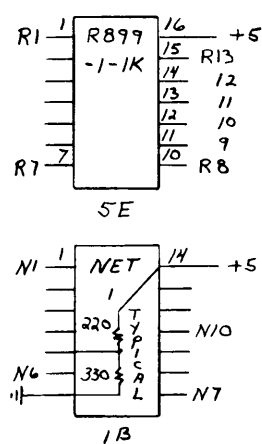
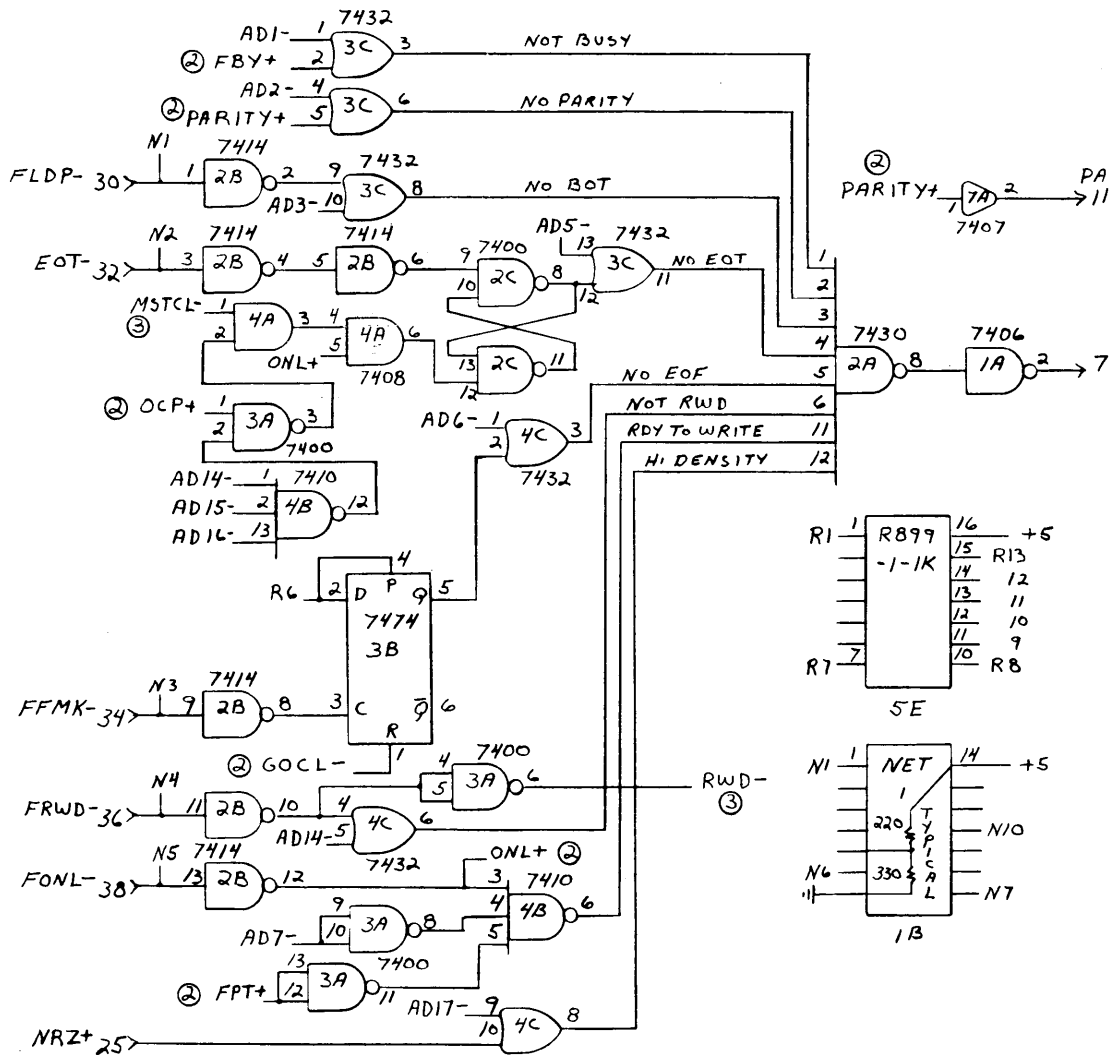
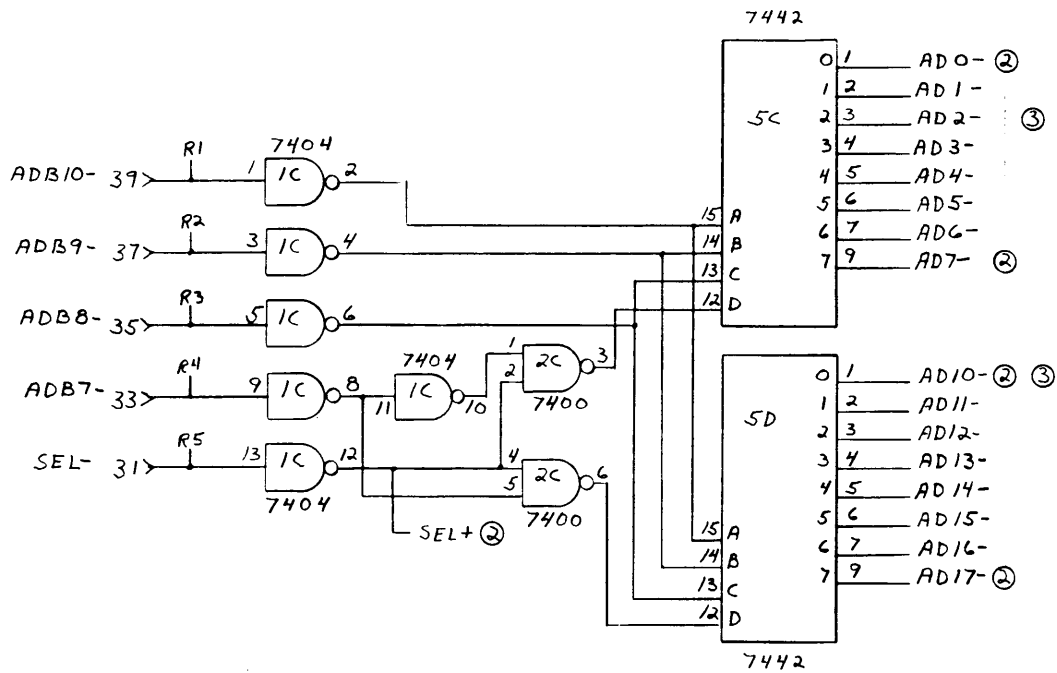
CARD 1 IDT/116
 FIFO, INB, TAPE
 WRITE DATA
 PAGE 4 OF 5 16



LOGIC ANALYZER
PORTS
PORT A CLK
PORT B DATA OUT
OF FIFO

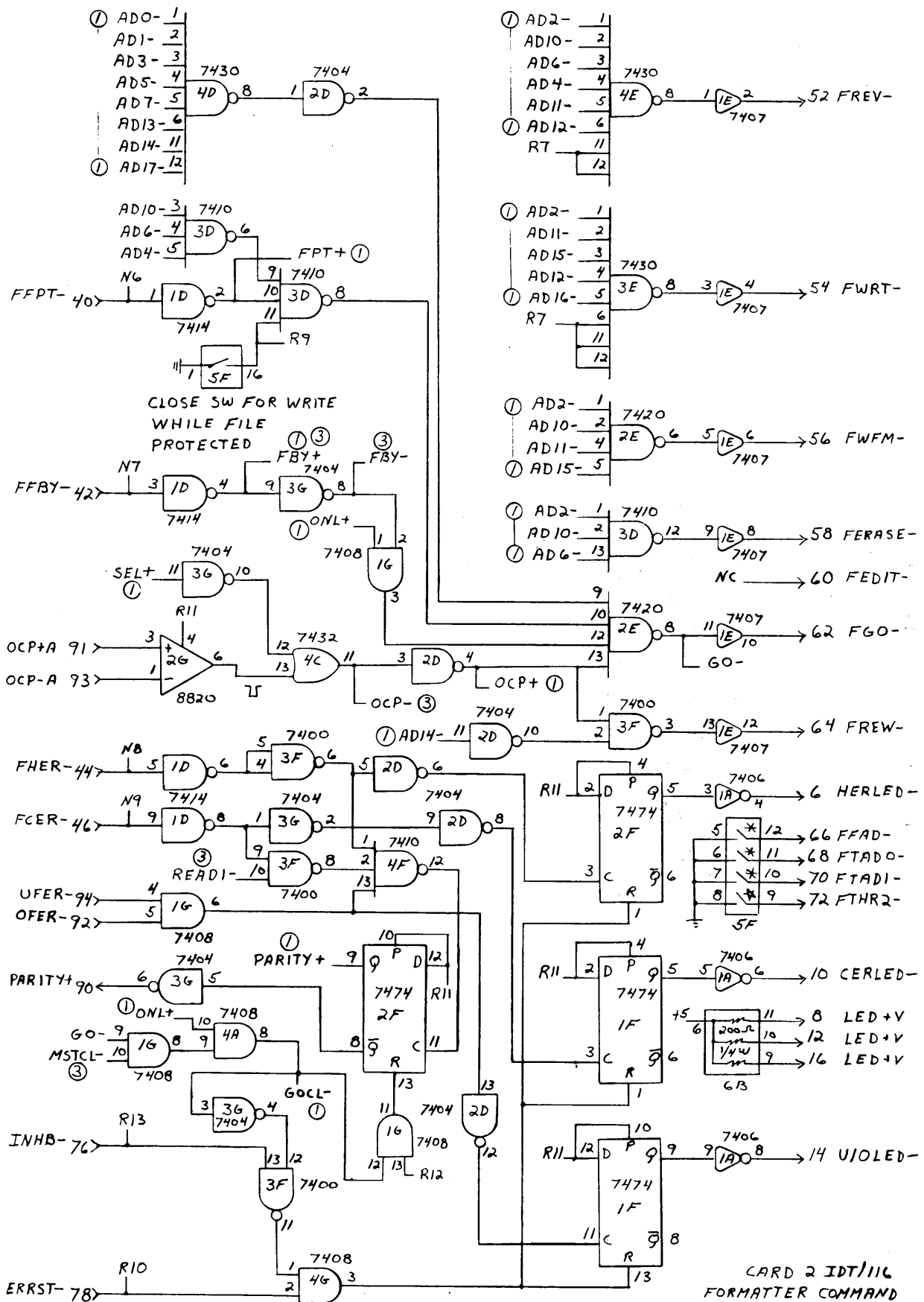
DATA
FROM FIFO





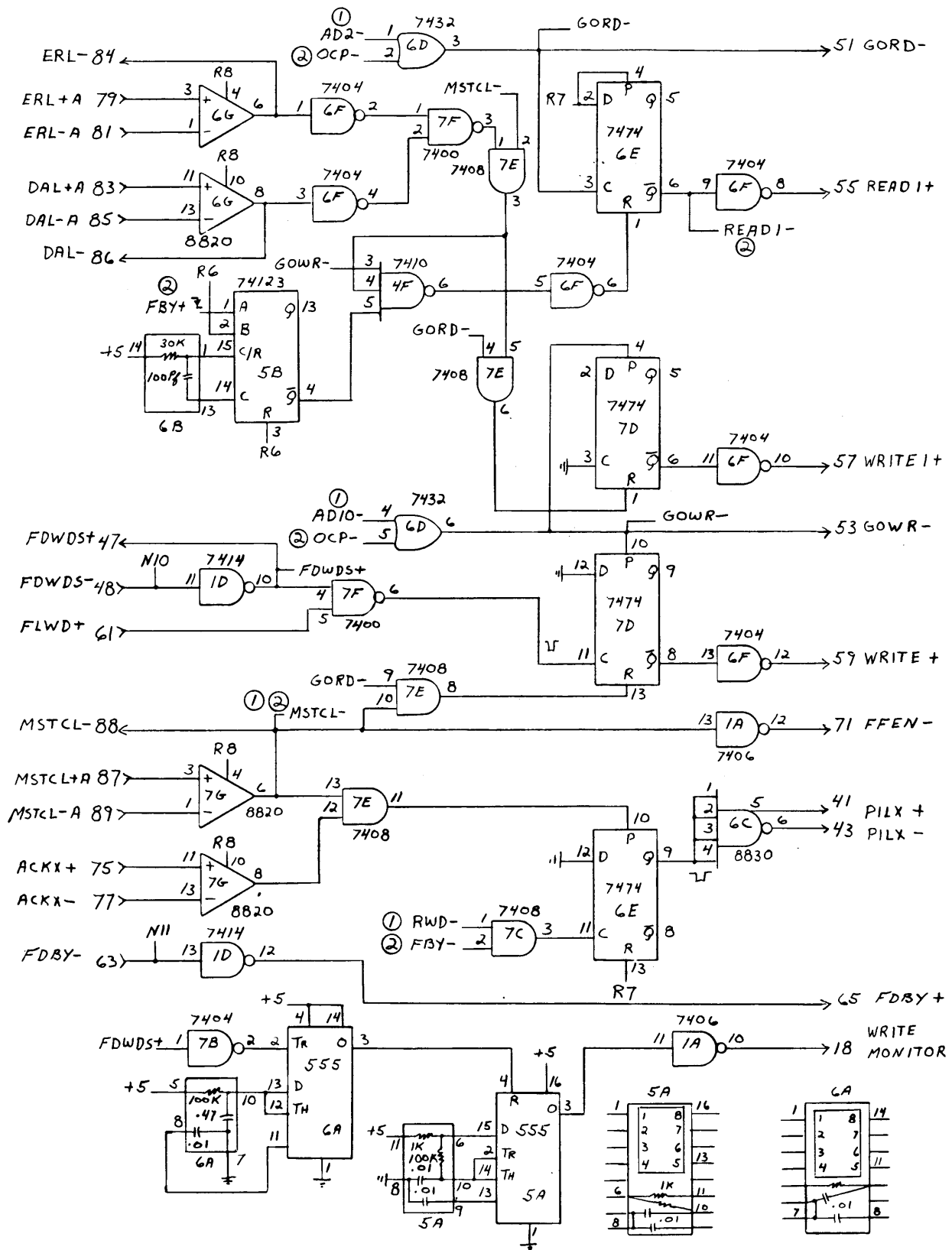
○ = SOURCE / DESTINATION

CARD 2 IDT/116
ADDRESS DECODE
SKS
PAGE 1 OF 3

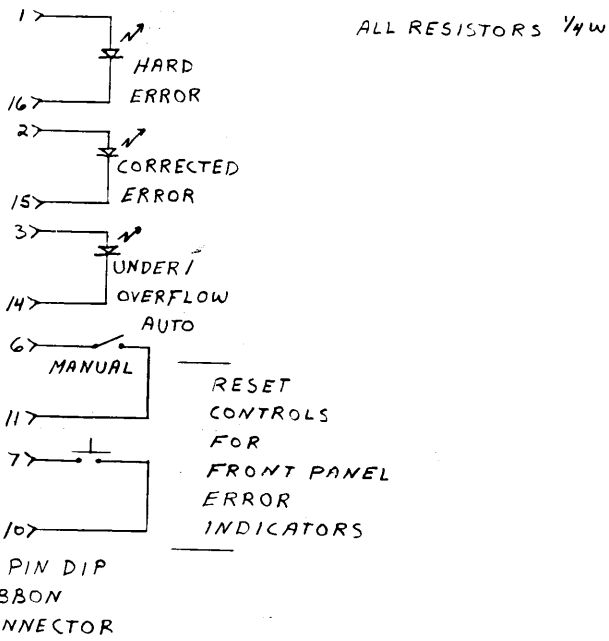
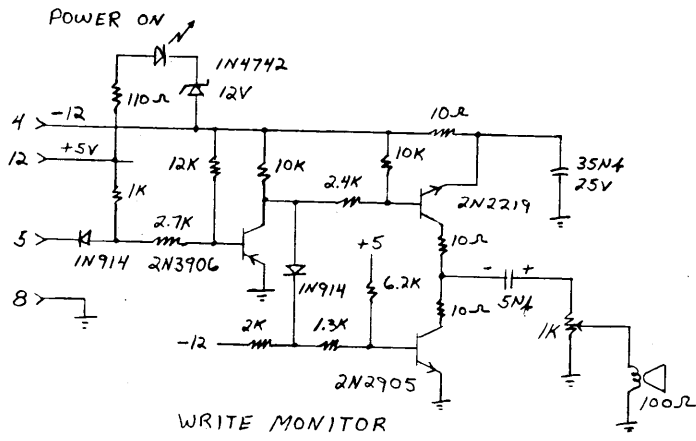


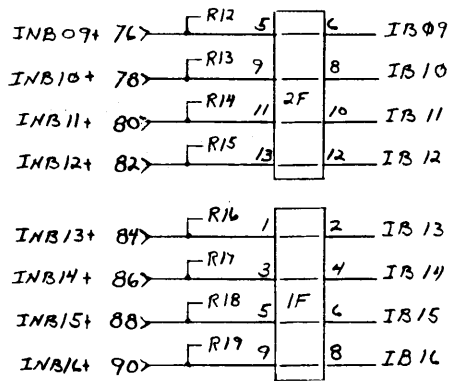
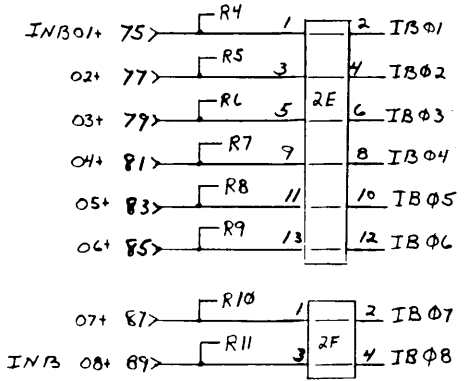
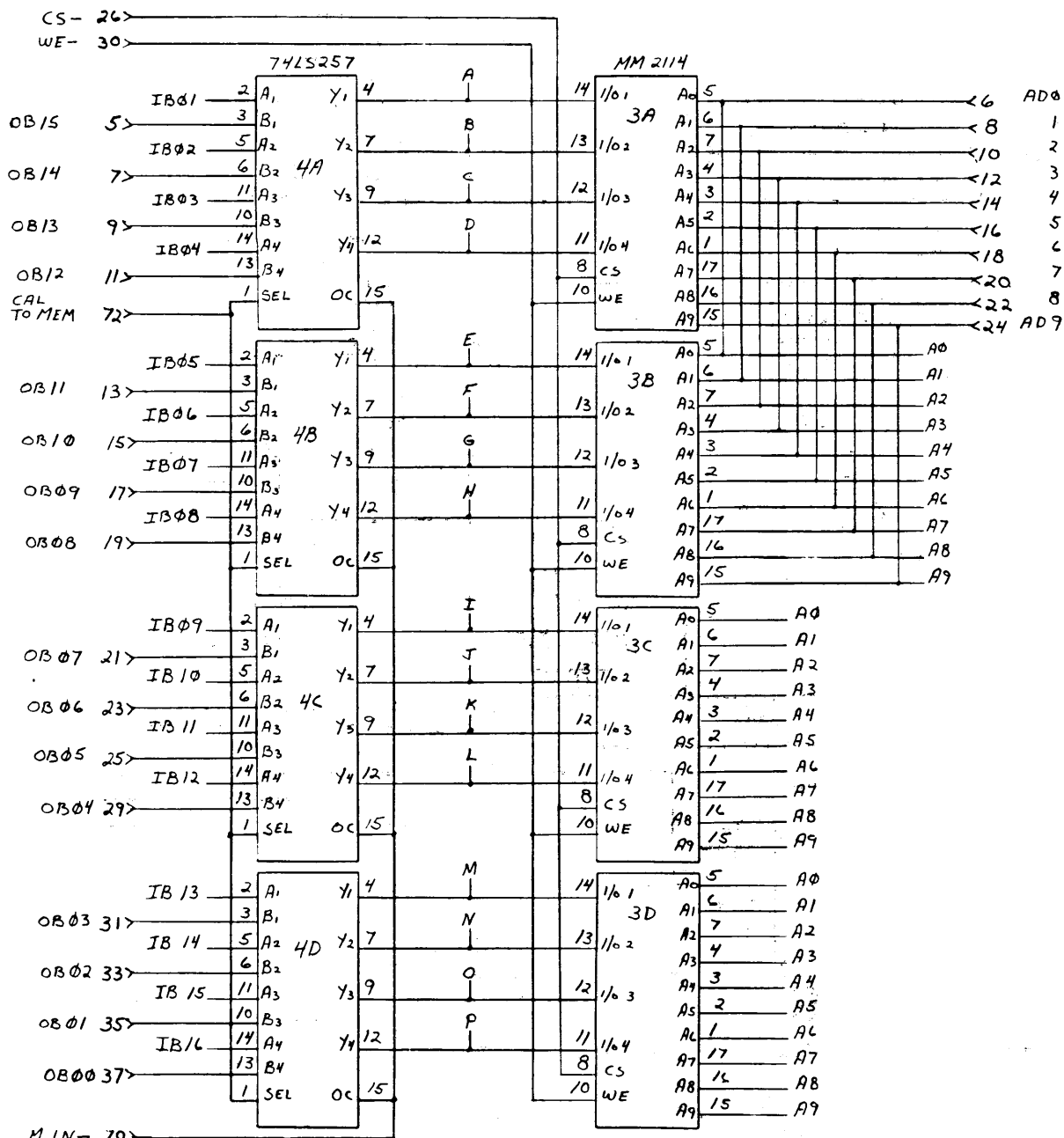
* CLOSE SW FOR EXTRA LOW READ THRESHOLD
 * THESE SW SHOULD NORMALLY BE OPEN

CARD 2 IDT/116
 FORMATTER COMMAND
 PARITY
 PAGE 2 OF 3



CARD 2 IDT/116
 READ/WRITE SELECT
 PAGE 3 OF 3





74LS257
 SEL=1=B
 OC=1=H/Z

MM 2114
 WRITE CS=0, WE=0
 READ CS=0, WE=1

TAPE UNIT TEST BOX
 MEMORY
 PAGE 1 OF 2

