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PROTOTYPE 2-4 GHz, LOW-NOISE, BALANCED AMPLIFIER DESIGN AND TESTS

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I. Introduction

In the 100-1000 GHz frequency range, where RF amplifiers are not available, superheterodyne radio astronomy receivers are constructed using a cryogenically cooled mixer as the first stage, followed by a low-noise IF amplifier. This IF amplifier, often a cooled FET amplifier, limits the instantaneous bandwidth of the system. Since the integration time required to achieve a given minimum detectable signal is inversely proportional to the instantaneous bandwidth of the receiver, it is desirable to make this bandwidth as large as practicable without sacrificing system noise performance.

At present, the IF amplifier used in most of the mixers constructed at NRAO is the L-band cooled FET amplifier reported by Weinreb, Fenstermacher, and Harris [1]. It has a bandwidth of 500 MHz, operating from 1.2 to 1.7 GHz. This report describes work on the design and construction of a cooled FET amplifier with 2 GHz bandwidth, operating from 2 to 4 GHz. The design work is a continuation of that reported by Kodaira, Weinreb and Granlund [2].

As it is difficult to achieve both good noise match and good power match over a wide bandwidth, a balanced amplifier design was chosen. The design incorporates two identical FET amplifiers with their inputs and outputs connected to quadrature 3 dB hybrids, as shown in Figure 1. In this configuration, reflections from the input (output) of each of the individual amplifiers cancel at the input (output) of the balanced amplifier. Thus, the input circuits of the individual amplifiers can be designed to present as nearly as possible an ideal noise match to the transistor, with little regard to the power match. This approach has

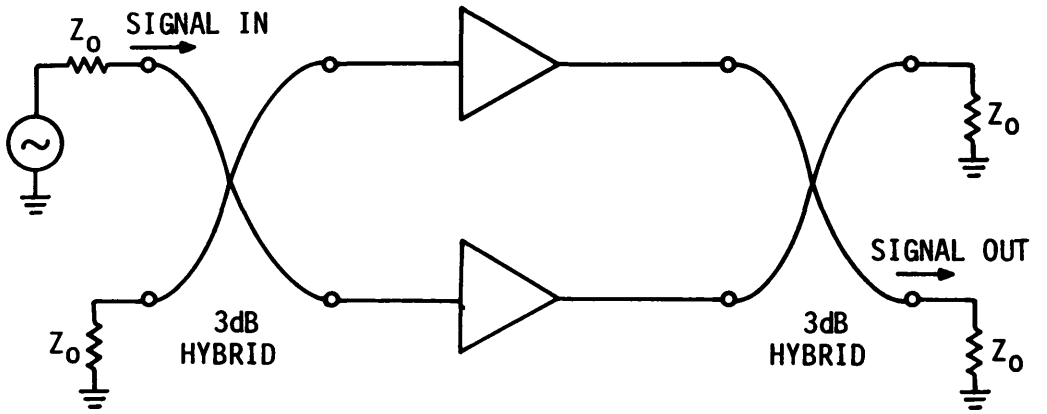


Figure 1. The balanced amplifier configuration.

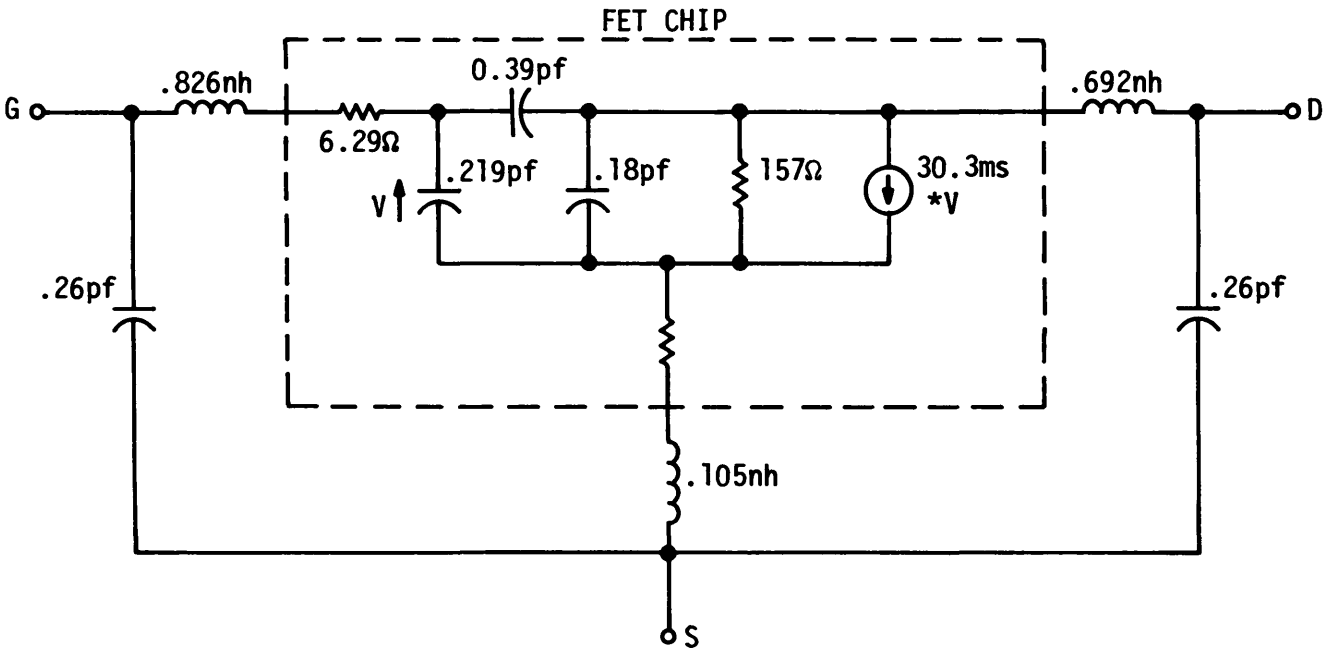


Figure 2. The FET model.

advantages over the use of a single-ended amplifier with an isolator: isolators which work well over this frequency range when cooled are difficult to construct, whereas hybrids can be readily built, and when constructed on alumina substrates are quite small.

The balanced amplifier was designed using the FARANT microwave analysis program developed at NRAO [3], [4], running on the HP9816 desktop computer. Transmission line circuits were used for the input and output matching networks. The transistor used was the Fujitsu FSC11 in chip form. The prototype amplifier, constructed using microstrip on alumina and cooled to 14K, exhibited a minimum noise temperature of 35K at 2.3 GHz, and an average noise temperature across the 2-4 GHz band of 60K. The maximum noise temperature was 120K at 4 GHz. The amplifier's gain was greater than 8 dB from 2 to 3.5 GHz, falling to 4 dB at 4 GHz. Input and output return losses were greater than 10 dB across the band.

In this report, details of the circuit design using FARANT will first be presented. Then, the construction of the amplifier will be described, and the test data will be presented. Finally, conclusions and suggestions for continuation of this work are given.

II. Circuit Design Using FARANT

The FARANT microwave analysis program is written in BASIC for the HP9816 computer. It consists of a simple mainline program and a large collection of subroutines which manipulate the two-port descriptions of networks, performing such functions as cascade, series, parallel, and branch. Subroutines for S-parameter, gain and noise analysis are available, as well as formatted output and powerful optimization routines. The designer writes a routine which calls

these various subroutines as needed and thus has great freedom in structuring the program to fit his needs. FARANT can deal with discrete R's, L's, and C's, as well as transmission lines and dependent sources.

In the design of the balanced amplifier, the following assumptions were made:

1) Since the S-parameters of the hybrid circuits to be used [5] were not available, assumptions had to be made about the source and load impedances seen by the FET amplifiers. The manufacturer specifies a VSWR of 1.3:1 or less for the hybrids across the band, so 50-ohm source and load impedances were assumed.

2) A circuit model of the form shown in Figure 2 was assumed for the FET. The element values were chosen to achieve a least-square-error fit of the network's S-parameters to those published for the packaged device [6] from 2 to 12 GHz. The parameters for the chip were then calculated by de-embedding the device from the case parasitics using FARANT.

3) The noise parameters of the FET at 14K were measured at a single frequency, 3 GHz [7]. Values of the noise parameters across the 2-4 GHz band were found by assuming that the noise parameters followed the trends predicted by the noise theory of Pucel, Haus, and Statz [8]. That is,

$$T_{min} \propto f$$
$$R_{opt} \propto f^{-1}$$
$$X_{opt} \propto f^{-1}$$
$$g_n \propto f^2$$

where f is frequency and the other quantities above are related to the noise temperature of the amplifier by

$$T = T_{min} + T_o \frac{g_n}{R_s} \left[(R_s - R_{opt})^2 + (X_s - X_{opt})^2 \right]$$

where $R_s + jX_s$ is the source impedance seen by the transistor, and T_o is 290K.

4) It was assumed that all transmission lines in the matching circuits (and the hybrids) were lossless. Dispersion was neglected. For the design, all transmission lines were assumed to have an effective dielectric constant of 1. This was later scaled to the proper values for microstrip on alumina.

The difficulty in designing a network to provide optimum noise match to an FET over a wide range of frequencies is that, as given above, R_{opt} and X_{opt}, the real and imaginary parts of the optimum source impedance, decrease with frequency. Thus, the optimum source impedance moves counterclockwise on the Smith chart with increasing frequency, while driving point impedance functions tend to move clockwise, when one is dealing with transmission line circuits.

The required rotation on the Smith chart can be realized over a limited frequency range by a resonance in the input circuit. Placing a shunt open line, which is half-wave resonant at the middle of the band, at a point where the reflection coefficient looking toward the source is purely real and negative is one possibility, and this approach was adopted in the present design. The length of line between the shunt stub and the transistor can then be adjusted to give an impedance looking toward the source with approximately the correct phase angle and counterclockwise rotation with frequency. Using this approach, Kodaira [2] designed an input matching network for the Mitsubishi MGF1412A transistor at room temperature over the 2 to 4 GHz band. His design is shown in Figure 3. The first step in designing the present amplifier was to re-optimize the Kodaira design with the MGF1412A parameters replaced by the parameters of the FSC11 at 14K.

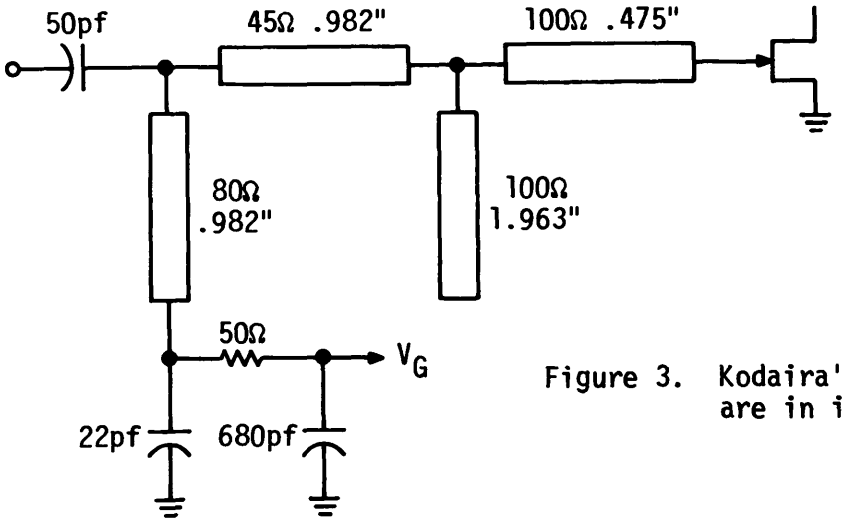


Figure 3. Kodaira's input network. Lengths are in inches for ε_r=1.

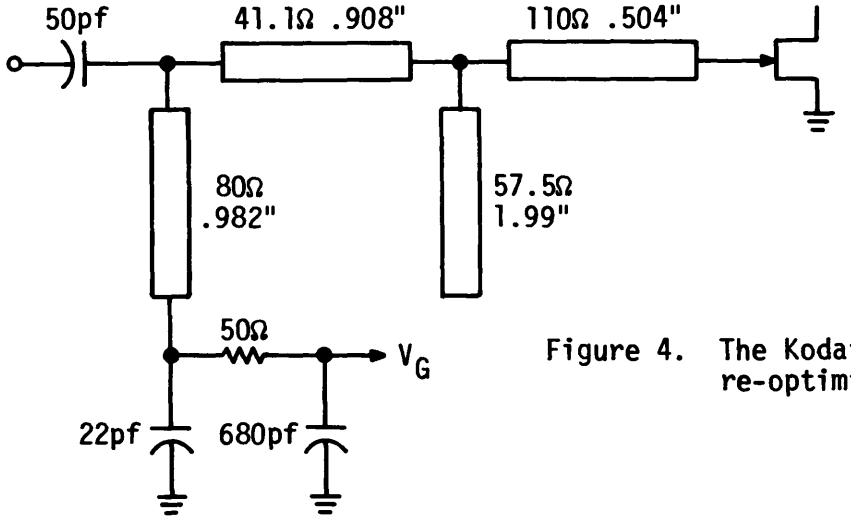


Figure 4. The Kodaira input network, re-optimized for the FSC11 at 14K.

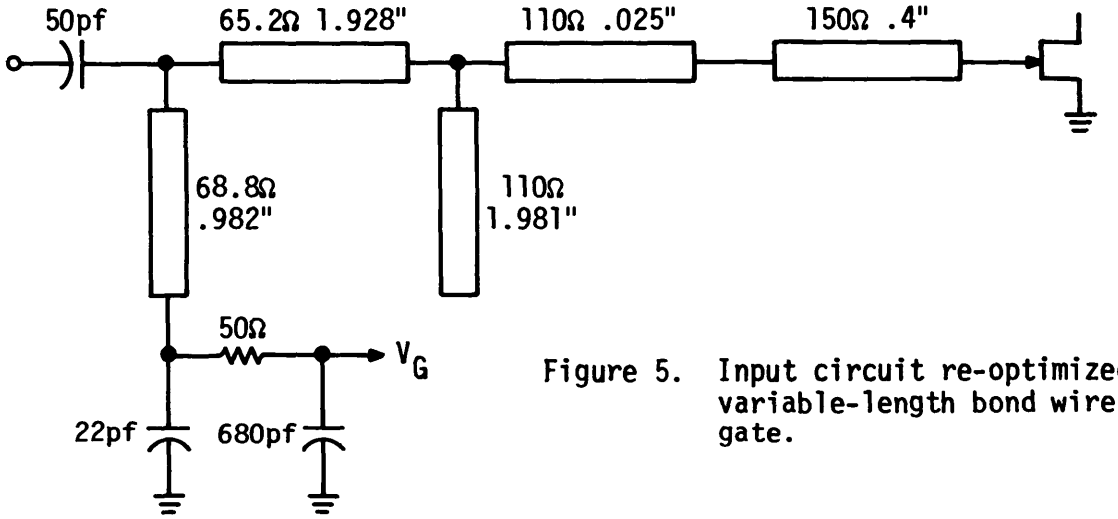


Figure 5. Input circuit re-optimized with a variable-length bond wire on the gate.

In using optimization in FARANT, the user specifies an objective function, Fvalue, which is positive and differentiable with respect to the circuit parameters to be optimized over. The optimization routine then varies the specified parameters to minimize Fvalue. In re-optimizing the Kodaira design, the lengths and characteristic impedances of all the transmission lines in the input network were allowed to vary and the objective function chosen was

$$\text{Fvalue} = \sum_{F=1.8\ \text{GHz}}^{4.2\ \text{GHz}} (T - T_{min})^2$$

The results of this optimization are shown in Figure 4.

Following this first optimization, methods for tuning the amplifier were investigated. Tuning freedom is quite limited when dealing with microstrip circuits. The characteristic impedances of transmission lines cannot be changed, though they can be lengthened, or have lumped elements connected to them by the use of bond wires and tuning pads. Also, the lengths of the various bond wires connecting the transistor to the circuit board can be varied. This last parameter was found to have the strongest effect on the amplifier's performance: increasing the length of the bond wire connecting the gate of the transistor to the matching circuit improved the noise match. This bond wire was modeled as a 150-ohm transmission line. The input network was re-optimized using the same objective function, with the length of this bond wire variable. The result is shown in Figure 5. The impedance which this matching network presents, with respect to Z_{opt}, is shown in Figure 6. It is seen that a 0.4" bond wire is required, a length which is not practical from a mechanical point of view. To realize this bond wire and have some freedom in adjusting its length, it was decided that an array of bonding pads, each only 0.003" on a side, would

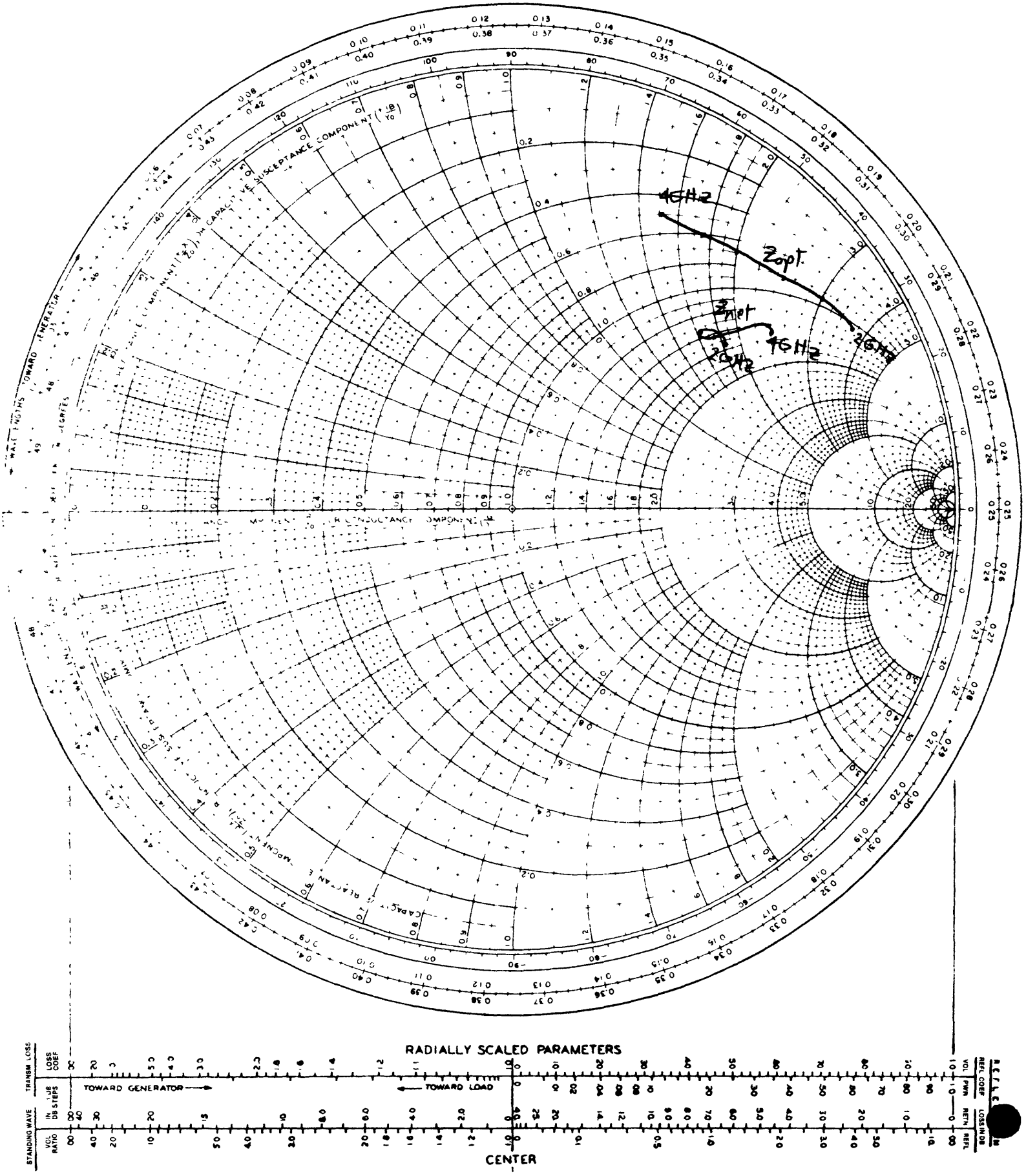


Fig. 6. Impedance seen by transistor, compared with Z_{opt}.

be placed on the alumina. The bond wire could then be stitched between pads, as shown in Figure 7. The pads themselves represent a shunt capacitive reactance on the order of a few thousand ohms, not greatly affecting the characteristics of the bond wire.

With the input circuit complete, the output circuit of Kodaira was re-optimized to give flat gain across the band. All parameters of the output circuit were allowed to vary and the objective function chosen was

$$F_{value} = Var(G) + \left[\frac{\Sigma(T - T_{min})^2}{\Sigma(T - T_{min})^2_{opt}} \right]^{64}$$

where Var(G) is the variance of the gain across the band, and the subscript "opt" indicates the value of that quantity given by the previous optimization. Thus, Fvalue decreases with decreasing Var(G), but increases sharply if the noise temperature across the band increases, so that the optimization flattens the gain without harming the noise figure.

The final circuit for the amplifier is shown in Figure 8, and its predicted gain and noise performance is shown in Figure 9.

III. Fabrication

The matching networks for the 2-4 GHz amplifier were fabricated using 0.025 inch thick alumina substrates coated with tantalum nitride/titanium-tungsten/gold. The gold layer was about 250 microinches thick. The design equations of Wheeler [9] were used to calculate line widths and propagation velocities for the transmission lines. The circuits were laid out so that the input and output matching networks each fit within a 1/2" x 1/2" area. Then, matching circuits for both

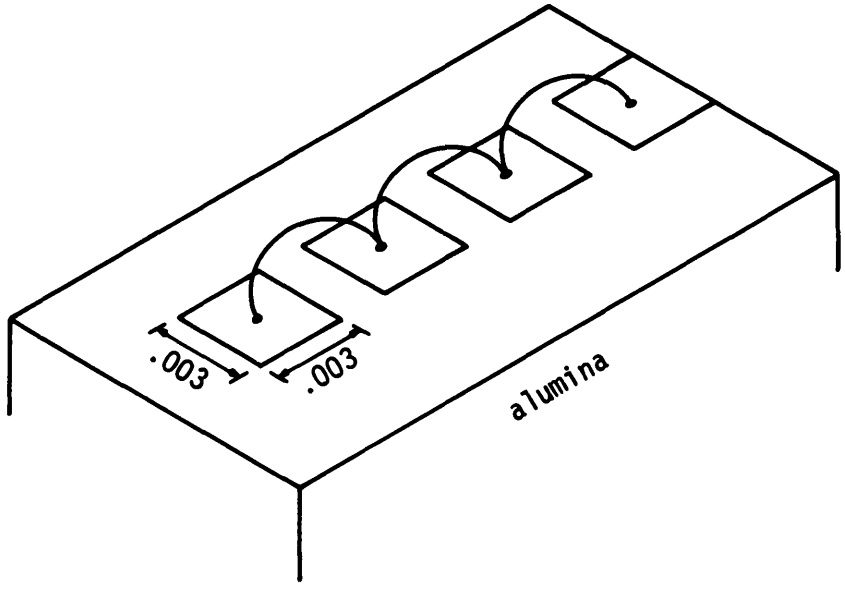


Figure 7. Realization of the long bond wire.

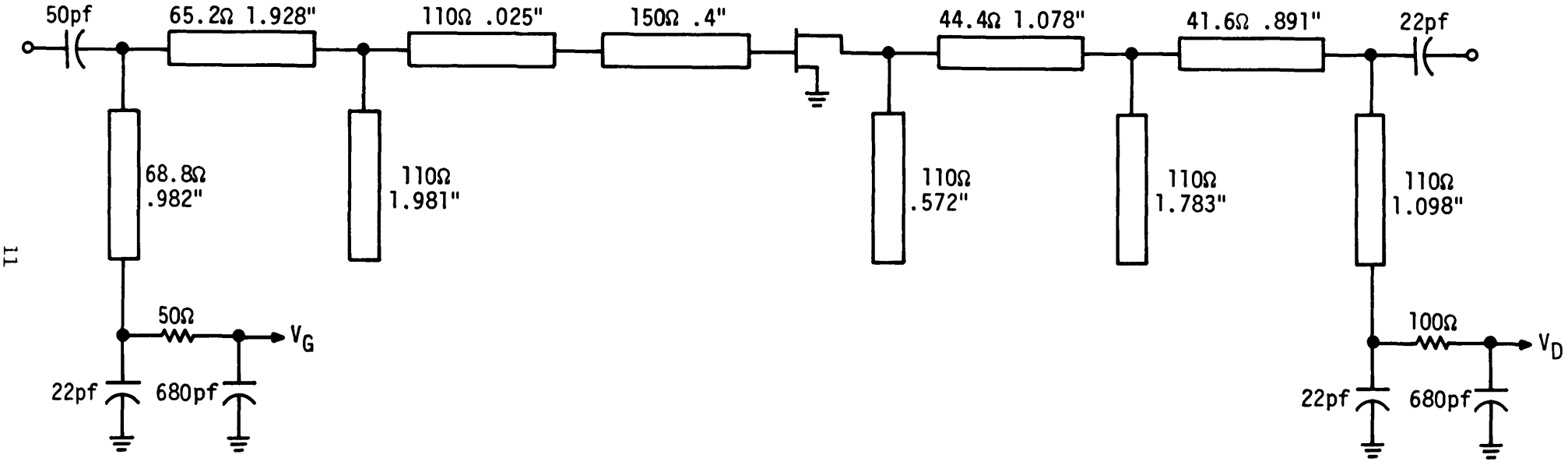


Figure 8. The final amplifier circuit.

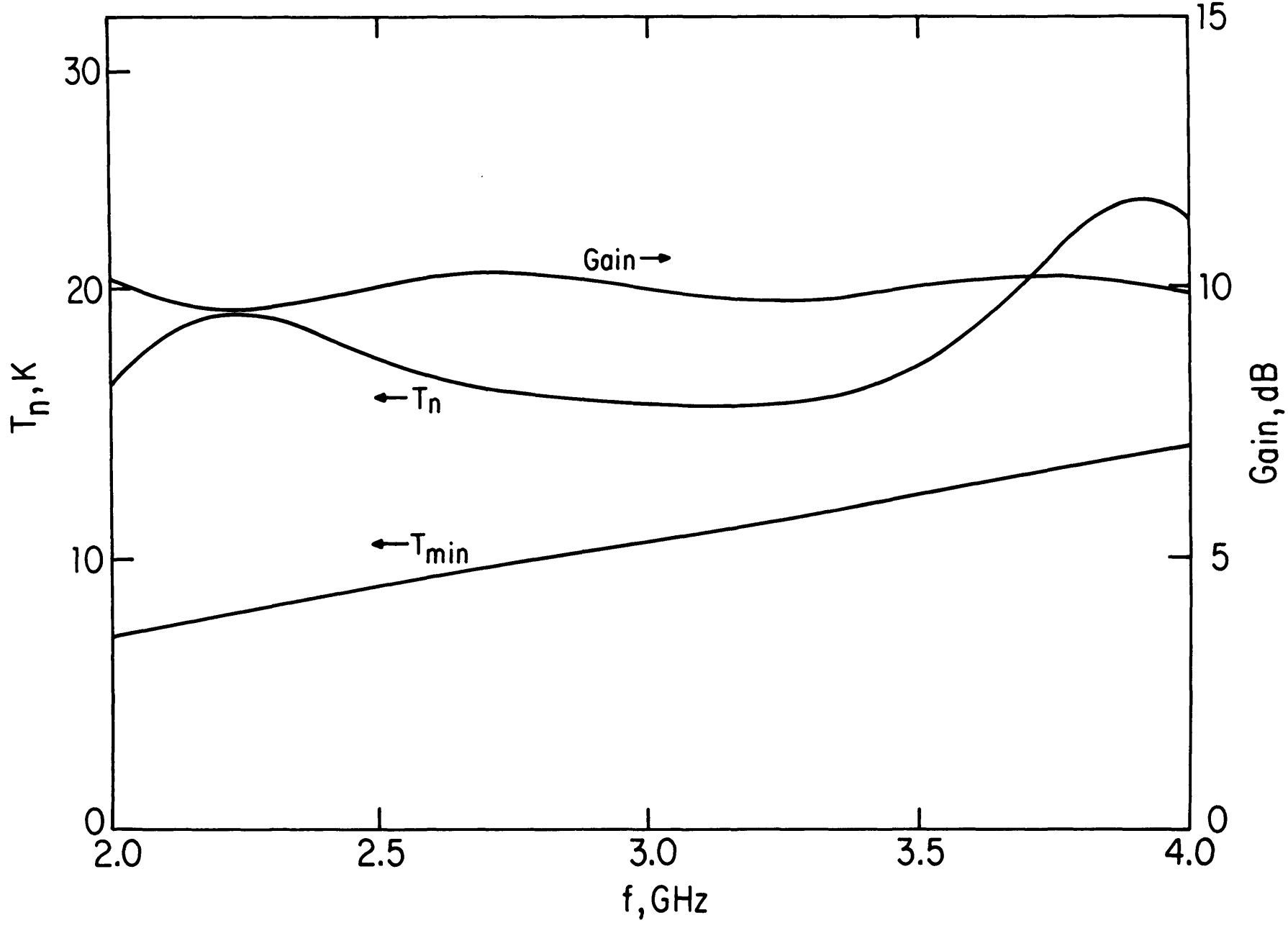


Figure 9. Gain & noise predicted for the amplifier.

halves of the balanced amplifier could be fabricated on two 1" x 1/2" circuit boards, one containing two input networks, and the other, two outputs.

Photomasks for the circuits were made, at twenty times actual size, using a rubylith cutter which allowed positioning of the knife edge to within 0.01 mm. Lines on the masks were widened by the equivalent of two substrate coating thicknesses to allow for undercutting during etching. The masks were photo-reduced onto two inch, high resolution plates, and transferred to iron oxide plates for contact printing. The networks were then fabricated from the masks using standard photolithographic and wet etching techniques.

The 3 dB quadrature hybrids used [5] were microstrip circuits fabricated on 0.4" x 0.9" x 0.025" alumina substrates with chrome/copper/gold conductors. Their specifications over the 2-4 GHz band included a maximum VSWR of 1.3, output phase of $90^{o} \pm 3^{o}$, and output balance of $\pm$ 0.6 dB.

The input and output circuit boards for the FET amplifiers were placed in a gold-plated copper box, with a 0.030" high ridge between them, upon which the transistors were mounted with conducting epoxy [10]. The circuit boards themselves were held in place with low temperature solder [11] to allow easy removal. SMA connectors were soldered to the microstrip lines so that the inputs and outputs of both FET amplifiers were accessible. Bias lines entered the box through a seven-pin connector. A thermal compression bonder was used to attach 0.7 mil gold bond wires to make the necessary connections to the FET's. Each of the hybrids was placed in its own smaller gold-plated copper box, with SMA connectors soldered to all four ports. Low temperature solder was used here as well. In this configuration, the hybrids and amplifiers could all be tested separately, tuned up and then connected to form the balanced amplifier.

IV. Testing

Gain and return loss measurements on the amplifiers were made using a sweeper and a scalar network analyzer. These instruments, giving rapid indication of changes in gain and SWR, were used for tuning the amplifiers. Noise and gain measurements were made using a noise diode and a standard 2-4 GHz receiver, as shown in Figure 10. This receiver has a maximum noise temperature of about 1700K. When calibrated with a liquid nitrogen hot/cold load, its error in noise temperature measurement when the device under test has about 10 dB gain is ± 5K.

In the first tests, a single amplifier was biased and its gain and noise were measured at room temperature.

On first power-up, the gain and noise properties of the amplifier were tuned too low in frequency, with gain dropping sharply at about 3.5 GHz. The amplifier also had a tendency to oscillate at 1.9 GHz. A bit of probing determined that the bond wire connecting the gate to the input network was presenting too large an inductance to the transistor. Its length was reduced in steps until no further steps improved performance. The gain and noise of the amplifier after these steps, at room temperature, is shown in Figure 11. At this point the gate connection had been changed from a single bond wire 0.4" long to a 0.2" long run of two bond wires side by side. This probably indicates that modeling the bond wire as a 150-ohm transmission line with dielectric constant 1 is not accurate.

The gain of the amplifier across the band is about 10 ± 2 dB, sloping downward with increasing frequency. The computer model predicts about 10 ± 0.5 dB gain, essentially flat across the band. This error probably represents an error in the element values used for the FET circuit model. As noted above, these elements were chosen for a best fit to the published S-parameters over frequencies from

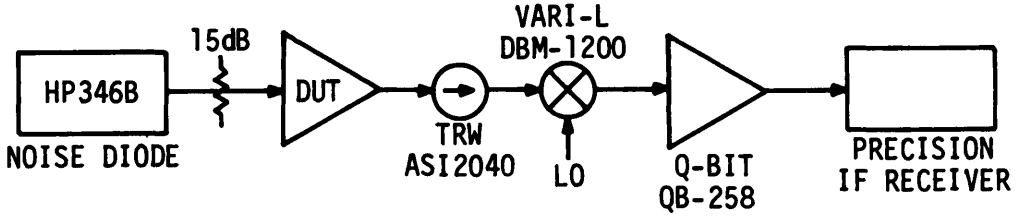
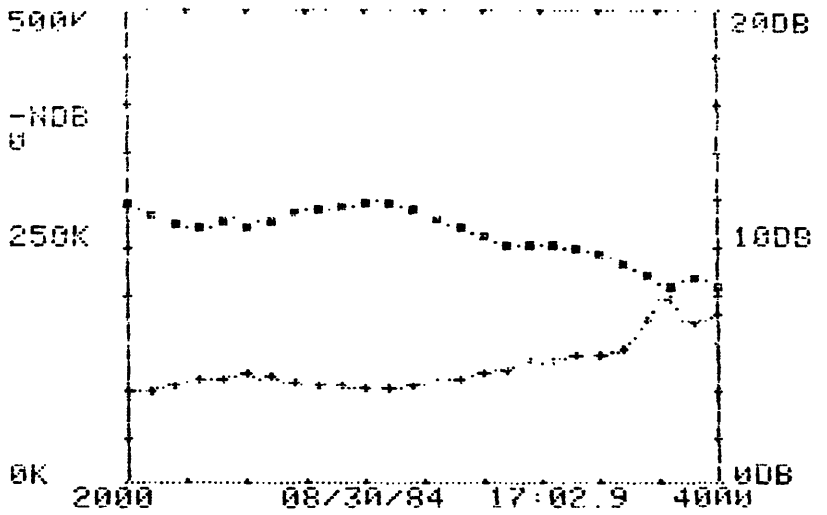


Figure 10. Noise measurement test set.

1) DOUBLE BOND WIRE ON GATE;SHORT OUTPUT STUB REDUCED;FSC11 3V,22MA
17:02.9 08/30/84 TAU=123.7 TLO=97.4 @ 2040 GL=8.3 GH=11.9 T=-1000K
-10,-100,-10 -10,-100,-10 -10,-100,-10



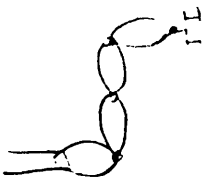


Fig. 11. Single amplifier at room temperature.

2 to 12 GHz. An examination of the model over the 2-4 GHz band shows, however, that it yields a value for S_{21} which increases slightly in magnitude as frequency increases across the band, whereas the manufacturer's data shows $|S_{21}|$ decreasing across the band.

Next, the single FET amplifier was cooled to 16K with no change in tuning. The results are seen in Figure 12. Unexpectedly, the gain increased to 17 dB at the low end of the band and dropped to 4 dB at the high end. The noise performance, with an average noise temperature of 55K across the band, is worse by a factor of three than that predicted by the computer analysis. Apparently the optimized design used here is too sensitive to small variations in transistor parameters to provide very good broad band performance. Another possibility is that the microstrip transmission lines do not match closely enough the values specificed by the design. Loss may be a problem, as well.

When the test amplifier was warming up from its first cryogenic test, the alumina substrate holding the input matching networks cracked, opening bias lines and rendering the amplifier inoperable. The amplifier was repaired by stitching bond wires across the cracks in the lines, but it is apparent that in the future, another case material, such as Kovar, with a thermal coefficient of expansion near that of alumina will have to be used.

Finally, the second FET amplifier was tuned so that its response matched that of the first as nearly as possible, and the two amplifiers were connected to hybrids to form the balanced amplifier. The gain and noise of the balanced amplifier at room temperature is shown in Figure 13. Some degradation in gain and noise performance, due to losses and asymmetries in the hybrids, is evident, but the input and output return losses were improved greatly, from 1 or 2 dB for a single amplifier to better than 10 dB for the balanced amplifier.

1) 3.75V,25MA,16.2K
14:25.0 08/31/84 TAU=54.6 TLO=26 @ 2200 GL=4.3 GH=17.3 T=16.3K
3.73,24.9,-.936 0,0,-1.961 .02,0,-7.079

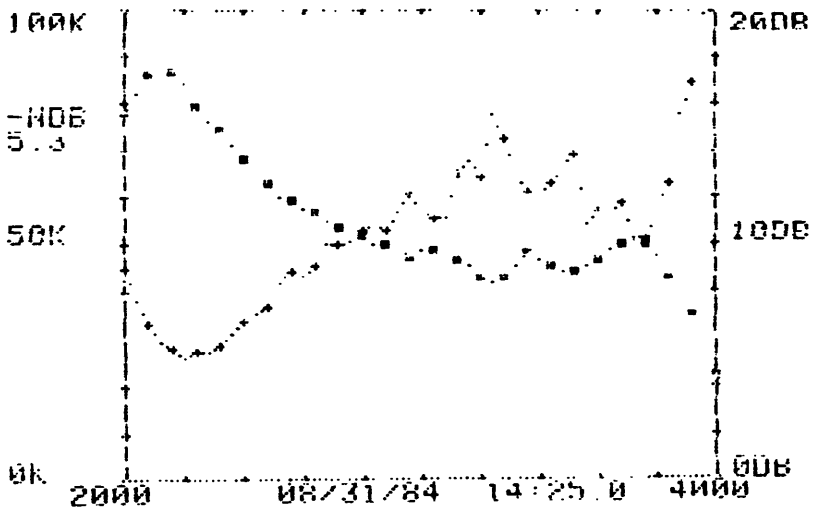


Fig. 12. Single amplifier at 16K.

1) BALANCED AMPLIFIER;3.75V,25MA
10:39.9 09/01/84 TAU=225.6 TLO=171.1 @ 2120 GL=6.8 GH=12.8 T=297.8K
3.72,24.8,-.68 3.76,24.7,-.531 .05,0,.659

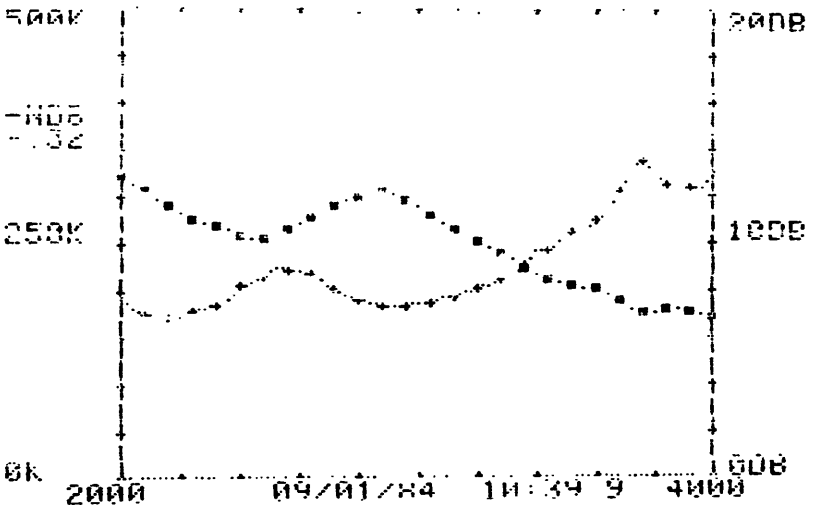


Fig. 13. Balanced amplifier at room temperature.

The balanced amplifier was cooled to 14K, and its cooled gain and noise are shown in Figure 14.

V. Conclusions and Suggestions for Further Work

Given the fact that lumped elements tend to be lossy at the upper end of the 2-4 GHz band, the designer of a broadband low-noise amplifier in this range is constrained to design in microstrip, with chip transistors, and is then faced with the prospect of a fabricated circuit which is, to a large extent, untunable. In these circumstances, one approach is to optimize the design to known parameters and allow for tuning wherever possible, assuming that the design will be approximately correct and that the meager amount of tuning which one can incorporate into the design will be sufficient to achieve good performance. This was the approach taken in the present work, and the parameters of the prototype amplifier did not approach those predicted. We suggest that an alternative approach now be investigated: a design which has suboptimum noise performance, but which can tolerate changes in transistor parameters. This is, the optimization criterion should not be maximum performance, but minimum sensitivity to transistor parameters. Whether a reasonably insensitive design can still have good characteristics is yet to be determined. Unfortunately, sensitivity optimization is likely to require a considerable amount of computer time.

To pursue further the work on the present amplifier, the next step would be to make accurate S-parameter measurements of the amplifiers, or of the disconnected circuit boards, to determine how well the microstrip circuits realize the intended design and how far the FET's are from their models.

Alternatives to microstrip, such as coaxial line designs, should also be investigated.

1) BALANCED AMPLIFIER AT 14.3K;FET1:3.75U,15MA;FET2:3.75U,30MA
05:57.9 09/02/84 TAU=59.9 TLU=35.1 @ 2320 GL=4 GH=16.7 T=14.4K
3.74,15.1,-1.218 3.75,29.5,-.638 .02,0,-7.067

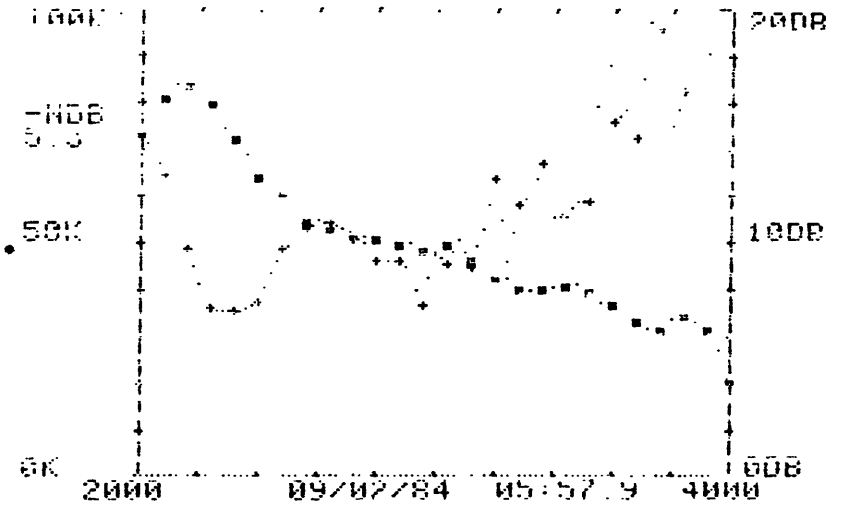


Fig. 14. Balanced amplifier at 14K.

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[5] Vectronics Microwave, Inc., Middlesex, NJ 08846, Model HC8009-3 quadrature 3 dB hybrid.

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[11] Indalloy solder #13, The Indium Corporation of America, Utica, NY 13502.