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LOW-NOISE, 8.0-8.8 GHz, COOLED, GASFET AMPLIFIER

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I. Introduction

This report covers the design and realization of a cryogenically cooled GaAs FET amplifier for the 8-8.8 GHz band. Commercially available transistors, the FSC10FA (Fujitsu) and MGF1412 (Mitsubishi), have been used for its construction. A minimum noise temperature of 20K at 8.4 GHz and an average noise temperature of 26K over 800 MHz bandwidth, as measured at the cold input of the amplifier, were obtained. The amplifier has a gain of 30 dB varying by no more than $\pm$ 2 dB over the 800 MHz bandwidth.

The design process involved the noise characterization of several transistors and computer-aided analysis and optimization techniques to achieve the amplifier performance close to the attainable limits for commercially available packaged transistors. Greater improvements in noise temperature can be expected only with the advent of the HEMT (high electron mobility) FET.

The study of the noise properties of commercial GaAs FET's is given in Section II of this report, together with the method of measurement employed. The signal and noise properties of Fujitsu FSC10FA transistor are discussed in detail. This transistor exhibited the lowest noise temperature of all measured transistors at this frequency.

Section III discusses the choice of circuit topology for the three-stage amplifier and CAD techniques used to optimize its performance. It also compares computer modeling results with experimental characteristics of a prototype amplifier. The emphasis was placed on low noise and flat gain response within the band specified. It resulted, as expected, in a large standing wave ratio at the amplifier input and warranted the use of the isolator.

Consequently, Section IV is devoted to the characterization of the cryogenic performance of several commercially available isolators. The noise model of a lossy isolator is also briefly discussed.

Finally, Section V describes the production version of 8.4 GHz amplifier, its design, construction, tuning and the experimental results for four amplifiers.

II. Comparative Study of Noise Parameters of Commercial GaAs FET's at 8.4 GHz

A. Introductory Remarks

The noise temperature T_n of any linear two-port can be written as [1]:

$$T_n = T_{min} + T_o \frac{g_n}{R_g} \left| Z_g - Z_{gopt} \right|^2 \qquad (1)$$

where:

$T_o = 290^\circ$ - standard temperature,

T_{min} - minimum noise temperature,

$Z_{gopt} = R_{gopt} + jX_{gopt}$ - optimum generator impedance, and

g_n - noise conductance.

Therefore, the complete description of the noise performance of any linear two-port is given by four real numbers*: T_{min}, R_{gopt}, X_{gopt}, g_n. The expression (1) can be rewritten in the following form:

$$T_n = T_{min} + NT_o \frac{\left| Z_g - Z_{gopt} \right|^2}{4R_g R_{gopt}} \qquad (2)$$

where $N = 4g_n R_{gopt}$.

*There are a number of other sets of noise parameters that will correctly describe noise performance of a linear two-port.

The significance of this form becomes apparent if it is observed that both T_{min} and the parameter N are invariant under transformation through lossless reciprocal two-ports connected to input and/or output of a noisy two-port [21]. Also for any physical two-port T_{min}, R_{opt}, and g_n must be non-negative and the following condition must be satisfied [2]:

$$T_{min} < NT_o \tag{3}$$

Expression (3) follows directly from the requirement that the correlation matrix for any reciprocal two-port be hermitian and non-negative definite. It provides fast and easy check of the validity of noise data. Unexpectedly large portions of published data does not satisfy this property, i.e., may not represent noise of any physical two-port (for instance: some data in [3], [4]). The explanation of this fact lies in measurement inaccuracies. It should be noted that the determination of all noise parameters requires at least four separate measurements for four different source impedances (for cryogenic data it takes four cool-downs). If adequate precautions are not taken with regard to bias, temperature, light, etc. conditions, each measurement could be done for a different two-port resulting in non-physical noise parameters.

B. Single Stage Amplifier as a Measurement Mount

The determination of noise parameters of GaAs FET's in this work was done by noise temperature measurement of a single stage amplifier of a similar design to that previously reported [3], [5]. The simplified schematic of the amplifier, its photograph and full equivalent circuit are shown in Figures 1, 2 and 3, respectively. The noise performance of this amplifier followed by an isolator was measured at both room and cryogenic temperatures. The schematic of a measurement setup is shown in Figure 4.

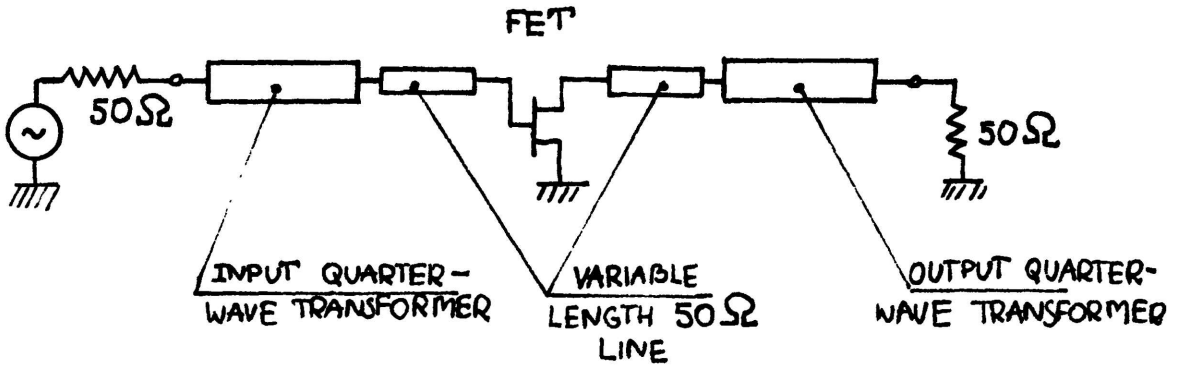


Fig. 1. Simplified schematic of the 8.4 GHz single stage amplifier.

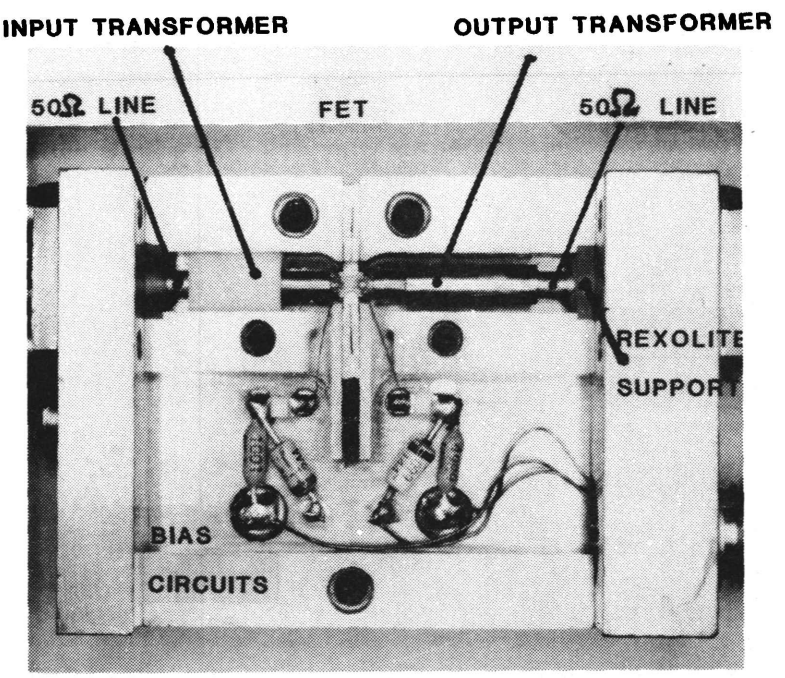
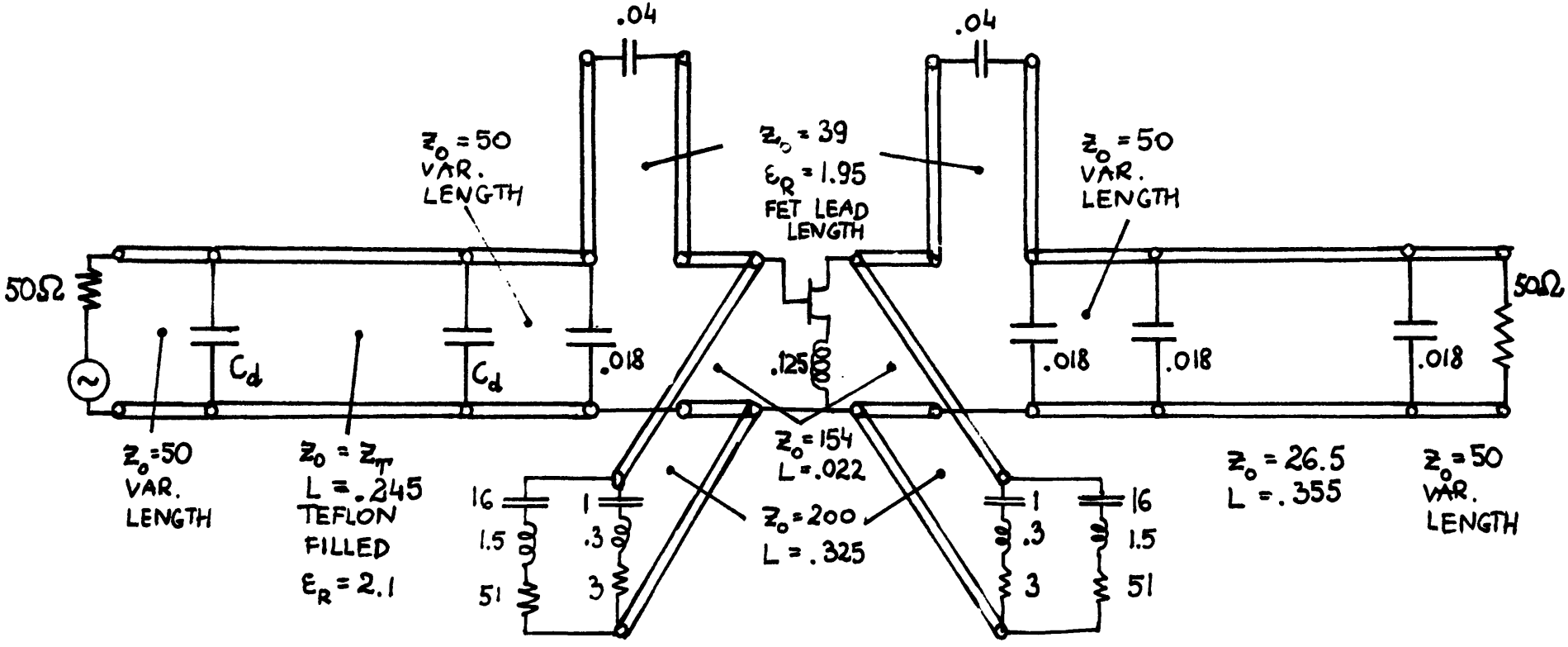


Fig. 2. Photograph of the 8.4 GHz single-stage amplifier with cover plate removed.



Z_T	C_d
9.2	.054
12.4	.037
18.3	.018
24.7	.007

VALUES IN INCHES, pF, nH and Ω.

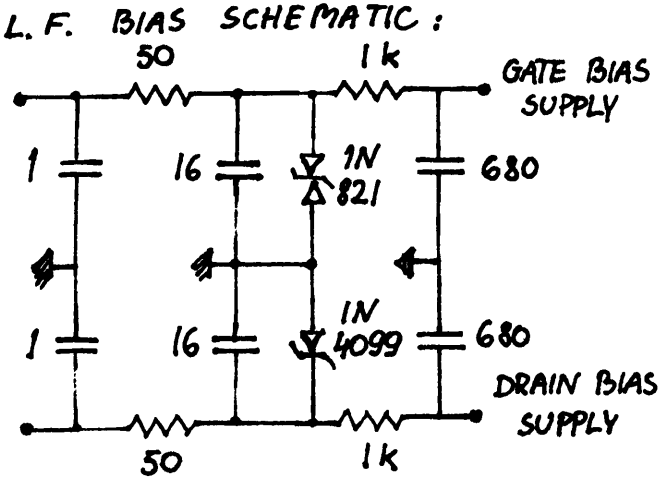


Fig. 3. Detailed equivalent circuit of the 8.4 GHz single stage amplifier.

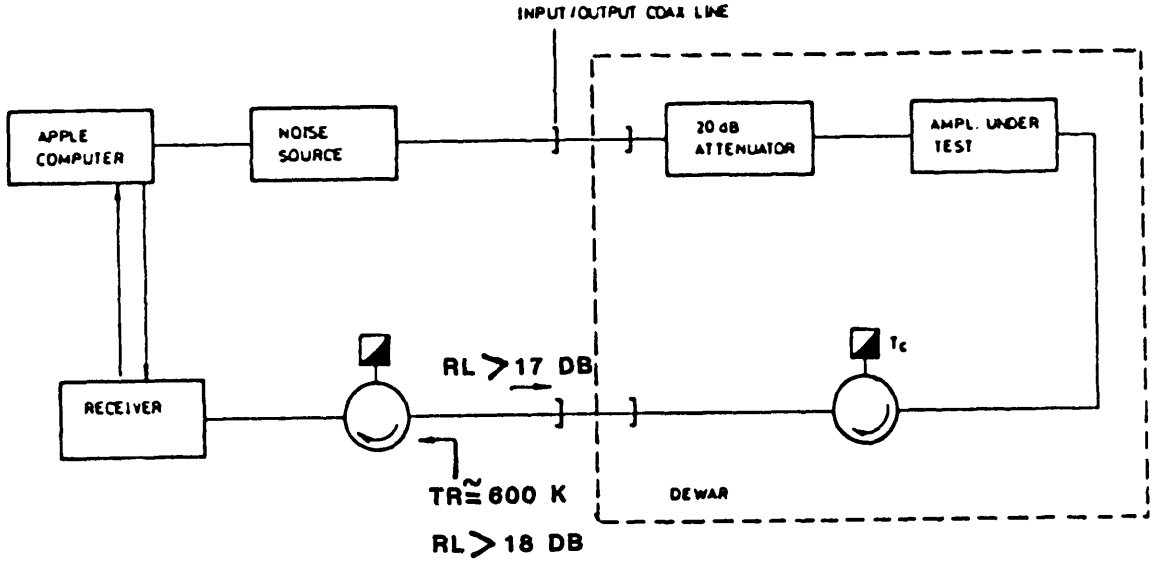


Fig. 4. Test setup for measurement of cryogenically-cooled amplifier.

The quarter-wave transformers are realized as movable slugs on a 50Ω transmission line. Therefore, for a given characteristic impedance of the input transformer, its position could be varied to minimize the noise temperature of the amplifier at the frequency of 8.4 GHz. For this network and the reference plane located at the transistor gate (Fig. 3), the imaginary part of source impedance X_g varies much faster with frequency than the real part R_g. Consequently, it can be assumed that the minimum in noise temperature vs. frequency occurs for $X_g = X_{gopt}$. In this case, expression (1) can be reduced to:

$$T_n = T_{min} + T_o \frac{g_n}{R_g} \left(R_g - R_{gopt} \right)^2 \qquad (4)$$

The knowledge of the equivalent network of the input circuit allows the determination of X_{gopt} and also R_g for a given characteristic impedance of the input transformer. Therefore, three measurements of noise temperature done for three different characteristic impedances of the transformers would suffice to determine remaining three noise parameters, R_{gopt}, T_{min} and g_n.

For reasons of accuracy, the measurements were performed for four different transformers, from which T_{min}, R_{gopt}, and g_n were determined to produce the "best fit" to experimental data. The novel "fitting" procedure and discussion of the accuracy of measurement is given in Section II.E.

The reference plane for determining the generator impedance was chosen to be at the plane of connection of the bias circuit (see Fig. 3). Therefore, the noise parameters, measured in this way, are those of a cascade connection of the gate bias network, FET (with source inductance), drain bias network, output matching network and isolator. This data can be deembedded to produce the noise data of the packaged FET, if the signal parameters of the transistor, isolator, bias and output circuits are known. The noise data of the chip can

also be determined if the equivalent circuit of the transistor package is known. Both operations can be done easily with the help of FARANT subprograms LSTRIP, RSTRIP, FLIP and FLOP [6].

C. Noise Parameters of FSC10FA, MGF1412 and NE67383 Transistors

The noise parameters of packaged FSC10FA, MGF1412 and NEC673 were measured using the method described in the preceding section at both room and cryogenic temperatures and at the frequency of f = 8.4 GHz. The measured values of noise temperatures for different operating bias and different values of generator resistance R_g together with computer "fitted" curves are shown in Figures 5, 6 and 7 for FSC10FA, MGF1412 and NE 67383 transistors, respectively. The values of noise parameters resulting from the least square error "fit" of measured data to theoretical curve are summarized in Tables I and II. The "fitting" procedure and errors involved are discussed in Section II.E. The measured results for different operating bias are summarized in Tables I and II. The noise parameters are those of the packaged transistor with bias circuits followed by the output matching network and isolator, as described in Section II.B. The deembedding of the transistor noise parameters was done only for the FSC10FA transistor biased at V_{ds} = 3 V, I_{ds} = 10 mA (compare Section II.D.) This procedure changed the measured noise parameters by the amounts comparable to measurement errors and much smaller than variations of noise parameters for several samples of transistors of the same type. Therefore, it was felt that deembedding of noise parameters for other transistors need not be done, especially for the purpose of comparison as all were measured in the same mount.

Table III and Table IV give the lowest noise temperatures with associated gain, source impedance and bias conditions observed for sample transistors at room and cryogenic temperatures, respectively.

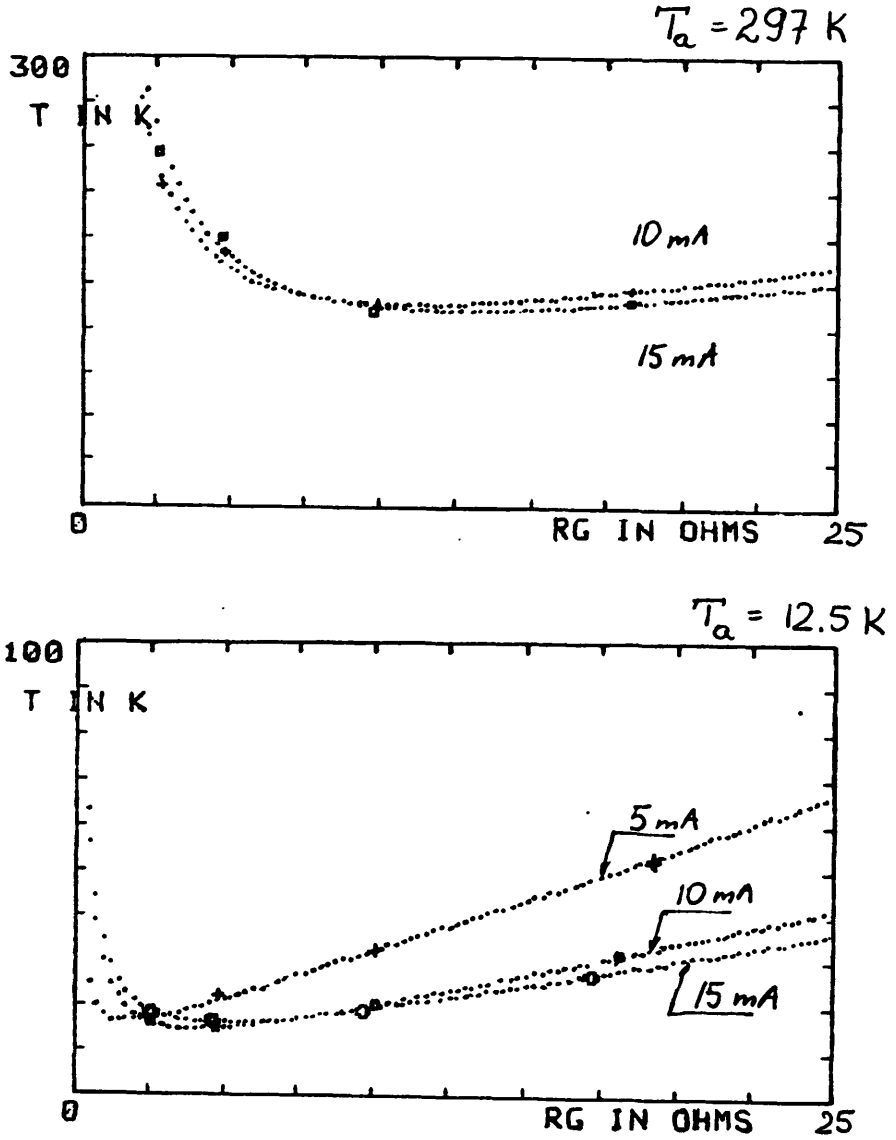


Fig. 5. Noise temperature vs. source resistance for FSC10FA. (Crosses and squares indicate measured data at f = 8.4 GHz.)

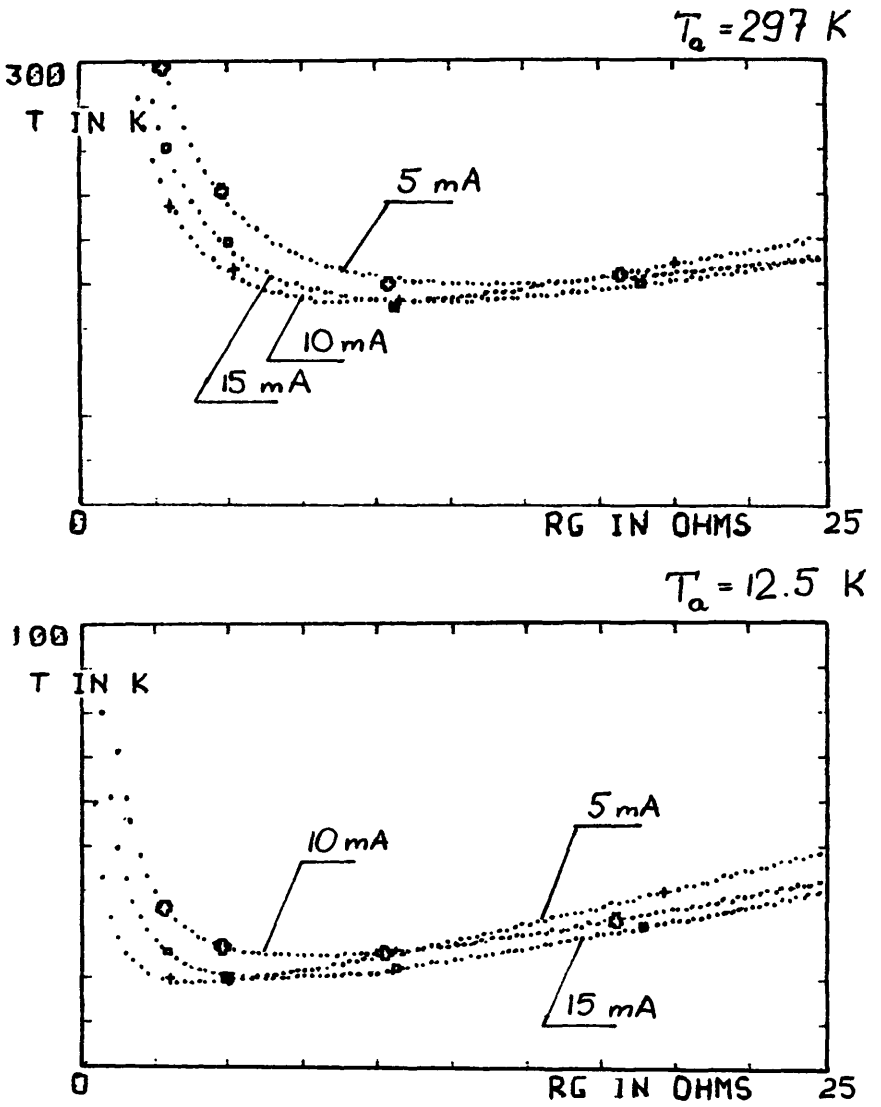


Fig. 6. Noise temperature vs. source resistance for MGF1412. (Crosses and squares indicate measured data at f = 8.4 GHz.)

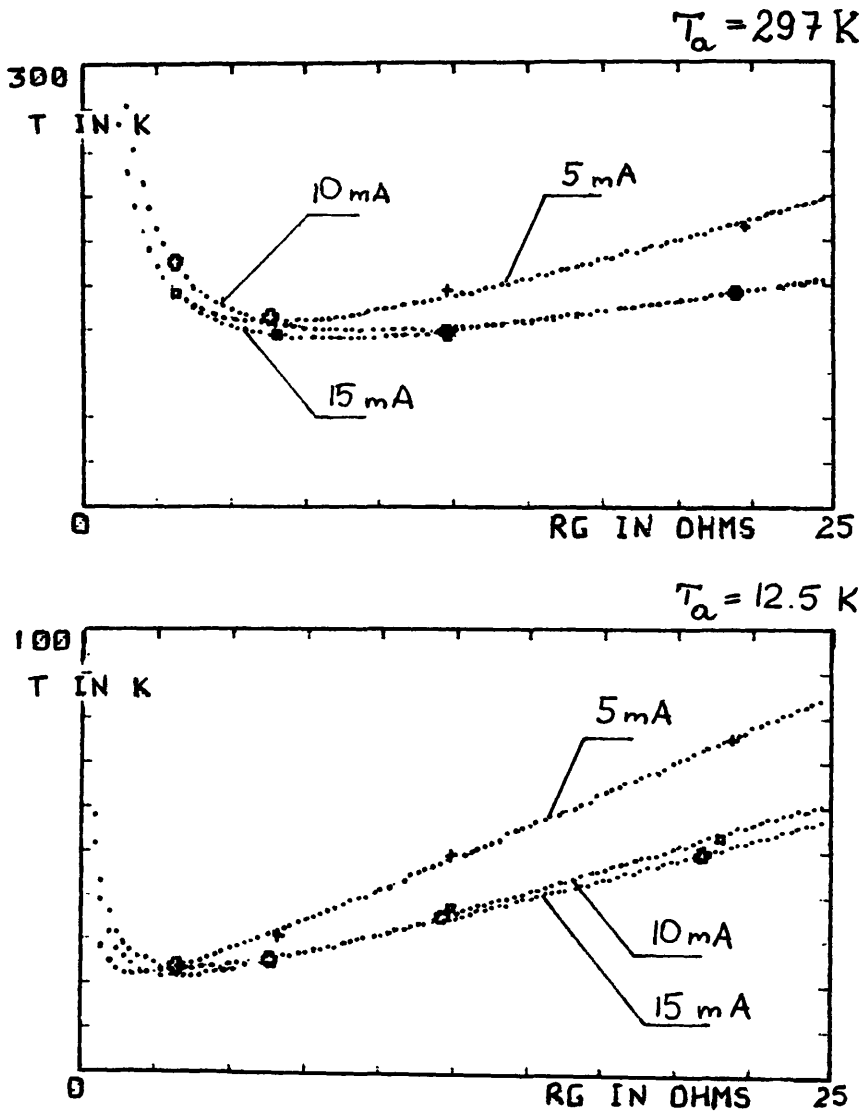


Fig. 7. Noise temperature vs. source resistance for NE 67383. (Crosses and squares indicate measurement data at f = 8.4 GHz.)

TABLE I. Noise Parameters of Sample of NE67383, MGF1412 and FSC10FA at T_a = 297K, f = 8.4 GHz.

FET	V_{ds}	I_{ds}	T_{min}	R_{gopt}	X_{gopt}	g_n
	V	mA	K	Ω	Ω	℧
NE 67383	3.5	5	124	6.5	37	.021
	3.0	10	113	8.3	35	.013
	2.5	15	116	9.5	34	.014
MGF 1412	4.5	5	136	9.7	36	.016
	4.0	10	137	11.7	32.5	.014
	3.5	15	149	13.7	31	.012
FSC 10FA	2.5	10	135	11.1	29	.011
	2.0	15	131	12.5	28	.010

TABLE II. Noise Parameters of Sample of NE67383, MGF1412 and FSC10FA at T_a = 12.5K, f = 8.4 GHz.

FET	V_{ds}	I_{ds}	T_{min}	R_{gopt}	X_{gopt}	g_n
	V	mA	K	Ω	Ω	℧
NE 67383	3.5	5	22	1.9	38	.010
	3.0	10	22	3.2	36	.0071
	2.5	15	23	3.6	35	.0063
MGF 1412	4.5	5	19	4.0	34.5	.0058
	4.0	10	20	6.4	32.5	.0049
	3.5	15	25	7.6	30.5	.0050
FSC 10FA	3.0	5	16	1.8	29	.0080
	2.5	10	14	4.1	28	.0053
	2.0	15	16	4.9	26	.0043

TABLE III. Best Observed Noise Performance of NE67383, MGF1412 and FSC10FA at T_a = 297K, f = 8.4 GHz.

FET	V_{ds}	I_{ds}	T_n	R_g	X_g	ASS. GAIN
	V	mA	K	Ω	Ω	DB
NE 67383	3.0	10	113	8	35	9.6
MGF 1412	4.2	8	129	10	34	8.9
FSC 10FA	3.3	12	130	12	29	7.5

TABLE IV. Best Observed Noise Performance of NE67383, MGF1412 and FSC10FA at T_a = 12.5K, f = 8.4 GHz.

FET	V_{ds}	I_{ds}	T_n	R_g	X_g	ASS. GAIN
	V	mA	K	Ω	Ω	DB
NE 67383	4	10	21.9	2	36	11.3
MGF 1412	4.4	6	18.4	4	34	10.3
FSC 10FA	2.5	10	14.2	4	28	8.9

TABLE V. Minimum Noise Temperature Observed at T_a = 12.5K and f = 8.4 GHz for Five of MGF1412 Transistors.

MGF 1412

FET	No	1	2	3	4	5
	BATCH	33H8	33H8	33H8	2ZG8	2ZG8
T_n	K	18.4	23.1	26.3	19.8	22.1
I_{ds}	mA	6	5	5	5	9
V_{ds}	V	4.4	4.0	5.0	4.0	4.0

TABLE VI. Minimum Noise Temperature Observed at T_a = 12.5K and f = 8.4 GHz for Five of FSC10FA Transistors.

FSC 10FA

FET	No	1	2	3	4	5
	BATCH	PS01	PT01	PT01	PT03	PT03
T_n	K	14.2	21.5	20.7	18.5	18.2
I_{ds}	mA	10	9	8	12.5	12.5
V_{ds}	V	2.5	2.0	2.5	2.5	2.5

The data included in Tables I through IV suggest the choice of the FSC10FA or MGF1412 transistor for input stage at the frequency of 8.4 GHz. To evaluate the consistency of the noise performance from sample to sample, five of each FSC10FA and MGF1412 were tested for their lowest noise temperature at 12.5K. The results are summarized in Table V and Table VI. For the FSC10FA transistors these results indicate the repeatability of the noise temperature for transistors within the same batch, but show large variations from batch to batch. For MGF1412 transistors large variations in noise temperature were observed even among transistors from the same batch.

The data given in this chapter lead to the conclusion that at the present time FSC10FA transistors should be chosen for the first and second stage of a three-stage amplifier. Therefore, the signal and noise properties of this transistor are discussed in detail in Section II.D.

D. Noise and Signal Parameters of FSC10FA Transistor

The analysis of the noise and signal parameters of FSC10FA transistor was done at the bias conditions: V_{ds} = 3 V, I_{ds} = 10 mA. The S-parameter data, as published by the manufacturer [7], are listed in Table VII.A. These data were used to determine the elements of an equivalent circuit of topology given in Figure 8, using the optimization procedure which minimizes the function:

$$F = \frac{1}{48} \sum_{n=1}^{12} \sum_{i=1}^{2} \sum_{k=1}^{2} \left| \frac{S^m_{ikn} - S^c_{ikn}}{S^m_{ikn}} \right|^2 \qquad (5)$$

where

S^m_{ikn} - i,k element of S-matrix measured at frequency of n GHz, and

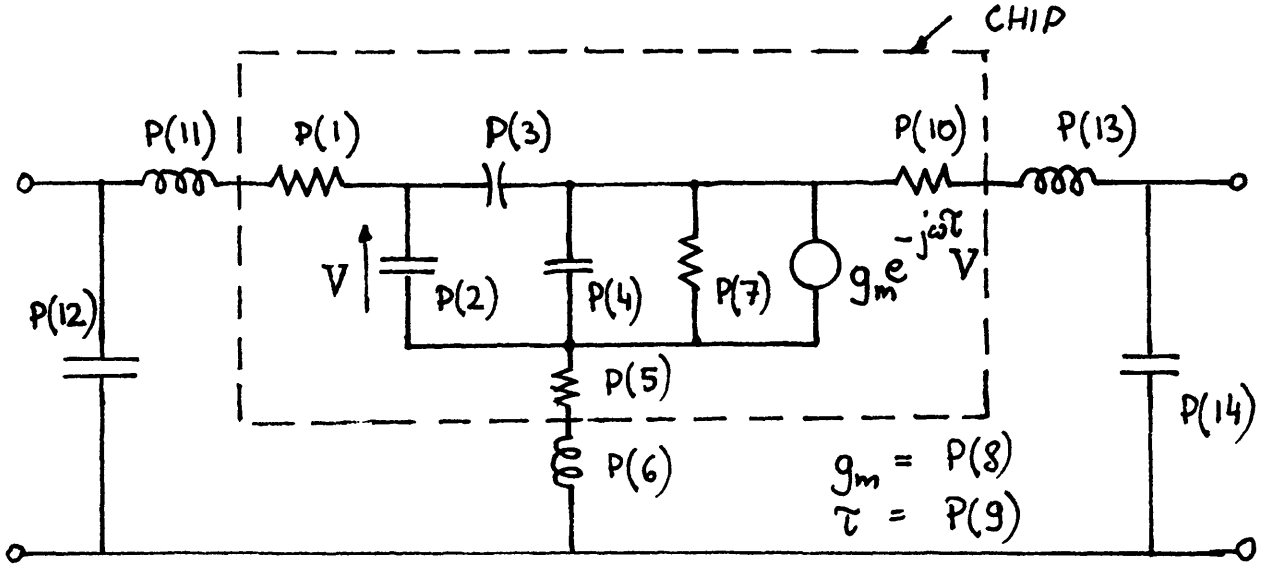
S^c_{ikn} - i,k element of S-matrix computed from the equivalent circuit of Figure 7 at frequency of n GHz.

This optimization was done using "FARANT" program and associated subprograms described in [6]. In the process of optimization, all elements of equivalent circuit of Figure 8 were allowed to vary with the exception of package capacitances P(12) and P(16), whose values are well established.

The resulting values of the equivalent circuit parameters are listed in Figure 8, and measured and computed values of S-parameters are compared in Figure 9 and Table VII. The agreement is considered to be fair; the function F, as defined by (5), has a minimum value of .05. Most of the elements of equivalent circuit assume values justified by the transistor structure. The exceptions are delay time τ (P(9)) and drain parasitic resistance P(10), which values are equal to zero as a result of optimization. This certainly suggests an inadequacy of the equivalent circuit employed. However, no effort has been made to resolve it, as the agreement between the measured S-parameters and those predicted by the model is quite good for the frequency range of interest between 8 and 11 GHz.

The circuit model of the FSC10FA FET was used to predict the performance of a single stage amplifier. An example of the computed and experimental results for the amplifier at the ambient temperature of T_a = 297K is shown in Figure 10. The agreement was found to be satisfactory and no effort was made to improve the accuracy of the FET model.

The noise parameters measured at 8.4 GHz and the circuit models of the transistor and amplifier were used to predict the noise performance vs. frequency for the single stage amplifier. First, the measured noise data of Section II.C. were corrected for the noise contribution from the bias circuits and the isolator



P(1)	P(2)	P(3)	P(4)	P(5)	P(6)	P(7)	P(8)	P(9)	P(10)	P(11)	P(12)	P(13)	P(14)
6.3	.22	.039	.18	1.2	.10	157	30	0	0	.83	.26	.69	.26
Ω	pF	pF	pF	Ω	nH	Ω	mS	ps	Ω	nH	pF	nH	pF

Fig. 8. The topology of equivalent circuit of FET and parameters of equivalent circuit for FSC10FA transistor biased at V_{ds} = 3 V, I_{ds} = 10 mA as determined by the optimization procedure.

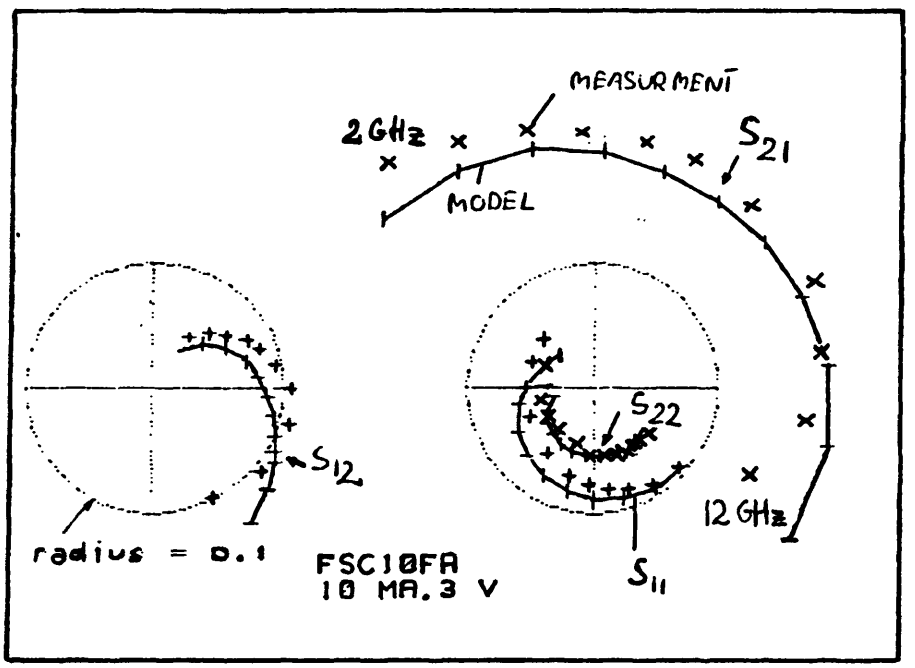


Fig. 9. Comparison between S-parameters measured by the manufacturer (crosses) and computed from the model.

TABLE VII. FSC10FA S-Parameters as a Function of Frequency: A - published by the manufacturer, and B - computed from the model of Fig. 8.

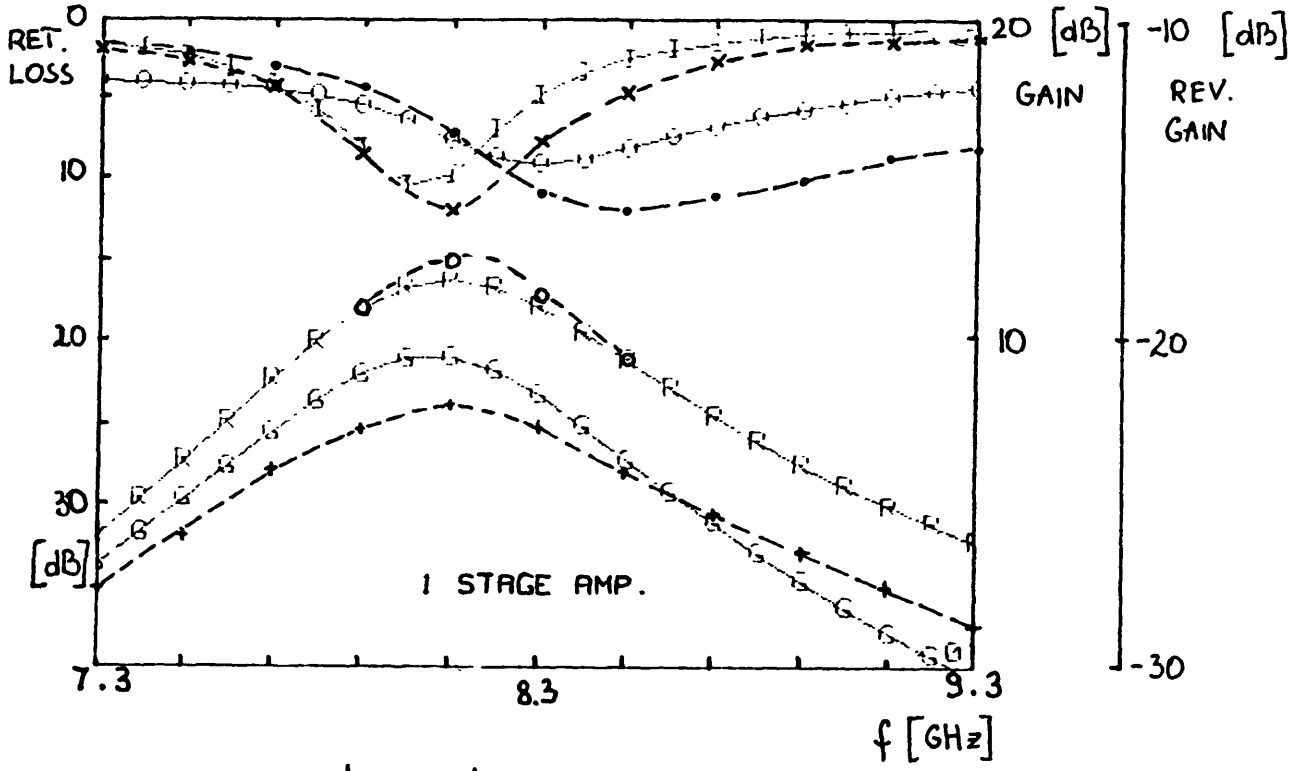
FSC10FA FSC11FA S-PARAMETERS
V_{DS} = 3V I_{DS} = 10mA

A. MANUFACTURER'S DATA:

FREQ (MHz)	S11		S12		S21		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2000	.941	-43	.049	55	2.432	132	.588	-39
3000	.915	-58	.061	45	2.246	119	.575	-48
4000	.863	-71	.070	37	2.120	105	.577	-58
5000	.824	-81	.081	29	2.042	93	.575	-70
6000	.778	-92	.087	21	2.004	78	.556	-80
7000	.732	-104	.096	12	1.989	66	.536	-90
8000	.640	-124	.106	0	1.931	49	.470	-105
9000	.556	-154	.108	-16	1.939	26	.431	-129
10000	.516	-179	.107	-29	1.849	9	.425	-146
11000	.516	156	.107	-39	1.719	-9	.412	-168
12000	.556	135	.100	-62	1.440	-29	.418	158

B. MODEL:

FREQ. (MHZ)	S11		S12		S21		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2 000	.9768	-39.1	.0368	57.9	2.1385	140.7	.5362	-37.7
3 000	.9519	-57.2	.0518	43.2	2.0511	122.2	.5402	-54.7
4 000	.9222	-74.1	.0640	29.7	1.9595	104.6	.5439	-70.0
5 000	.8890	-89.8	.0737	17.3	1.8791	88.0	.5455	-83.9
6 000	.8519	-104.6	.0816	6.1	1.8198	72.0	.5435	-96.5
7 000	.8088	-119.0	.0885	-4.3	1.7876	56.2	.5360	-108.1
8 000	.7563	-133.7	.0951	-14.0	1.7854	40.3	.5208	-119.2
9 000	.6891	-149.5	.1021	-23.4	1.8131	23.6	.4955	-130.2
10 000	.6013	-167.8	.1103	-32.9	1.8659	5.6	.4567	-141.6
11 000	.4895	168.8	.1204	-43.2	1.9292	-14.5	.3996	-154.5
12 000	.3667	133.8	.1322	-55.1	1.9722	-37.2	.3172	-170.8



		MEAS.	COMP.
INP.	RET. LOSS	×	I
OUT.	RET. LOSS	•	O
TRANS.	GAIN	+	G
REV.	GAIN	o	R

Fig. 10. Computer generated and measured results for a single stage amplifier (Fig. 2) with equivalent circuit as shown in Fig. 3. (Characteristic impedance of input transformer is Z_T = 12.4 Ω.)

using the equivalent circuit of the amplifier as shown in Figure 3 and the isolator equivalent circuit given in Section IV of this report. Then the noise parameters at 8.4 GHz of the transistor chip were determined using the equivalent circuit of the transistor package (Figure 8). The results of this procedure for the FSC10FA transistor at room temperature are summarized in Table VIII. The dependence of the noise parameters of the chip on frequency, as predicted by Pucel et al. [8], was assumed to compute the noise performance of the amplifier. The comparison between measured and computed results for the amplifier followed by the isolator is given in Figure 11.

The agreement between measured noise temperature and that determined from the model was found to be very good for frequencies below 8.7 GHz. For higher frequencies, the measured curve exhibits a much smaller frequency dependence than the computer generated curve. As the same property is observed for the gain and output return loss of the amplifier, it points out to some inadequacy in FET and/or amplifier model. This problem has not been investigated further.

For cryogenic temperatures, no S-parameter data are available. In fact, the measurement of S-parameters at cryogenic temperatures is much more difficult than measurement of noise parameters. Brookes' work [9] indicates, however, that these elements of the equivalent circuit, which can be measured by a DC method, undergo only slight change with temperature down to 20K. Therefore, for the deembedding of cryogenic noise data for FSC10FA FET and for the modeling of the single stage amplifier, the room temperature equivalent circuit was used. The results of deembedding procedure are summarized in Table IX. The measured and computed performance of the single stage amplifier (with isolator) at T_a = 12.5K is shown in Figure 12. The agreement was found to be good at the band center, but quite poor at the band edges. The discrepancy could be explained

TABLE VIII. Noise Parameters of FSC10FA at V_{ds} = 3 V, I_{ds} = 10 mA, T_a = 297K, and f = 8.4 GHz at Different Stages of Deembedding.

	T_{min} K	R_{gopt} Ω	X_{gopt} Ω	g_n ℧
FET WITH EXTER. SOURCE INDUCTANCE BIAS CIRCUITS OUTPUT NETWORK, ISOLATOR.	135	11.1	29	.011
FET WITH EXTERNAL SOURCE INDUCTANCE.	126	9.8	29	.012
PACKAGED FET	111	8.9	35	.012
FET CHIP	111	30	109	.0035

TABLE IX. Noise Parameters of FSC10FA at V_{ds} = 3 V, I_{ds} = 10 mA, T_a = 12.5K and f = 8.4 GHz at Different Stages of Deembedding. (Note that room temperature S-parameters were used.)

	T_{min} K	R_{gopt} Ω	X_{gopt} Ω	g_n ℧
FET WITH EXTER. SOURCE INDUCTANCE BIAS CIRCUITS OUTPUT NETWORK, ISOLATOR.	14.2	4.1	28	.0053
FET WITH EXTERNAL SOURCE INDUCTANCE.	13.2	3.7	27	.0055
PACKAGED FET	10.2	3.7	33	.0055
FET CHIP	9.8	12.4	107	.0017

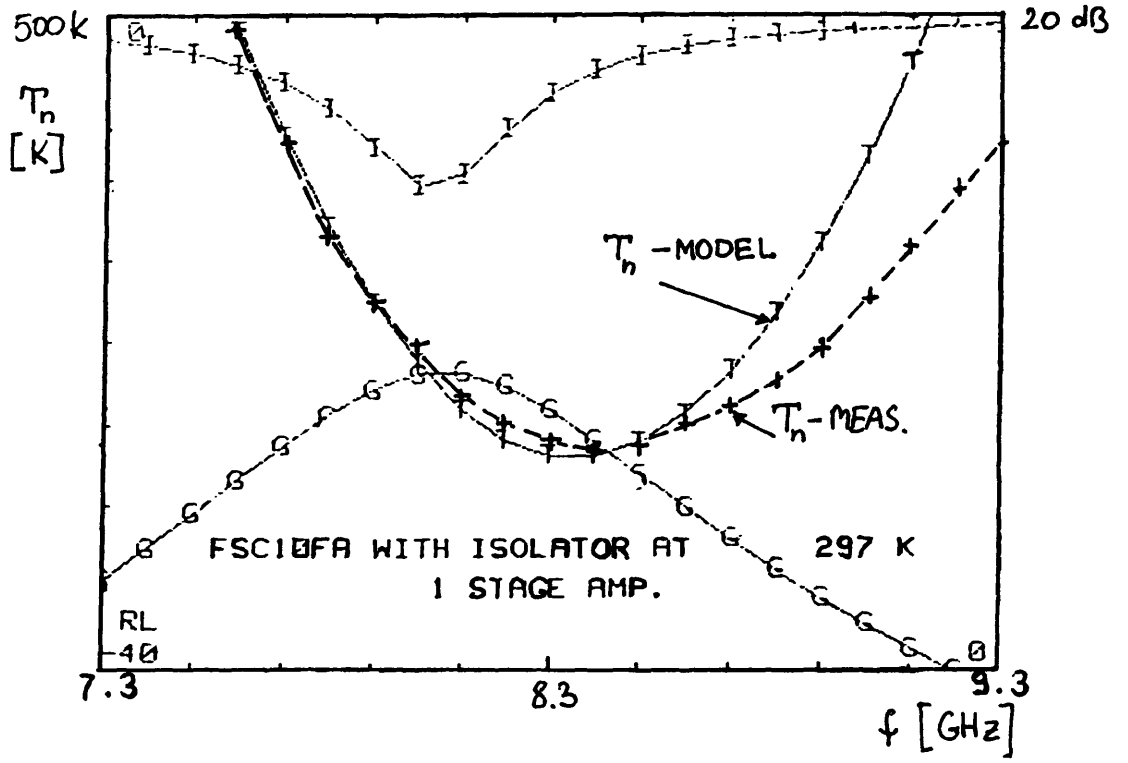


Fig. 11. Noise temperature of a single stage FSC10FA amplifier with isolator at room temperature computed from the model and measured (characteristic impedance of input transformer is Z_T = 12.4 Ω).

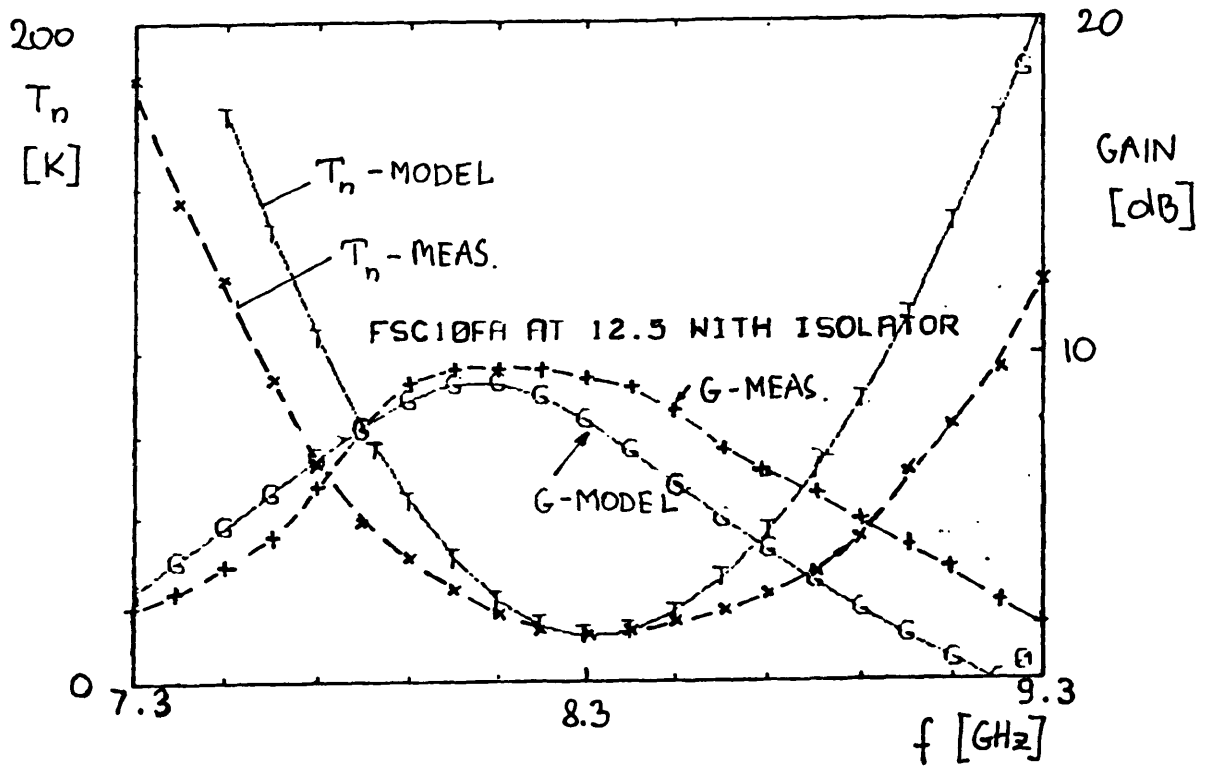


Fig. 12. Noise temperature and gain of a single stage FSC10FA amplifier with isolator at 12.5K computed from the model and measured (characteristic impedance of input transformer is Z_T = 12.4 Ω).

by two factors: a possible error in determining the noise conductance g_n, and/or inadequate transistor model at cryogenic temperature. No effort has been made to investigate this problem further.

In the frequency range of interest, 8.0 through 8.8 GHz, the measurement results and those computed from the model agree quite well. It was felt, therefore, that the use of room temperature model of FSC10FA FET together with cryogenic noise data is justified for use in the computer-aided design of a three-stage amplifier for cryogenic applications.

In conclusion of this section, it should be noted that the DC characteristic of FSC10FA transistor at cryogenic temperatures exhibits an unusual property. This is demonstrated in Figure 13, which gives the drain current vs. gate voltage characteristics for two values of source-to-drain voltage at both room and cryogenic temperatures. These characteristics indicate that the channel at cryogenic temperatures may not be pinched off. It is caused by "soft breakdown" between gate and drain or source. The occurrence of this "breakdown" has not been observed to lead to a failure of any of the devices tested. No explanation has been found for this effect, which has not been observed in either MGF1412 or NEC673 transistors in this range of drain-to-gate voltages.

E. Comments on Measurement Errors of Noise Parameters

The error in the determination of the noise parameters of a microwave FET by the method employed in this work is related to:

- the error in determining the noise parameters of an "embedded" transistor, i.e., of a two-port composed of a FET with source inductance, bias circuit, output matching circuit and isolator;
- the error caused by a deembedding procedure.

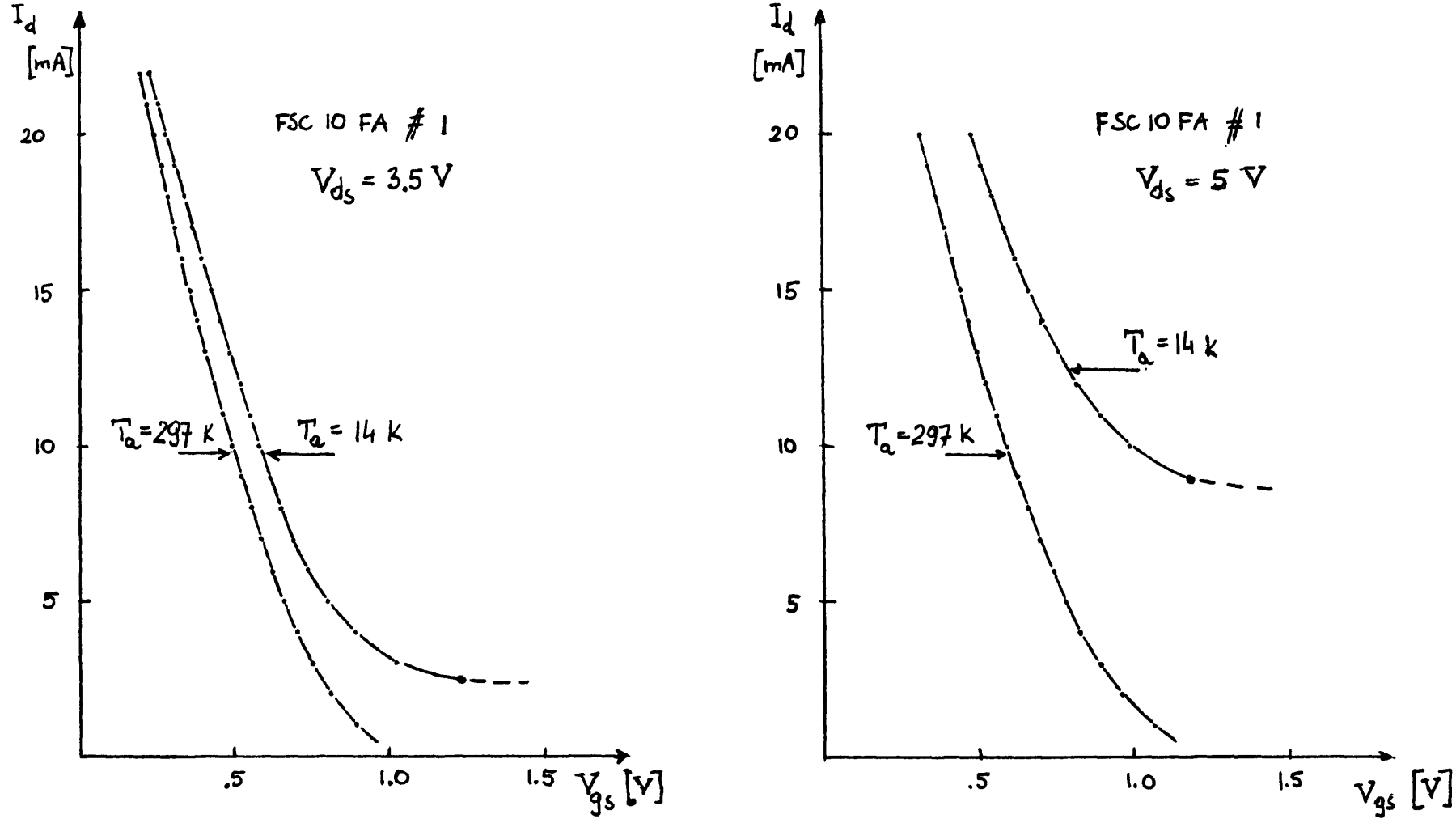


Fig. 13. Drain current I_{ds} as a function of gate voltage V_{sg} for FSC10FA transistor at room and cryogenic temperatures.

The latter error is dependent only on the accuracy with which the equivalent circuits and/or noise models of a bias network, output matching network, isolator and S-parameters of the transistor are known. An accurate determination of these models is not an easy task, as demonstrated in Section II.D. of this report. However, as is shown in Section II.D., the changes in noise parameters resulting from the deembedding procedure need not be large for a properly designed amplifier and should not exceed the error in determination of noise parameters of an "embedded" transistor. This is especially true at cryogenic temperatures where thermal noise contributions from the bias circuits and isolator are small. Therefore, this section deals only with the error in the determination of the noise parameters of an "embedded" transistor.

The accuracy with which the noise parameters of a two-port can be determined is dependent on:

- the accuracy of noise temperature measurement;
- the accuracy with which the source impedance for a given noise temperature measurement is known;
- the number of measurements;
- the procedure used to "fit" the measured points to theoretical curve $T_n = f(R_g)$.

If the number of measurement is greater than the number of parameters to be determined, the influence of random errors may be reduced by a proper "fitting" procedure of theoretical curve to measurement points. A number of computational methods have been proposed for the general case of four noise parameters [2], [13], [14], [15] or the simplified case of three noise parameters [3]. These procedures seek the values of the noise parameters for which there is a minimum of an error function defined on the sets of measured values of

noise temperature (or noise figure) and those predicted from theory. The definition of an error function and the choice of a set of noise parameters with respect to which this function is minimized differs from reference to reference. None of the published methods, however, takes into account that the correlation matrix of the resulting equivalent noise sources has to be non-negative definite [22]. The same, in simpler terms, means that the magnitude of the correlation coefficient has to be less than one, or that inequality (3) has to be satisfied. As a result, the minimum of an error function sometimes occurs for a set of noise parameters that may not represent the noise of any physical two-port (for instance [3], [4], [13]).

In the method used in this work, the optimum generator reactance is determined by the tuning procedure, independently of the remaining three noise parameters. The other noise parameters are then determined from four measurements. It can be shown that the minimization of mean square error defined as:

$$E = \sqrt{\sum_{i=1}^{N} \left(T_{ni}^{m} - T_{ni}^{c} \right)^2} \qquad (6)$$

can be done only with respect to one noise parameter, namely the optimum generator resistance.

The accuracy of the noise temperature measurements for the measurement setup as that shown in Figure 4 is analyzed in [3]. It has been determined that the error in the T_n measurement performed in this work should not exceed $\pm$ 2K for cryogenic temperature and $\pm$ 7K for room temperature.

The accuracy with which the optimum generator reactance can be found is primarily dependent on the accuracy with which the equivalent circuit of the input network is known (compare Figure 3).

Very accurate data for the characteristic impedance of a square-slab line are available [10]. The values of the discontinuity capacitances can be estimated from those for a coaxial line [11]. The least known parameters are those of the reentrant line, which is composed of a transistor gate lead covered with teflon tubing placed inside the inner conductor of the square-slab line. The characteristic impedance, effective dielectric constant and open end capacitance of this line were estimated from the low-frequency capacitance measurement [12]. It has been estimated that the error in the determination of the optimum source reactance X_{gopt} from the network as shown in Figures 2 and 3 does not exceed $\pm 3\ \Omega$.

If X_{gopt} is known, the dependence of noise temperature on T_{min}, R_{gopt} and g_n is given by equation (4). This expression can be rewritten in the following form:

$$\frac{T_n}{T_o} = \left(\frac{T_{min}}{T_o} - 2g_n R_{gopt} \right) + g_n R_{gopt} \left(\frac{R_g}{R_{gopt}} + \frac{R_{gopt}}{R_g} \right) \tag{7}$$

It should be noted that a new set of variables can be chosen: $y = \frac{T_n}{T_o}$, $x = \frac{R_g}{R_{gopt}} + \frac{R_{gopt}}{R_g} \geq 2$. Then equation (7) describes a straight line

$$y = a + bx \tag{8}$$

where

$$a = \frac{T_{min}}{T_o} - 2g_n R_{gopt}$$

$$b = g_n R_{gopt} \tag{9}$$

The coefficients a and b are invariant under any losses transformation at the input or output; consequently, equation (7) does not depend on the choice of reference plane for determination of generator resistance R_g. This plane should therefore be chosen with regard to most accurate determination of R_g. Then the "fitting" algorithm for a number of measurement $N > 3$ can be reduced to finding the R_{gopt} for which the measured values of noise temperature T_{ni} for generator resistances R_{gi} give the best fit the straight line. This was the procedure used to find noise parameters R_{gopt}, T_{min}, and g_n presented in the preceding sections from the set of four measurements of noise temperature for four values of source resistance.

An example of the experimental data for the FSC10FA transistor biased at V_{ds} = 2.5 V, I_{ds} = 10 mA and "best fitted" line, given by equation (7), are shown in Figure 14. Equation (3) allows one to assess easily the accuracy of the resulting noise parameters. By assuming that the source resistance R_{gopt} is different from that which minimized the error function E (eq. (6)) and finding a and b of equation (8) by linear regression, one can plot the error E, T_{min}, and g_n as a function of R_{gopt}. This analysis, done for the transistor data of Figure 14, is shown in Figure 15. The "forbidden region" is also shown, i.e., the region in which inequality (3) is not satisfied. It is clear, that although the minimum in error function E of .18K is sharp, the error function value is within the limits of estimated accuracy of measurement (< 2.1K) for all R_{gopt} from within this range (2.5 ÷ 5 Ω). It means that with less accurate data the minimum of E function could be anywhere in this region, which includes also "forbidden region." An example of experimental data which illustrates this point is shown in Figure 16 for the same transistor, FSC10FA #1, biased at V_{ds} = 3.0 V, I_{ds} = 5 mA. For this case, due to the larger measurement errors,

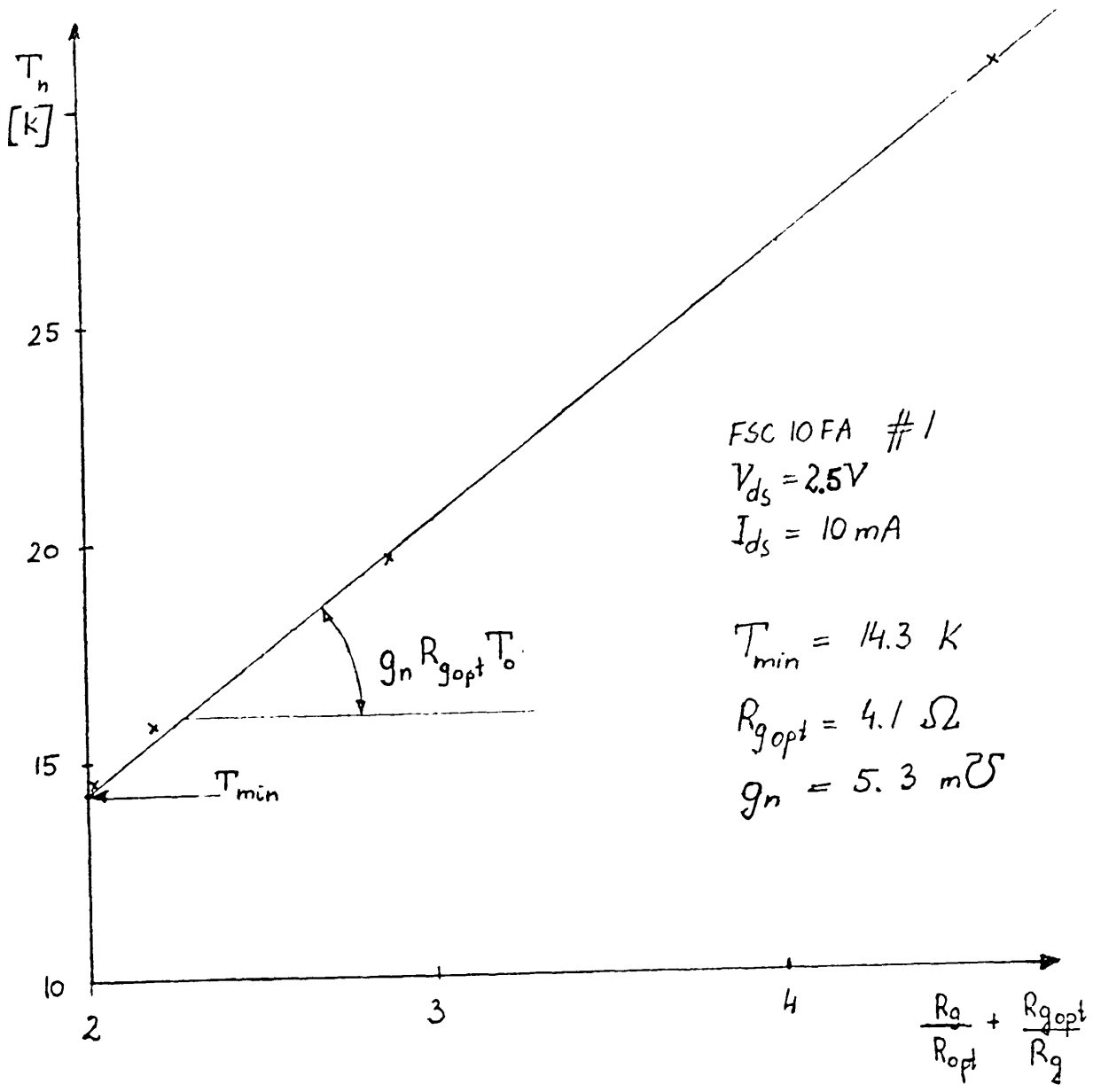


Fig. 14. The noise temperature T_n as a function of new variable $\frac{R_g}{R_{gopt}} + \frac{R_{gopt}}{R_g}$ best "fitted" to four experimental points (crosses) for transistor FSC10FA #1 at V_{ds} = 2.5 V, I_{ds} = 10 mA, T_a = 12.5K, f = 8.4 GHz.

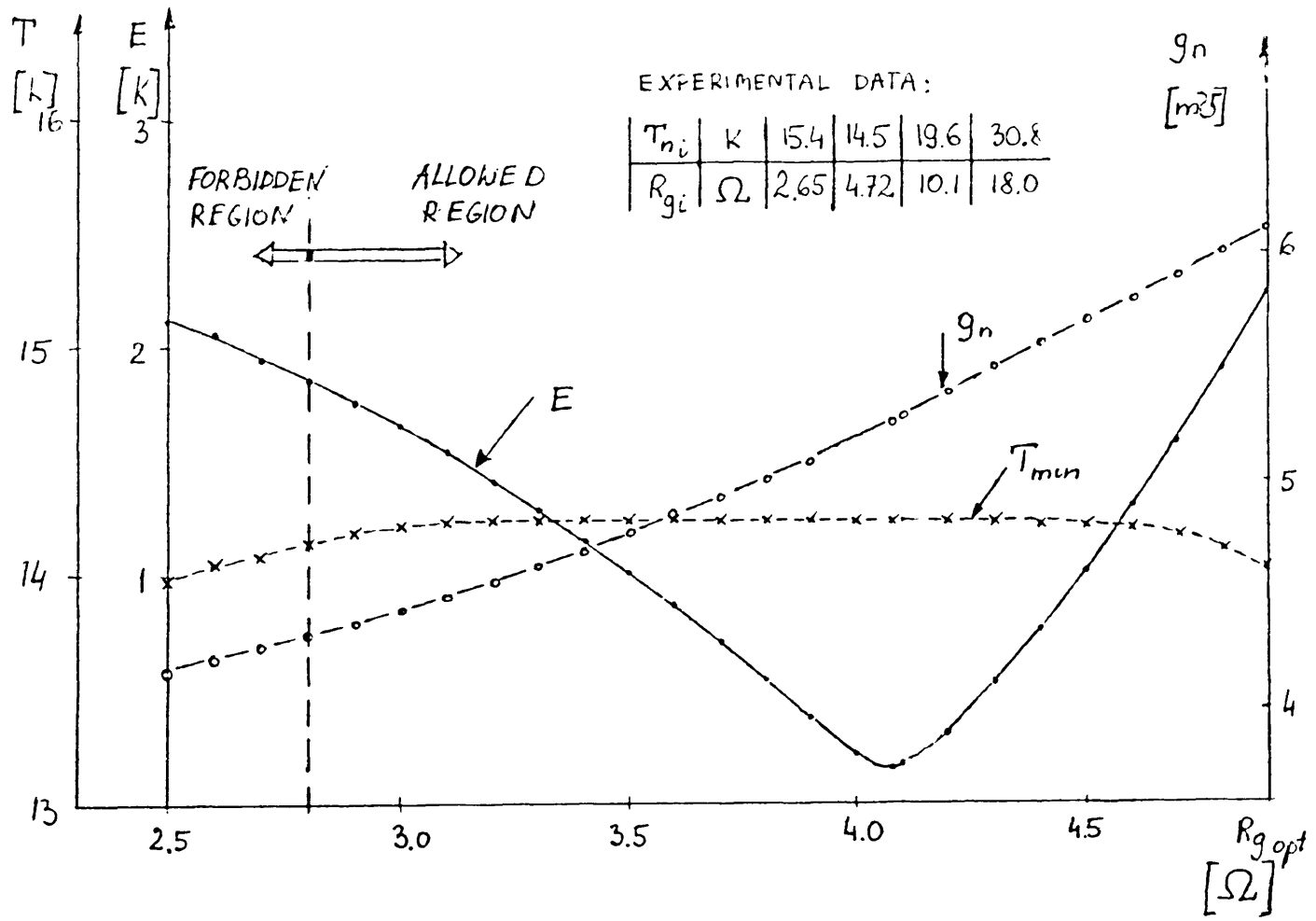


Fig. 15. The error function E, minimum noise temperature T_{min} and noise conductance g_n found by linear regression using equation (8) versus assumed value of the optimum source resistance R_{gopt}. The experimental data used are given in the table and are for FSC10FA #1 transistor at V_{ds} = 2.5 V, I_{ds} = 10 mA, T_a = 12.5K, f = 8.4 GHz.

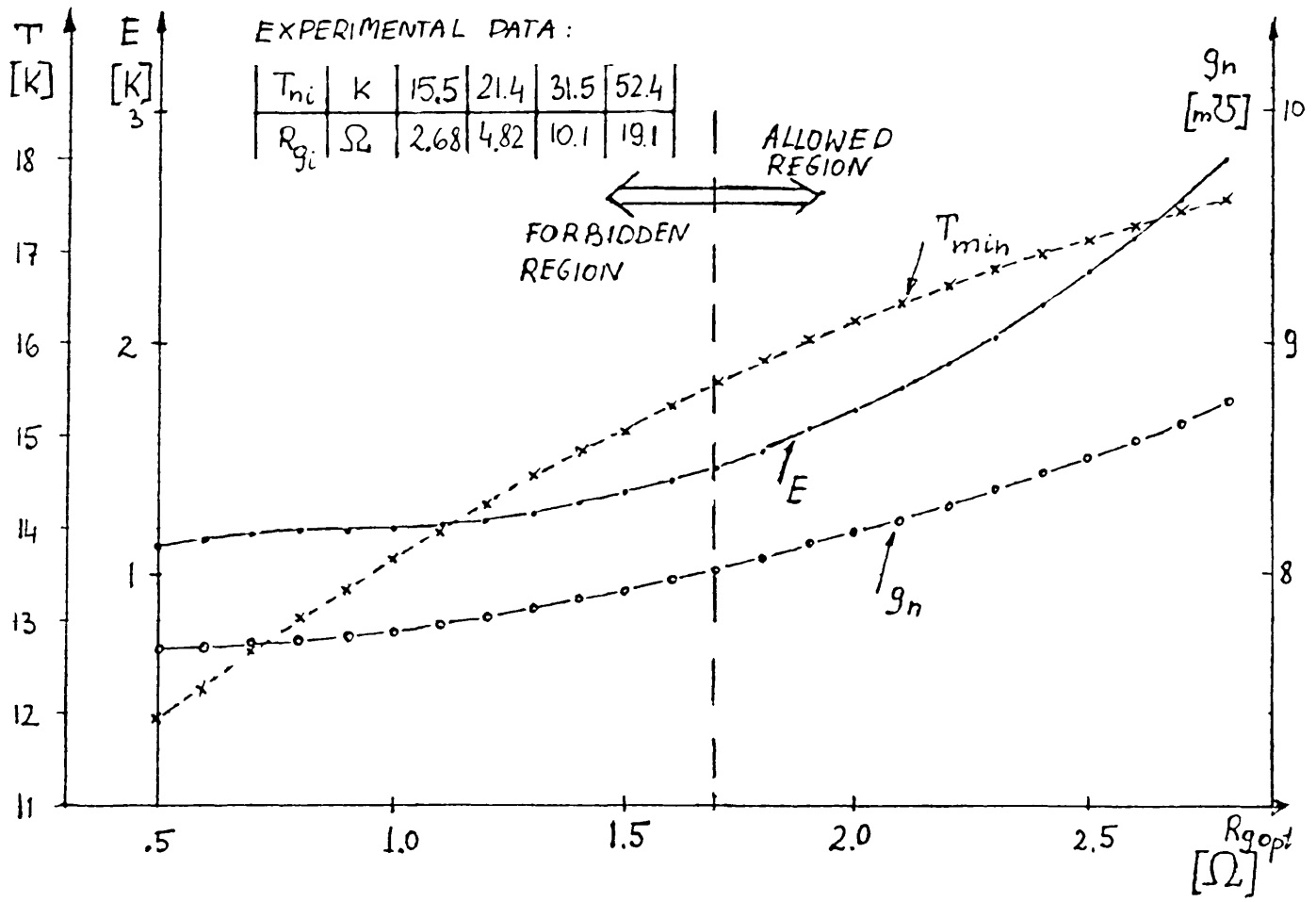


Fig. 16. The error function E, minimum noise temperature T_{min}, and noise conductance g_n found by linear regression using equation (8) versus assumed value of the optimum source resistance R_{gopt}. The experimental data are given in the table and are for FSC10FA #1 transistor at V_{ds} = 3.0 V, I_{ds} = 5 mA, T_a = 12.5K, f = 8.4 GHz.

no minimum of error function E occurs in the allowed region. This example provides a good insight into why so many noise data published in literature (for instance [3], [4]) may not represent any physical two-port.

The preceding analysis shows that it is very difficult to make a statement about the accuracy of the measurement of the noise parameters, unless the analysis similar or equivalent to these illustrated in Figure 15 or Figure 16 is carried out. For the data of Figure 15, the accuracy of T_{min} is determined only by the accuracy of the noise temperature measurement alone, as estimated previously. Optimum source resistance R_{gopt}, however, may assume a value from within the range (2.9-4.9) Ω and noise conductance g_n from within the range (4.4-6.1) mmhos. The error brackets should be of the same order for all cryogenic data given in this report. It should be pointed out that in all analyzed examples, the lower bound on noise conductance g_n is determined by the inequality (3).

The accuracy of the measurement of noise parameters can certainly be increased with the increased number of noise temperature measurement taken for properly chosen values of generator resistance. For cryogenic temperatures, however, this does not seem to be a feasible approach because of a number of cool-downs required.

III. Computer-Aided Design of Three-Stage Amplifier

The noise and circuit model of the FSC10FA transistor, described in Chapter II of this report, was used in the computer-aided design of a three-stage amplfiier. The general schematic of the circuit under consideration is shown in Figure 17 The assumed structure of the input and output coupling networks and also the interstage coupling networks are shown in Figures 18 and 19, respectively.

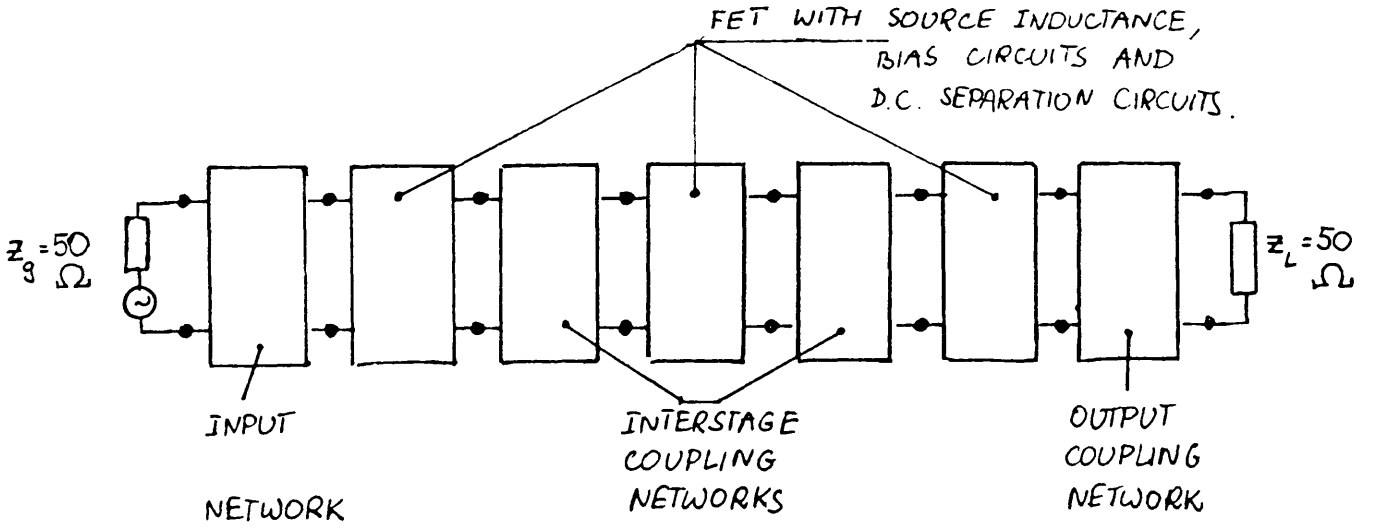


Fig. 17. The general schematic of the three-stage amplifier.

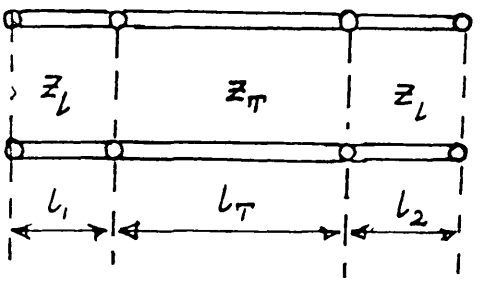


Fig. 18. The structure of the input and output coupling networks.

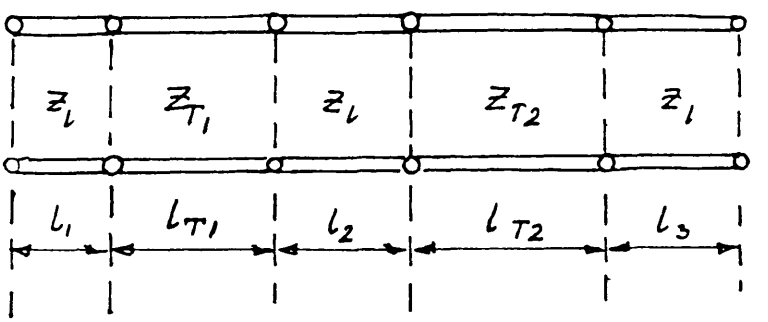


Fig. 19. The structure of the interstage coupling network.

The performance of the amplifier was computer optimized using the following criteria:

1) The input coupling network and the coupling network between the first and the second stage were optimized from the point of view of the best noise performance within the specified frequency range. The objective function, that had been minimized, was defined as follows:

$$F_1 = \sum_{j=1}^{11} T_{nj}^c \tag{10}$$

where T_{nj}^c is the noise temperature computed at the frequency f_j given by:

$$f_j = \{7.9 + (j-1) * .1\} \text{ GHz} \tag{11}$$

2) The interstage coupling network between the second and the third stage and the output coupling network were optimized from the point of view of the gain flatness within the band specified. The objective function, that had been minimized, was defined as:

$$F_2 = \sum_{i=1}^{11} (G_j^c - 30)^2 \tag{12}$$

where G_j^c is the transducer gain in decibels for $Z_g = Z_c = 50\ \Omega$ computed at the frequency f_j given by the relation (11).

Some other types of input, output and interstage coupling networks were also tried in the computer experiments. No meaningful improvement in the amplifier performance was observed, as compared with the networks of Figures 18 and 19. These networks were chosen for the realization for the following reasons:

1) The mechanical realization was relatively easy using square-slab line as a transmission medium. This realization assured also very low losses of the networks.

2) For the characteristic impedance Z_1 assuming values between 40 and 50 Ω (consult Figures 18 and 19) the values of Z_T for the best performance of the amplifier were in the range 10 to 20 Ω and could be "traded" for the total length of the coupling networks. This in turn enabled the distance between the transistors to be chosen with regard to other factors like the bias circuit realization or parasitic coupling between the stages.

3) The low impedance sections of the coupling networks could be realized in the form of movable slugs, thus enabling small experimental corrections of the noise and gain characteristics of the amplifier by moving the slugs along the line.

The computer programs implementing the design approach described in the preceding part were written in BASIC for the HP9816 computer using general purpose FARANT program [6].

In the prototype version of the amplifier the characteristic impedance Z_1 was chosen to be equal to 50 Ω (compare Figures 18 and 19) and the FET d.c.-bias and d.c.-separation circuits (reentrant line) were exactly the same as in the single stage design (see Figures 2 and 3). Then the optimization process with the objective functions as defined by (10) and (12) was carried out. It was observed during many optimization runs that without any sacrifice in the amplifier noise and gain performance, the value of characteristic impedances Z_{Tn} could be set at certain conveniently realized values. For the prototype version these were: 13.7 ohms for the input and first interstage coupling networks, 19.3 ohms for the second interstage and output coupling network. These choices allowed

in turn the distance between the stages to be set at .9", a convenient trade-off between space requirements for the bias circuit realization, stability considerations and the amplifier compactness.

The photograph of the practical realization of this design is shown in Figure 20.

The low impedance sections were designed as a square-slab lines with movable slug-type cylindrical center conductors and a coaxial dielectric filling. The approximate design data for this line are given in Appendix I. All other elements of this realization are the same as for the single stage amplifier discussed in Chapter II of this report.

The comparison between the computer predicted and measured performance is shown in Figures 21, 22 and 23. The measured performance is for the amplifier with the FSC10FA transistors in the first and the second stage and the MGF1412 transistor in the third stage, all biased at I_{ds} = 10 mA, V_{ds} = 3 V. Use of the MGF1412 transistor in the third stage did not change the noise performance of the amplifier, as compared with the FSC10FA realization, but slightly increased the gain (by approximately 1.5 dB). The computer model used the equivalent circuit of FSC10FA transistor and its noise parameters given in Chapter II of this report. The only parameter that was experimentally adjusted was the length of the reentrant line (compare the equivalent circuit of a single stage in Figure 3), i.e., the length of the transistor gate and drain leads. The length of the gate and drain leads used in the computer model was .250", while in the experimental realization it was necessary to trim it down to .21" in order to obtain the center frequency of 8.4 GHz. The transistor used in the first stage was FSC10FA #1, which noise parameters were measured and are given in Chapter II. Hence, the good agreement between predicted and measured noise performance

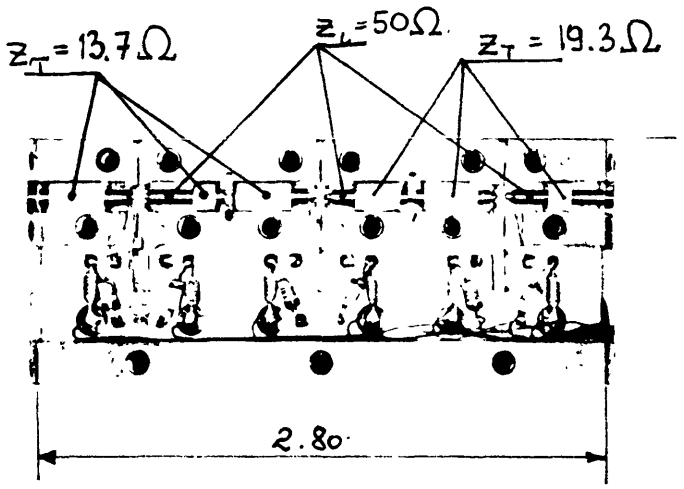
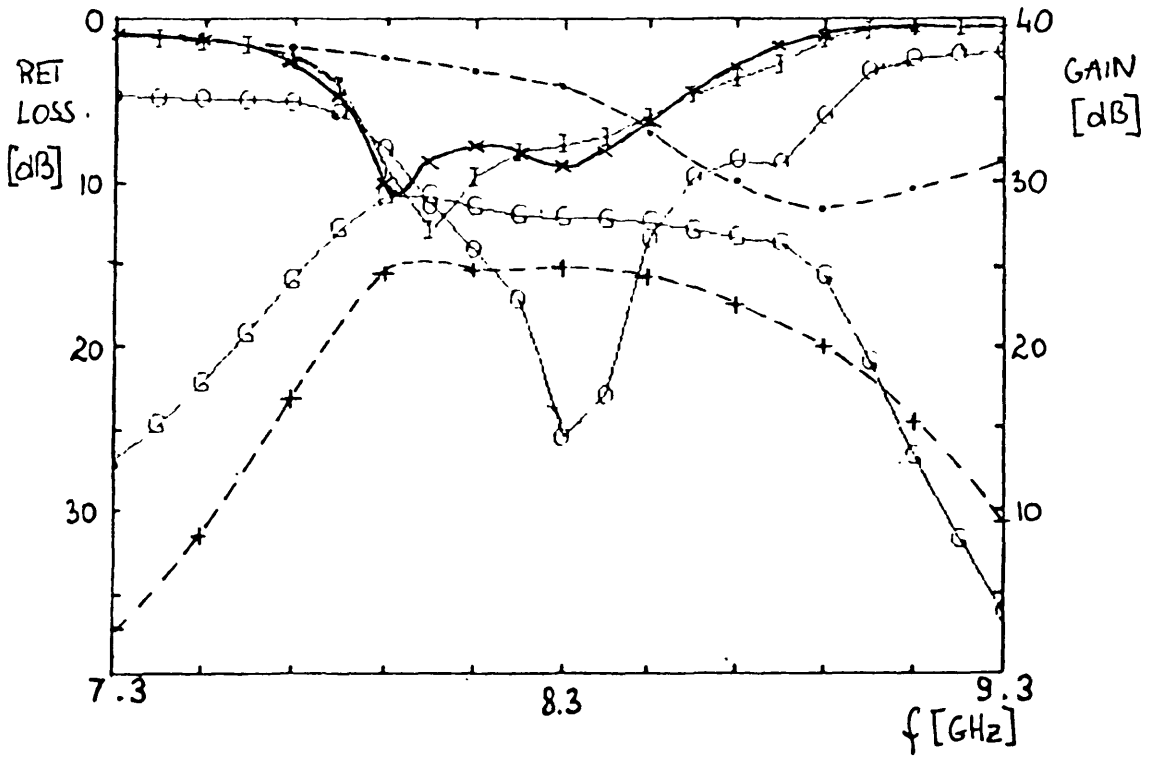


Fig. 20. The photograph of the prototype version of the three-stage 8.4 GHz amplifier with cover plate removed.



	MEAS.	COMP.
INP. RET. LOSS	×	I
OUT. RET. LOSS	•	O
TRANS. GAIN	+	G

Fig. 21. Computer generated and measured results for the three-stage amplifier of Fig. 20 at the room temperature. All transistors are biased at V_{ds} = 3 V, I_{ds} = 10 mA.

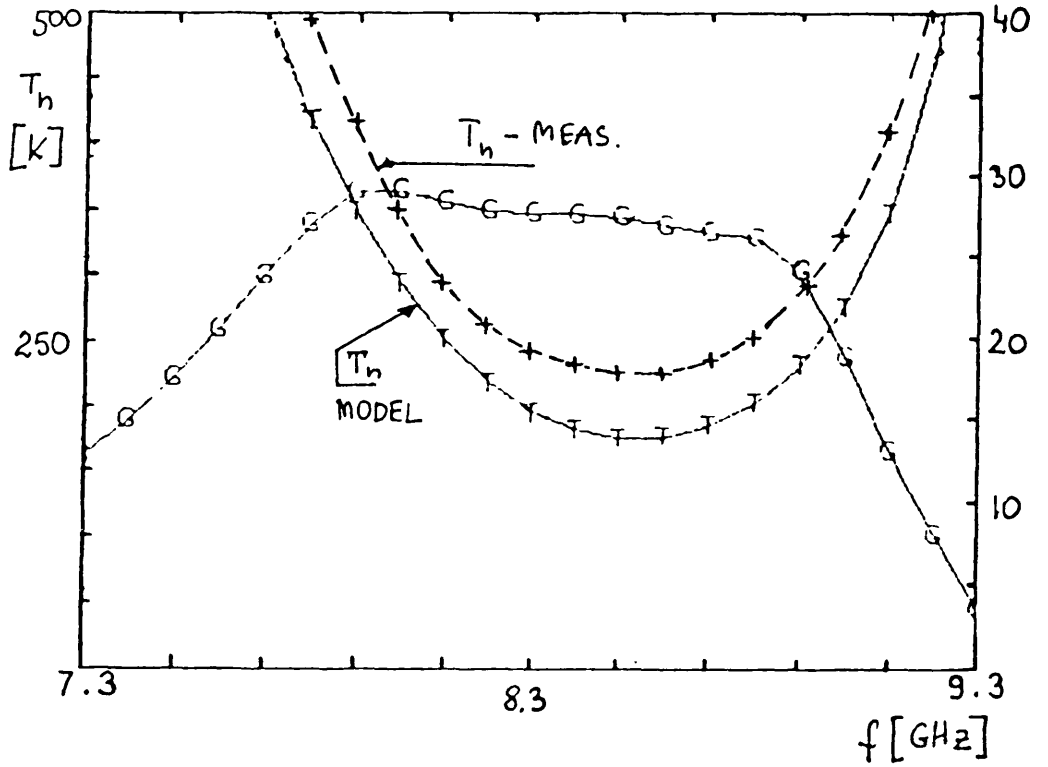


Fig. 22. Noise temperature of the three-stage amplfiier of Fig. 20 at the room temperature computed from the model and measured. All transistors are biased at V_{ds} = 3V, I_{ds} = 10 mA.

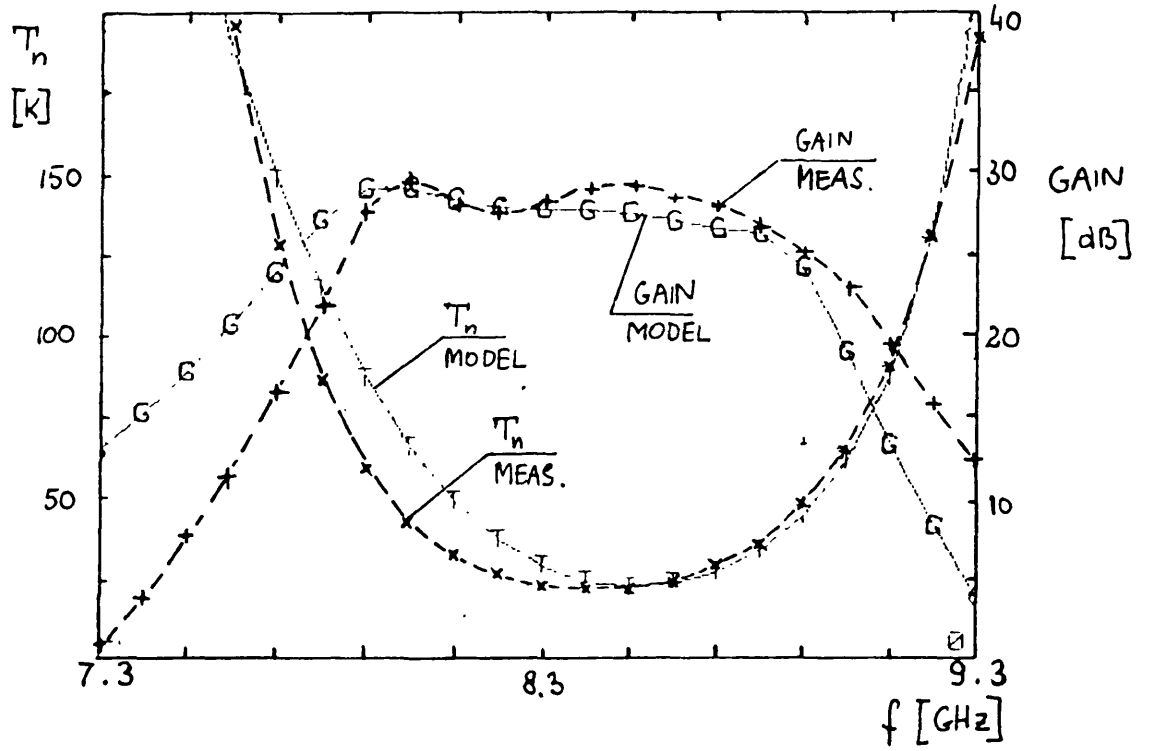


Fig. 23. Noise temperature and gain of the three-stage amplifier of Fig. 20 at the cryogenic temperature (T_a = 12.5K) computed from the model and measured. All transistors are biased at V_{ds} = 3V, I_{ds} = 10 mA.

for cryogenic temperatures was to be expected, as it is demonstrated in Figure 23. In contrast, the agreement between the computer prediction and the measurement for the room temperature is not very good (Figure 22). In this case, however, the impedances determining the noise performance of the first and second transistor are far from the optimum values for the room temperature and therefore small errors in the noise conductance determination could account for quite large differences between the measured and computed values of the noise temperature. The differences between the computer predicted and measured values of the transducer, gain, input return loss, and output return loss can be accounted for by the differences between the model and the experiment for the single stage.

The experimental search for the optimal operating bias for this amplifier from the point of view of minimum noise and maximum gain resulted in the characteristic shown in Figure 24. The minimum noise temperature of 20K and average noise temperature of 26K with the minimum gain of 28.4 dB and maximum gain of 32.1 dB across 8.0-8.8 GHz band have been obtained.

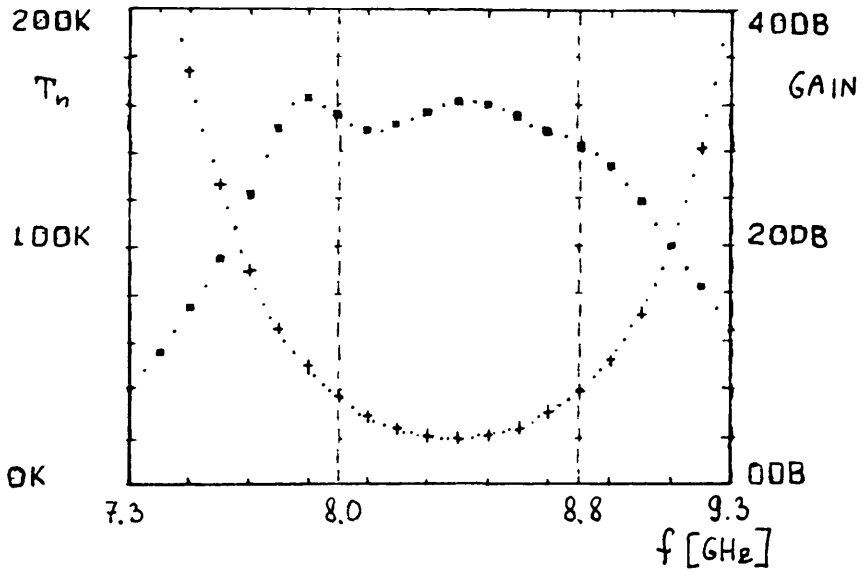
An isolator was needed at the input of the amplifier to improve the input match. The isolator ASI7011 made by TRW was chosen for that purpose. This isolator has losses of 0.4 dB at the temperature of 12.5K. The noise temperature of the cascade connection of the isolator and amplifier cooled to 12.5K was on the average 3.5K higher than the noise temperature of the amplifier alone.

The study of cryogenic performance of some commercial X-band isolator is described in the next chapter.

IV. Room Temperature and Cryogenic Performance of Commercial X-Band Isolators

A. Experimental Study of Parameters of Commercial X-Band Isolators

Four commercially available X-band, coaxial isolators have been tested for their cryogenic performance. These were: ASI7011 and AMI7984 models made



f,GHZ	T_n, K	GAIN,DB	f,GHZ	T_n, K	GAIN,DB
7.8	65.3	29.9	7.9	48.8	32.3
8	36.4	30.8	8.1	28	29.7
8.2	23	30.1	8.3	20.4	31.2
8.4	19.7	32.1	8.5	20.7	31.9
8.6	23.7	30.8	8.7	29.1	29.7
8.8	37.9	28.4	8.9	51.1	26.6

Fig. 24. Noise temperature and gain for the three-stage amplifier of Fig. 20 at the optimal bias conditions: first stage, V_{ds} = 2.4 V, I_{ds} = 11 mA; second stage, V_{ds} = 2.3 V, I_{ds} = 17.5 mA; third stage, V_{ds} = 3.3 V, I_{ds} = 17.5 mA.

by TRW-Aertech [16], XTE-1120 model made by Pamtech [17] and 60B4 model made by Ferrocom [18]. Their parameters measured in the bandwidth of 7.9 to 8.9 GHz, both at room and cryogenic temperatures, are presented in Table X.

The best performance at the cryogenic temperature was exhibited by the TRW-Aertech isolators. The performance of both units was virtually the same. Also, their parameters at the temperature of 14K showed very little variation over the specified frequency range, what was not the case for the Pamtech and Ferrocom units. The construction of the ASI7011 isolator seemed to be much better suited for cryogenic applications than that of the AMI7986 isolator. Therefore, the ASI7011 isolator has been chosen for the 8.4 GHz receiver construction. This isolator was also used as the output isolator in the noise parameters measurement setup described in Chapter II. The procedure of deembedding of the noise parameters, described also in Chapter II, required a noise model of a lossy isolator. Two approximate noise models of a lossy isolator are presented in the next section.

B. Noise Models of a Lossy Isolator

It has been concluded [19], [20] that all isolators are the equivalent of terminated circulators insofar as their inherent noise is concerned. Therefore, the approximate models developed in this section are not dependent on the particular type of the isolator. Only the simplest case of a lossy isolator is discussed here, i.e., the isolator for which $S_{11} = 0$, $S_{22} = 0$, $S_{12} = 0$ and $|S_{21}| < 1$.

The two simple models of an isolator with losses are shown in Figure 25. Each of these is composed of an ideal isolator, which is either preceded or followed by a matched attenuator of an attenuation A given by:

$$A = \frac{1}{|S_{21}|^2} \tag{13}$$

MANU-FACTURER	TYPE	T_a = 297 K			T_a = 14 K		
		LOSS [dB]	ISOLATION [dB]	INPUT RET. LOSS [dB]	LOSS [dB]	ISOLATION [dB]	INPUT RET. LOSS [dB]
TRW-AERTECH	ASI 7011	.4	>20	>19	.4	>20	>19
TRW-AERTECH	AMI 7984	.2	>25	>20	.4	>22	>18
PAMTECH	XTE 1120	.4	>16	>20	<.7	>16	>16
FERROCOM	60B4	.4	>22	>19	<.7	>16	>16

TABLE X. Room Temperature and Cryogenic Performance of Several Commercially Available Isolators in the Frequency Band of 7.9 to 8.9 GHz.

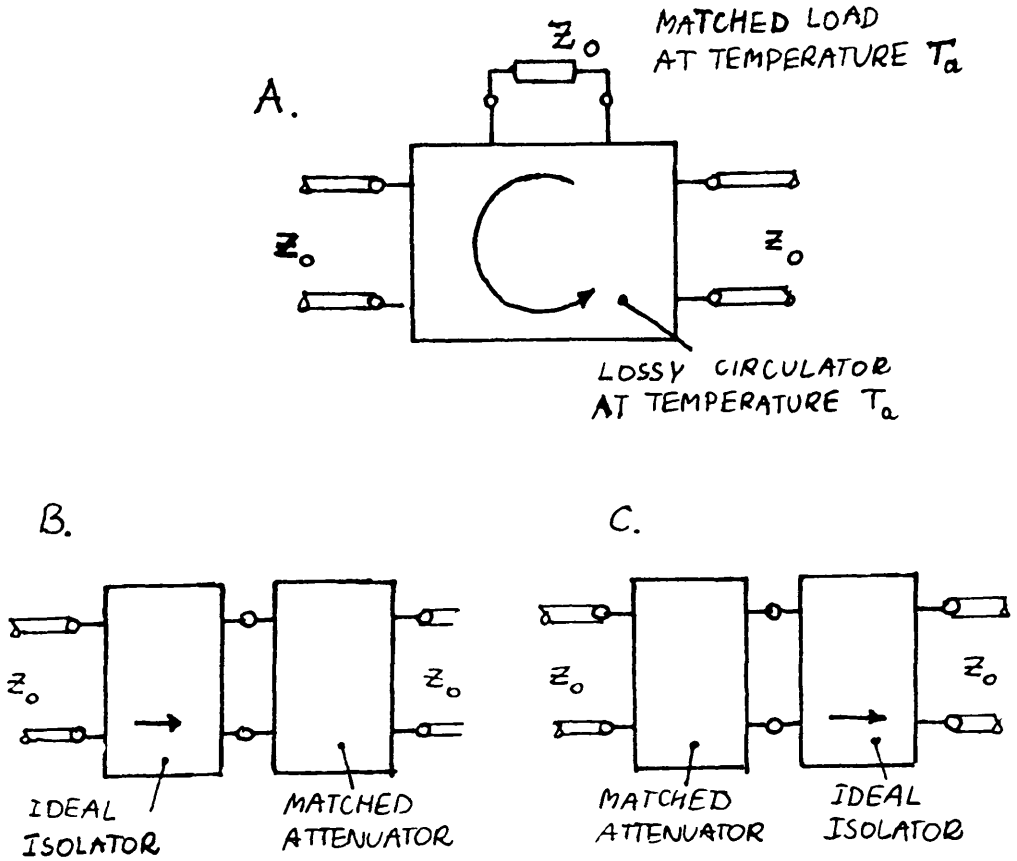


Fig. 25-A. A lossy isolator made of a lossy circulator with one port terminated in a matched load.

B-C. The possible equivalent circuits of a lossy isolator.

It is easily observed that for both models of an isolator the minimum noise temperature T_{min} is equal to:

$$T_{min} = T_a \left(\frac{1}{|S_{21}|^2} - 1 \right) \tag{14}$$

where T_a is the ambient temperature. This minimum noise temperature occurs for the source impedance Z_{gopt} equal to the characteristic impedance Z_o.

The remaining fourth noise parameter is most easily expressed in terms of N parameter (see equation (2)). For the equivalent network of Figure 25-B, it is given by:

$$N = \frac{T_a}{T_o} \tag{15}$$

and for the equivalent network of Figure 25-C, it is given by:

$$N = \frac{T_a}{T_o} \left(|S_{21}|^2 + \frac{1}{|S_{21}|^2} - 1 \right) \tag{16}$$

where T_o is the standard temperature 290K.

It should be observed that both equivalent networks give very similar answers for N for any practical value of isolator attenuation. The difference in N computed from expressions (15) and (16) is less than 5 percent for attenuations up to 1 dB.

V. 8.4 GHz, Cooled, Three-Stage Amplifier

A. Design

The prototype version of the three-stage amplifier was modified for the purpose of making the amplifier easier to manufacture, assemble and tune.

Relying on the CAD techniques described in Section III of this report, the following changes were made:

1) The d.c. separation circuits (re-entrant lines) were realized in the form of an open-end section of a triplate stripline of a very low characteristic impedance. This change was introduced to make the transistors replaceable without the need of disassembling any of the input, output and/or interstage coupling networks. The very low characteristic impedance of the triplate stripline (~ 7 Ω) makes the band-reducing influence of the d.c. separation circuit negligible.

2) The characteristic impedances Z_{Ti} of all low-impedance sections of the matching and coupling circuits (compare Figures 18 and 19) were set to be the same and equal to Z_T = 13.7 Ω. This modification was made solely to simplify the manufacturing process.

3) The characteristic impedance Z_l of the air filled slab lines was set to be equal to Z_l = 42 Ω. This change was introduced as a result of the computer aided optimization of the amplifier performance carried out under the condition $Z_{Ti} = Z_T$ = 13.7 Ω. The optimization determined also the length of the low impedance sections as well as their position in the input, output and interstage coupling networks.

B. Construction

The assembled amplifier with cover plate removed is shown in Figures 26, 27 and 28. The low impedance sections were designed as square-slab lines with movable, slug-type cylindrical center conductors and a cylindrical dielectric filling (design data for this line are given in Appendix I). The teflon cylinders of the low impedance sections provide also the mechanical support for the inner

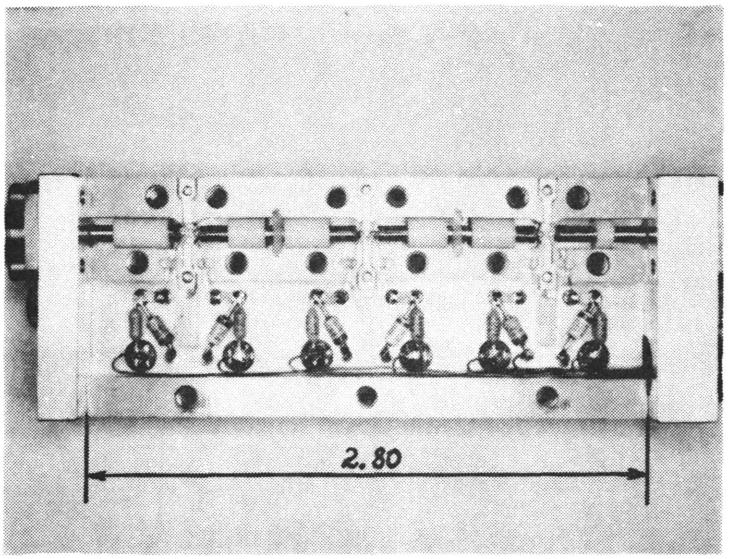


Fig. 26. Three-stage amplifier with cover removed. Input is at left and output and DC bias connector are at right.

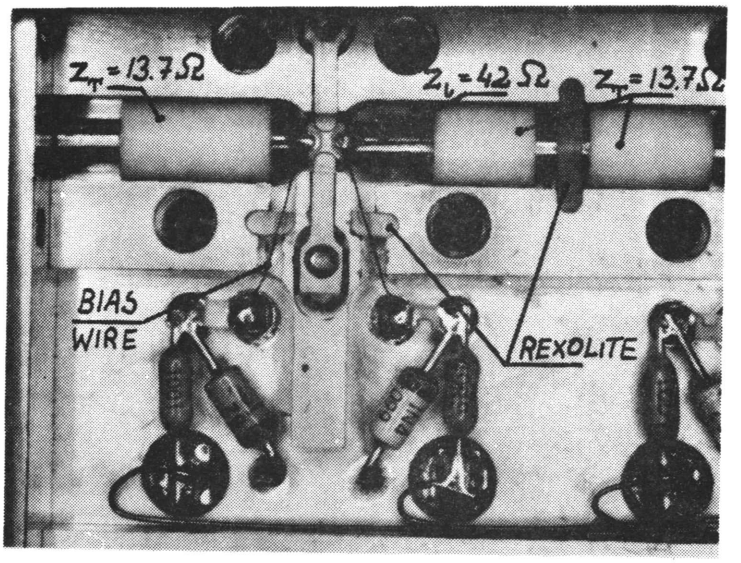


Fig. 27. The enlarged view of the first-stage section of the three-stage amplifier.

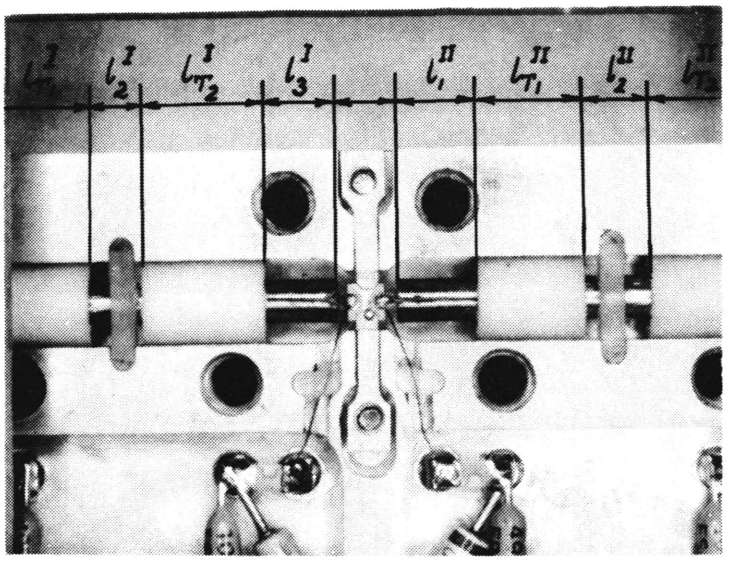


Fig. 28. The enlarged view of the second-stage section of the three-stage amplifier. Shows length designation corresponding to that used in Figures 18 and 19.

conductor of the 42 Ω line. The inner conductor is prevented from moving along the channel by the rexolite "captor," as it is shown in Figures 27 and 28.

The dimensions of the different sections of the input, output and interstage coupling networks resulting from the computer optimization of the amplifier performance are given below (notation as shown in Figure 28, dimensions in inches):

Input network: $l_{1in} = .085$, $l_{Tin} = .277$, $l_{2in} = .078$

I Interstage coupling network: $l_1^I = .140$, $l_{T1}^I = .185$, $l_2^I = .106$,

$l_{T2}^I = .221$, $l_3^I = .138$

II Interstage coupling network: $l_1^{II} = .143$, $l_{T1}^{II} = .195$, $l_2^{II} = .134$,

$l_{T2}^{II} = .215$, $l_3^{II} = .103$

Output network: $l_{1out} = .184$, $l_{Tout} = .083$, $l_{2out} = .173$

The details of the construction of the d.c. separation circuits are shown in Figure 29-A. The gate and drain FET leads are first twisted by 90 degrees and then cut to the desired length (Table XI):

TABLE XI. Length of the Transistor Leads in the Three-Stage Amplifier

		Lead Length	
	FET	Gate	Drain
I Stage	FSC10FA	.090	.110
II Stage	FSC10FA	.090	.90
III Stage	MGF1412	.085	.085

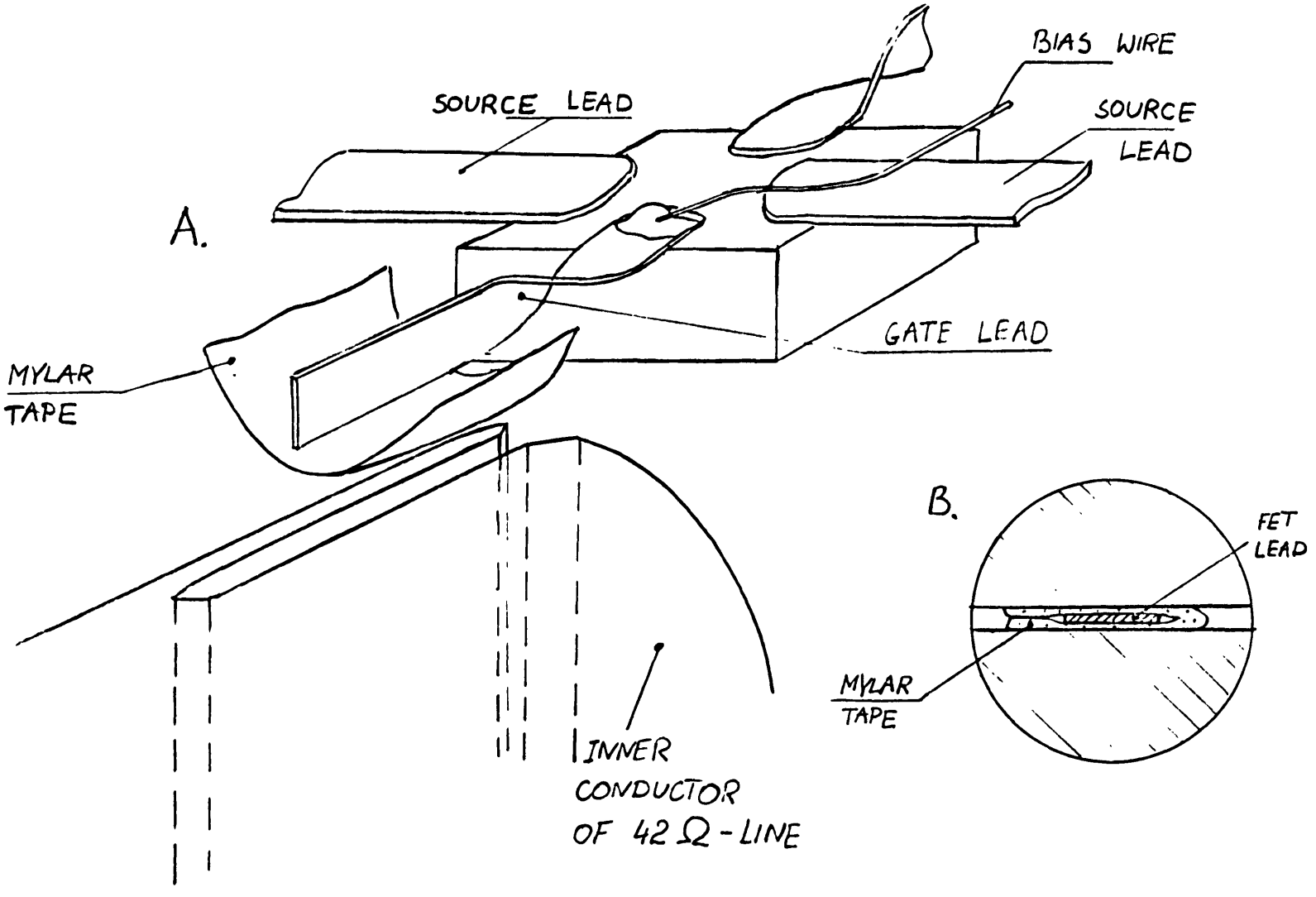


Fig. 29. A. Schematic view of the realization of the d.c. separation circuits.

B. Cross-section of the re-entrant line after assembling.

After soldering of the bias wires to the gate and drain pads on the transistor package, the leads are wrapped in MYLAR tape of .5 mil thickness. Either self-adhesive MYLAR tape or non-adhesive tape and Eastman 910 glue can be used. The insulated lead, placed in the slot, 6 mils wide, cut in the inner conductor of the slab-line, forms a re-entrant line of a very low characteristic impedance (~ 7 Ω). The cross-section of this line is shown in Figure 29-B. The value of its characteristic impedance was determined using Gunston's data for the tri-plate stripline [10].

The construction of the d.c. bias circuit is in principle the same as reported previously [3], [23]. The schematic of this circuit is identical as for the single stage amplifier and is given in Figure 3. It should be noted that the one pF chip capacitor exhibits series resonance at the frequency of 9 GHz with the Q-factor of 6 [24]. The detailed assembling instructions of the bias circuit are given in [23]. The rexolite supports of the bias wires, shown in Figure 27, assure the mechanical stability of this structure.

C. Results

The measured room temperature performance of the amplifier which photographs are shown in Figures 26, 27 and 28 is shown in Figure 30. The expected performance derived from the computer model is also shown. The only parameter adjusted experimentally was the position of the input transformer. Off-the-shelf FSC10FA and MGF1412 transistors were used.

The performance of the same amplifier measured and the temperature of T_a = 12.5K and computed from the model is shown in Figure 31. Finally, the best performance of the amplifier with respect to the operating biases of the transitors is shown in Figure 32.

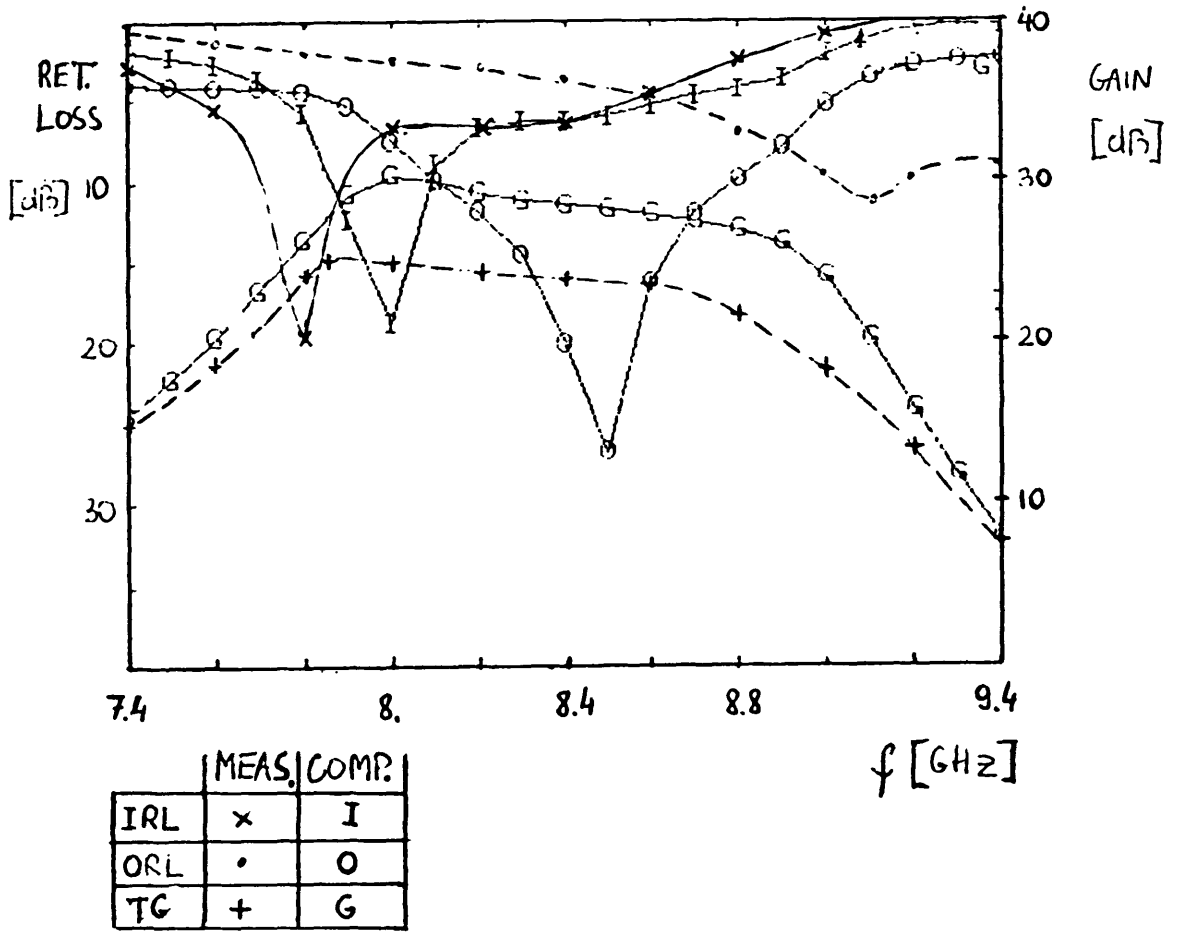


Fig. 30. Computer generated and measurement results for the three-stage amplifier of Fig. 26 at the room temperature. All transistors are biased at V_{ds} = 3 V, I_{ds} = 10 mA.

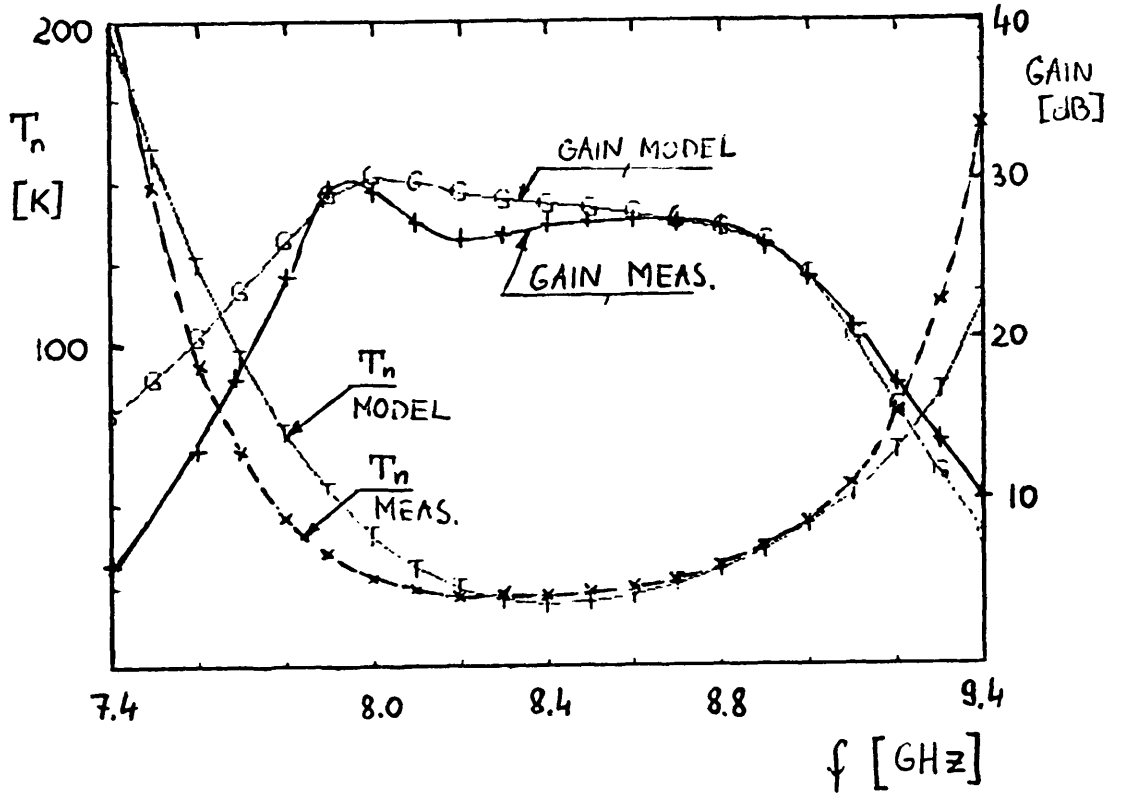


Fig. 31. Noise temperature and gain of the three-stage amplifier of Fig. 26 at the cryogenic temperature (T_a = 12.5K) computed from the model and measured. All transistors are biased at V_{ds} = 3 V, I_{ds} = 10 mA.

1) AMP.#312; BEST OP. BIAS
13:33.7 11/02/84 TAU=24.1 TLO=21.9 @ 8350 GL=28.3 GH=30.8 T=12.4K
3.24,8.2,-.543 4,15,-.669 4.01,19.5,-.896
13:34.8 11/02/84 ZERO=4.7 ADB=20 TF=14.7 -NDB=5.4

F,GHZ	T_n,K	GAIN,DB	F,GHZ	T_n,K	GAIN,DB
7.9	32.7	32.9	8	27.1	30.8
8.1	24.1	29.1	8.2	22.7	28.8
8.3	22	29.3	8.4	21.9	29.9
8.5	22.4	30	8.6	23.7	29.7
8.7	26.1	29.3	8.8	30	28.3
8.9	36.3	26.2	9	46.6	22.8

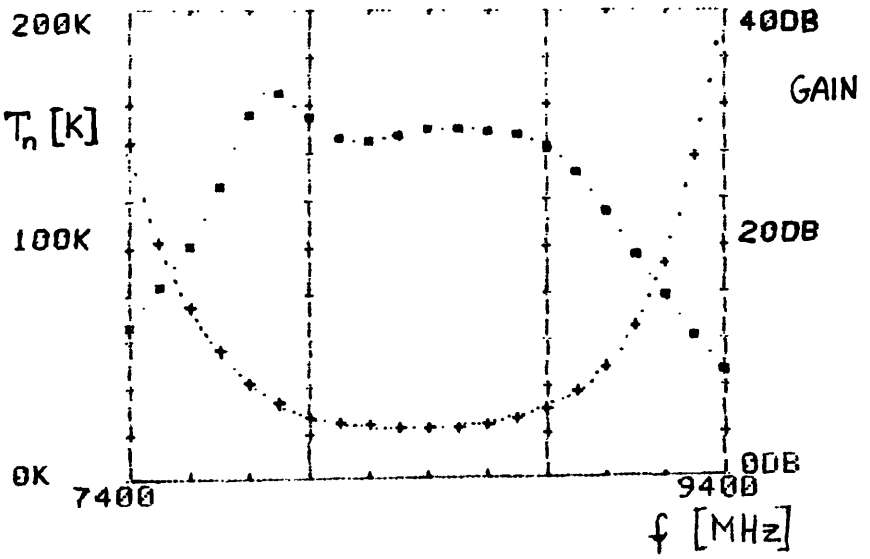


Fig. 32. Noise temperature and gain for the three-stage amplifier of Fig. 26 at the optimal bias conditions: first stage, V_{ds} = 2.3 V, I_{ds} = 8 mA; second stage, V_{ds} = 2.5 V, I_{ds} = 15 mA; third stage, V_{ds} = 2.0 V, I_{ds} = 20 mA. These results are not corrected for approximately .7 dB of cold losses at the output (isolator and connecting lines).

The comparison of measured performance of this design with that of the prototype version reveals better bandwidth properties of the final version. Slightly higher noise temperature in the midband (22K as compared to 20K for the prototype version) is thought to be caused by the higher minimum noise temperature T_{min} of the transistor used in the first stage.

There are two very important practical questions:

1) How repeatable is the performance of the amplifier if not-preselected transistors are used?

2) How much tuning is required to obtain the desired performance?

The tuning of the amplifier of the present design can be done by several means:

- changing the length of the re-entrant lines which affects mostly the center frequency of the amplifier,
- changing the position of the low impedance sections which affects both the shape of the amplifier response and the center frequency,
- and varying the bias of the transistors.

Four amplifiers of the same design were constructed using off-the-shelf FSC10FA and MGF1412 transistors. Their performance for the optimal bias conditions is summarized in Table XII.

TABLE XII. The Summary of Cryogenic Performance of the Three-Stage Amplifiers Within the Frequency Range 8.0-8.8 GHz

AMP	NOISE TEMP. [K]		GAIN [dB]	
	Minimum	Average	Minimum	Maximum
Prototype	20	26	28.4	32.1
#1	22	24	28.3	30.8
#2	24	28	28.4	31.3
#3	24.5	29	28.7	31.8
#4	25	30	29	33

For comparison, the performance of the prototype version is also included. It was found that no individual trimming of the transistor lead length was required. The positions of the low-impedance sections were slightly varied, but by no more than 30 mils to achieve the desired performance. The position of the low impedance section in the input network has been found to be especially important, as it determines the frequency at which the minimum noise temperature occurs. Final tuning was done by varying the transistor bias.

VI. Conclusions

The complete set of information needed to design X-band, cryogenically cooled amplifiers has been presented. The feasibility of using room temperature S-parameters for a design of cryogenically cooled amplifiers has been demonstrated in the design of the three-stage amplifier for the 8.0-8.8 GHz frequency band.

The careful evaluation of noise properties of a number of GaAs FET's and the use of the computer-aided optimization techniques in the amplifier design allowed to achieve the amplifier performance which should be close to the attainable limits for packaged, commercially available GaAs FET's. Several amplifiers were constructed using commercial, off-the-shelf transistors. These amplifiers exhibited minimum noise temperatures of 20K to 25K, average noise temperatures over 800 MHz bandwidth of 24K to 30K, and gain variation of less than $\pm$ 2 dB at the gain of about 30 dB.

The novel procedure for determining the noise parameters of the transistor has been introduced. In this procedure the computations necessary to find the noise parameters from the set of measurements of the noise temperature for different values of the source impedance are greatly simplified. This method allows also for an easy assessment of the accuracy with which the noise parameters can be determined from the given set of measurement data.

VII. Acknowledgements

The author gratefully acknowledges many stimulating discussions with Dr. S. Weinreb. R. Harris and K. Crady are thanked for their excellent experimental and technical assistance.

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APPENDIX I

IMPEDANCE DATA FOR A SQUARE SLAB LINE WITH NON-UNIFORM TEFLON FILLING

The cross section of the air filled square slab line is shown in Figure A1 and the cross section of the line under consideration is shown in Figure A2. Several methods of analysis of the square slab line with the uniform dielectric filling have been published [10]. The approximate formula of Frankel ([10], p. 64) is sufficiently accurate for most practical applications. This formula for the air filled line takes the form:

$$Z_o = 59.952 \ln(1.0787 \frac{D}{d}) \text{ ohm} \qquad \text{(A1)}$$

The formula is virtually exact for $d/b < .65$ and gives an error within 1.5 percent for $d/b < .80$ [10]. Equation (A1) can obviously be rewritten as:

$$Z_o = 59.952 \ln \frac{D}{d} + 4.542 \text{ ohm} \qquad \text{(A2)}$$

The first term in expression (A2) is the characteristic impedance of the coaxial line having the same inner conductor as the square slab-line and the outer conductor as denoted by the broken line in Figure A1. The second term therefore appears to be a correction due to the different shape of the outer conductor. Hence,

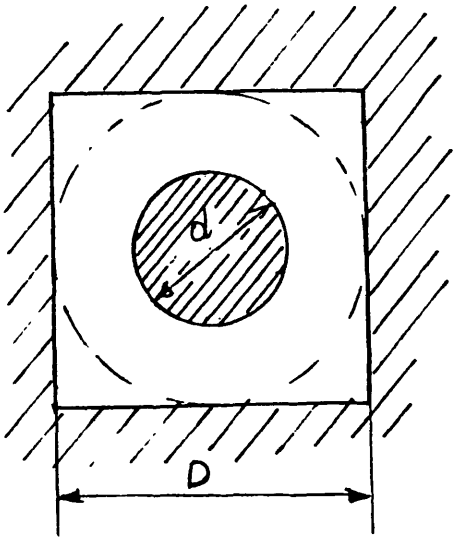

Figure A1. Cross-section of the air-filled, square-slab line.

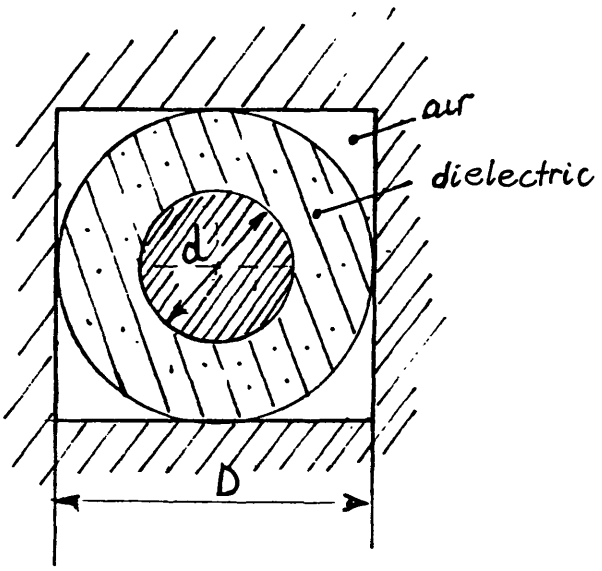

Figure A2. Cross-section of the square-slab line with the cylindrical dielectric filling.

the square slab line can be modeled as a series connection of two transmission lines, i.e.:

$$Z_o = Z_{oc} + Z_{or} \tag{A3}$$

where:

$$Z_{oc} = 59.952 \ln \frac{D}{d} \text{ ohms} \tag{A4}$$

and

$$Z_{or} = 4.542 \text{ ohms} \tag{A5}$$

For large $\frac{d}{D}$ ratios ($\frac{d}{D} > .8$), the validity of this model can be retained, if different values of Z_{or} are taken for each value of $\frac{d}{D}$. Using the most accurate data of Gunston ([10], p. 65) for the square slab line, the impedance Z_{or} can be found as a function $\frac{d}{D}$. This is done by substracting from the accurate value of the characteristic impedance of a given air-filled square slab line the corresponding value of the characteristic impedance Z_{oc} of the coaxial line. This procedure for an air-filled line yields the results presented in Figure A3. The results in this figure indicate that the expression (A1) is valid for $\frac{d}{D} < .85$ with the accuracy better than .2 ohms.

The comparison of the cross sections of lines in Figures A1 and A2 reveals that only the "coaxial portion" of the line of Figure A2 is filled with the dielectric. Hence, to a first approximation the characteristic impedance of a square-slab line with coaxial dielectric filling is given by the formula:

$$Z_o' = \frac{59.952}{\sqrt{\varepsilon_r}} \ln \frac{D}{d} + Z_{or} \tag{A6}$$

where ε_r is the relative permittivity of the dielectric. Once Z_o' is found from

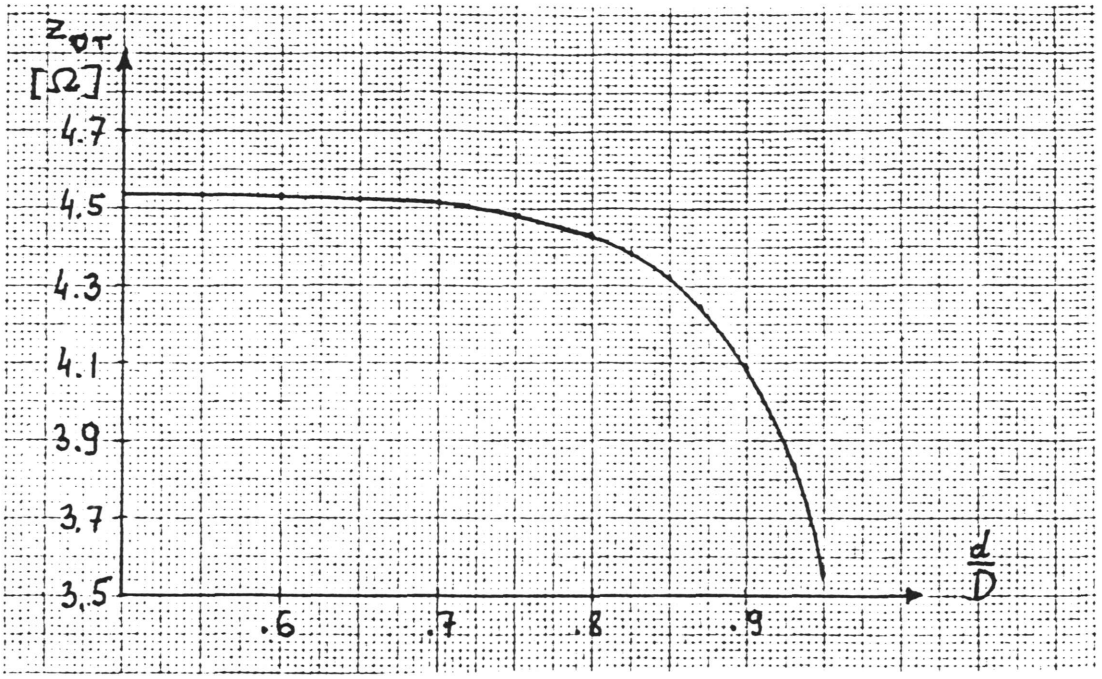

Figure A3. The dependence of the impedance Z_{or}, as defined by the equation (A3) on $\frac{d}{D}$ ratio of the air-filled, square-slab line.

the expression (A6) the effective dielectric constant for this line can be easily found from:

$$\varepsilon_{reff} = \left(\frac{Z_o'}{Z_o} \right)^2 \qquad \text{(A7)}$$

where Z_o is the characteristic impedance of the air-filled line with the same cross section as given by equation (A3).

The data for the square slab line with the coaxial teflon filling obtained the method outlined in this Appendix are presented in Figure A4. These data were used in the design of the three-stage amplifier. The data are believed to be sufficiently accurate for most practical applications, but no direct theoretical or experimental verifications of their accuracy have been carried out.

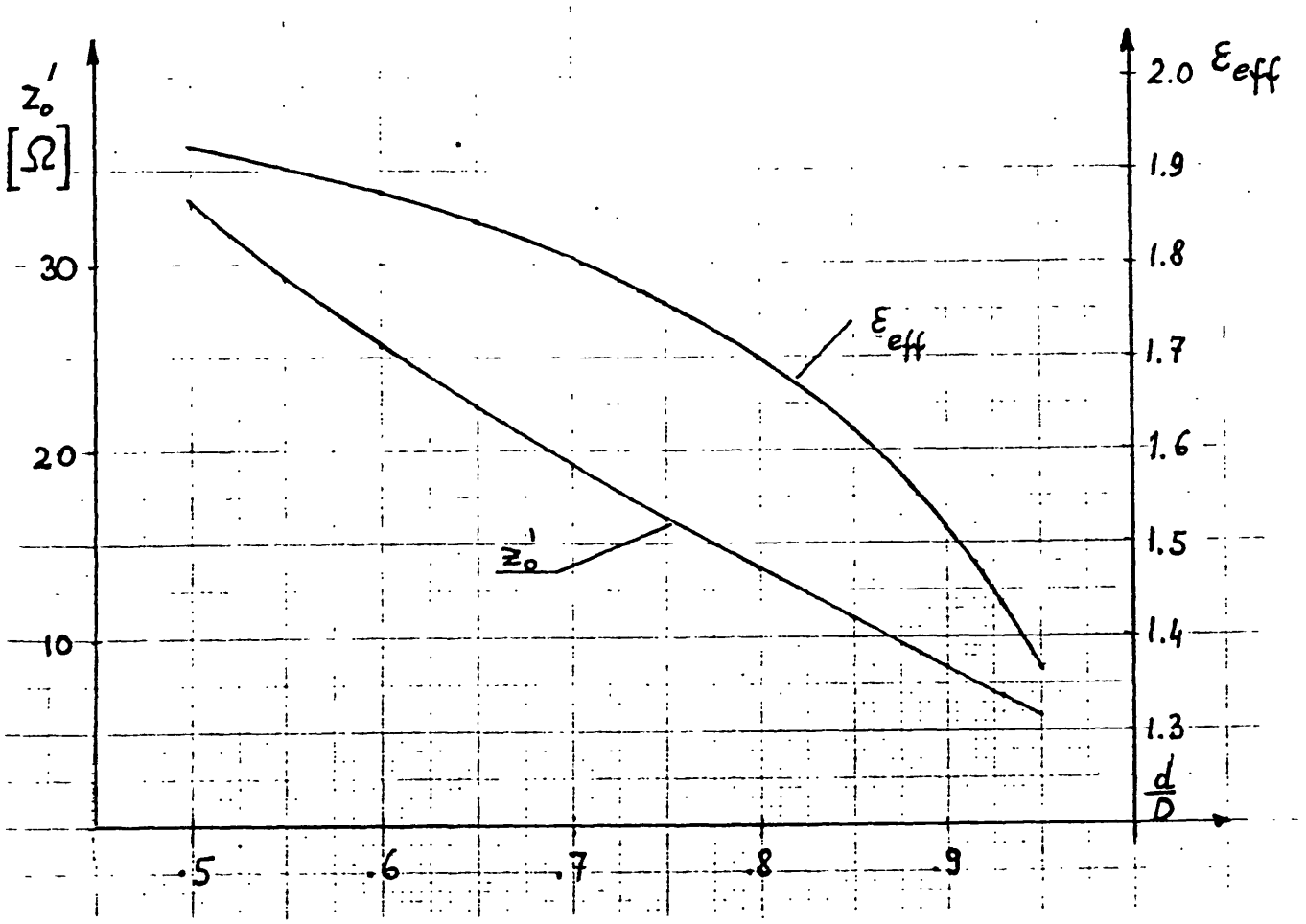

Figure A4. The characteristic impedance and effective dielectric constant of the square slab line with coaxial teflon filling.