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IF SYSTEM MANUAL FOR THE SPECTRAL PROCESSOR

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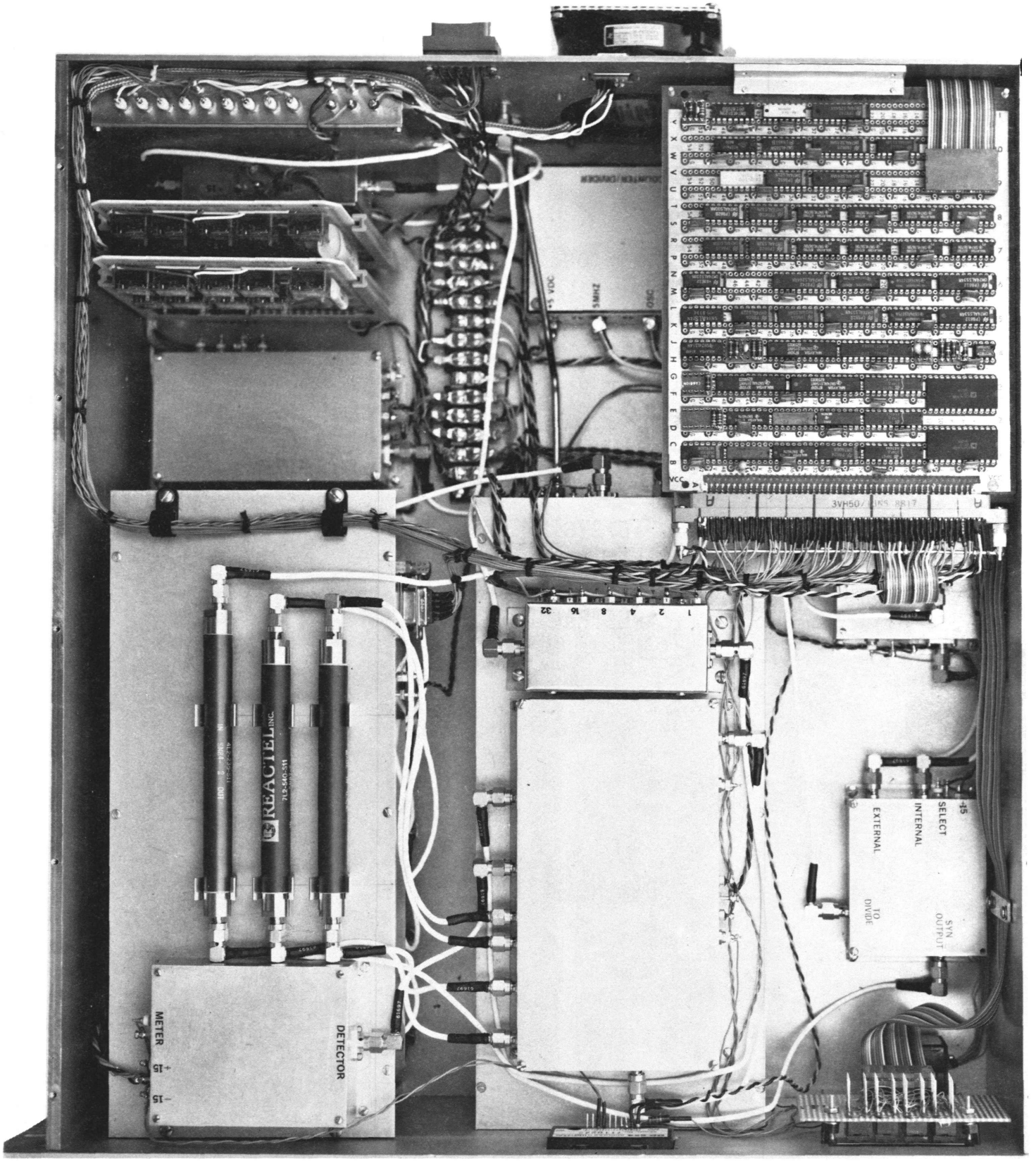

PHOTOGRAPH OF SSB DOWNCONVERTER

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IF DRAWER FOR THE SPECTRAL PROCESSOR

S. D. White and D. R. Schiebel

I. Introduction

The IF system consists of a Digital Interface drawer for translating a RS-422 serial bus to a 16 line parallel bus for controlling the SSB Downconverters, a phased-locked 160 MHZ LO distribution drawer, a 5 MHZ buffer and distribution module, a power supply drawer, a Wavetek frequency synthesizer, and eight SSB Downconverters. The system parameters are set by a rack controller via a serial bus and then monitored. The system accepts signals in the 100 MHZ to 500 MHZ frequency range and demodulates them using a single-sideband scheme to a maximum baseband frequency of 40 MHZ. All local oscillators and frequency synthesizers are phased locked to an external 5 MHZ reference. All the drawers are housed in a standard rack.

II. Digital Interface

A. Introduction

The digital logic that controls each SSB Downconverter can be divided into two sections. The first section is a small chassis (BUS DRIVER) that contains a "VLBA MONITOR AND CONTROL CARD" (vlba c/m) and a logic card to drive the "IF RACK ADDRESS AND DATA BUS". The vlba c/m card gets setup information from the "RACK CONTROL COMPUTER" over a RS422 serial bus. The second section is a logic card located in each IF drawer. It gets setup information from the IF RACK ADDRESS AND DATA BUS. The circuit analysis for the logic card is contained in the SSB Downconverter section.

B. Detailed Logic Description Bus Driver

The vlba c/m card in the bus driver chassis provides the link between the rack control computer and a logic card to drive a address and data bus inside the IF rack. A detailed description of the operation of the vlba c/m card will not be presented here, it can be found in vlba memo number 302.

The logic on page 1 of "ADDRESS/DATA BUS DRIVER CARD" as shown in Figure 5 drives the address and data bus in the IF rack. The address is a buffered version of the"RelativeAddress" from the vlba c/m card. The data bus is more complicated in that it is a bi- directional bus. In the write mode data from the vlba c/m card CON/MON bus is

buffered and applied to the data bus in the IF rack. In the read mode data from the IF rack data bus is latched in two latches then applied to the vlba c/m CON/MON bus.

The last page of the logic drawings contain the logic necessary to communicate with the vlba c/m card and control the timing of the IF rack address and data bus. The following is a list of signals used by the vlba c/m card.

DEV REQ	This line is normally low and goes high when the vlba c/m card is requesting a read or write sequence by the interface.
DEV ACK	This is a reply line from the interface to the vlba c/m card. It is normally low and goes high to indicate the requested action has been completed.
RD/WR-	Used to indicate a read or write sequence. Normally low which indicates a write, goes high for a read.
ID REQ	Issued by the vlba c/m card requesting the interface to put its ID on the con/mon data bus. In our system the A rack has an ID of 4 and the B rack has and ID of 8.

The timing of the read or write operation is controlled by a shift register U21. During a write operation the vlba c/m data is passed to the IF rack data bus then 4-6 micro sec later the data will be latched in the selected IF drawer by the WR pulse.

The read operation timing is such that after the address has been placed on the address bus the read pulse (U25 pins 3 & 4) will go active. At the leading edge of the RD pulse the selected IF drawer will place its data on the IF rack data bus. On the trailing edge (about 2 micro sec. later) of the RD pulse the data on the IF rack data bus will be latched in U19 & U24. Then 2 micro sec. later the vlba c/m card is informed (dev ack) that data is available. On the trailing edge of the RD pulse the selected IF drawer will remove its data from the IF rack data bus.

Two time stretched pulses are generated to drive led's to indicate read and write activity on the IF rack data bus.

For RFI rejection it was necessary to put a ferrite bead on each address and data line and connect a 1500 pf capacitor to ground.

This logic is contained on a standard "SMALL SHALLOWAY CARD" which had a 40 pin ribbon connector attached to the top of the card. A 40 pin ribbon cable runs between each IF drawer and the Bus Driver Chassis.

III. 160 MHZ PLL

An oven controlled Vectron CO233VHBR crystal oscillator is phased locked to a 5 MHZ reference. The circuit diagram is shown in Figure 6. A lock indicator is displayed on the front panel. The output is amplified by a QB-210 amplifier and filtered by a 160 MHZ bandpass filter. The LO is split by an Olektron HJ-308V 8-way divider. The second and third harmonics are less than 50 DBc at an output level of +13 DBm.

IV. 5 MHZ Buffer

The buffer contains three of the circuits shown in Figure 7. The buffer provides 12 outputs at a gain of 0 DB. The measured stability performance of the 12 outputs was an average of 4 ps/℃.

V. Wavetek Frequency Synthesizer

An operations manual is available for the Wavetek Model 2200 frequency synthesizer.

VI. Power Supply

The power supply drawer contains a +24 V supply, a +15 V supply, a + 5V supply, and a -15 V supply. The power supplies are manufactured by Power One. The ratings for the supplies are: +24 V @ 2.4 A, +15 V @ 15 A, +5 V @ 35A, and -15 V @ 9A. A table of total power consumption for the rack is given in Table 1. The power is available through a 90 pin Elco connector, and the pin assignments are shown in Table 2.

VII. SSB Downconverter

A. System Analysis

The SSB Downconverter accepts RF frequencies in the range from 100 MHZ to 500 MHZ and downconverters the signal to a maximum baseband frequency of 40 MHZ using a single sideband demodulation scheme. A block diagram of the SSB downconverter is shown in Figure 8. The connector assignment is shown in Table 3. The SSB downconverter is externally set using a VLBA monitor and control card. An internal digital card provides the interface to the monitor and control card. A 0 - 63 DB variable attenuator at the input adjusts the output power level to any desired level. The input signal is split and square law detected. A logarithmic amplifier drives an LCD located on the front panel which displays the power level at the RF input of the mixer in DBm. Also, an overload detection circuit detects signal levels greater than -10 DBm at the mixer input. The input signal is converted to an IF frequency of 160 MHZ using an inverting upperside LO injection scheme in the RF downconverter module. The frequency range of the internal synthesizer is 170 MHZ to 500 MHZ with a 10 KHZ resolution. A doubler extends the range to 660 MHZ with a 20 KHZ resolution. The LO must be set to convert the desired 40 MHZ bandwidth signal in the RF input into an IF frequency range of 120 MHZ to 160 MHZ when the upper sideband is selected or an IF frequency range of 160 MHZ to 200 MHZ when the lower sideband is selected. For RF frequencies in the range 100 MHZ to 355 MHZ, an image spectrum exits ; therefore, a lowpass filter in the RF input rejects the image frequencies. A SSB demodulator converts the IF signal to a baseband signal from 8 KHZ to 40 MHZ while rejecting the undesired sideband by approximately 28 DB. The baseband signal is then filtered by a filter bank having a range from a maximum of 40 MHZ varying in octave steps to a minimum of 78 KHZ. The signal is split with one path being amplified by 37 DB and output to the A/D converters while the other path is square law detected and processed by analog circuits in order to generate a pulse approximately equal to the width of the interference. The detected signal is also input to the voltage-to-frequency converter in order to monitor the power output. The output amplifier is capable of providing a power level of +5 DBm with no compression for band limited Gaussian noise.

B. Circuit Analysis

1. RF Downconverter

The circuit diagram of the RF Downconverter is shown in figure 9. The RF downconverter consists of three QB-104 amplifiers, a CDB-223 mixer, a DS-109 power divider, and a overload detection circuit. The RF to IF gain is approximately 21 DB. The maximum RF power into the RF port of the mixer is 0 DBm; therefore, the overload detection circuit is adjusted to toggle high when -10 DBm is applied to the mixer to allow for 10 DB of headroom. A Teledyne DPDT relay selects the input bandwidth of either 355 MHZ or 540 MHZ. A 235 lowpass filter at the output rejects all unwanted harmonics of the LO and RF inputs.

2. Single Sideband Demodulator

The circuit diagram for the SSB Demodulator is shown in Figure 10. The design goal for rejection of the unwanted sideband is 40 DB for signals in the 8 KHZ to 40 MHZ frequency range. The theoretical analysis for the image rejection is presented in a paper by Archer, Granlund, and Mauzy.[1] The block diagram of the circuit, Figure 1, is essentially the same except a pre-conversion to an IF of 160 MHZ eliminates the need for a quadrature LO over a broad band. Also John Granlund developed a program to compensate for the cross talk effects and adjust the values to achieve equal ripple in the image response. The theoretical image response is shown in Figure 2. The values for the phase shift network were computed for an image rejection of 52 DB with equal ripple over a band from 8 KHZ to 40 MHZ. The tolerance for error in amplitude and phase from quadrature in the signal paths is computed to be ~0.18 DB and ~1.15° respectively.

The circuit is similar to the circuit in the Model IV autocorrelator.[2] The technique of winding the shield of semirigid coax on pot cores to construct the inductors in order to generate a floating signal was used. A shunt current feedback amplifier was added

after the quadrature mixers to improve signal to noise ratio. The pre-conversion eliminates the need for a quadrature hybrid: a coax delay was used for the 160 MHZ LO. The network rejected the image frequencies a minimum of 25 DB. The source of error was attributed to the difference in conversion loss and phase match between the quadrature mixers. An increase in LO power improves the VSWR of the mixers thereby improving the match between mixers. However, the distortion introduced to the LO by the increased power increases the uncertainty in measurement of coax needed to achieve quadrature and also increases the LO feedthru. Therefore, no net gain in rejection is obtained from the improved match. The desired image rejection may be achieved from more carefully selecting the quadrature mixers if time and expense allows. A typical measurement for image rejection in shown in Figure 3.

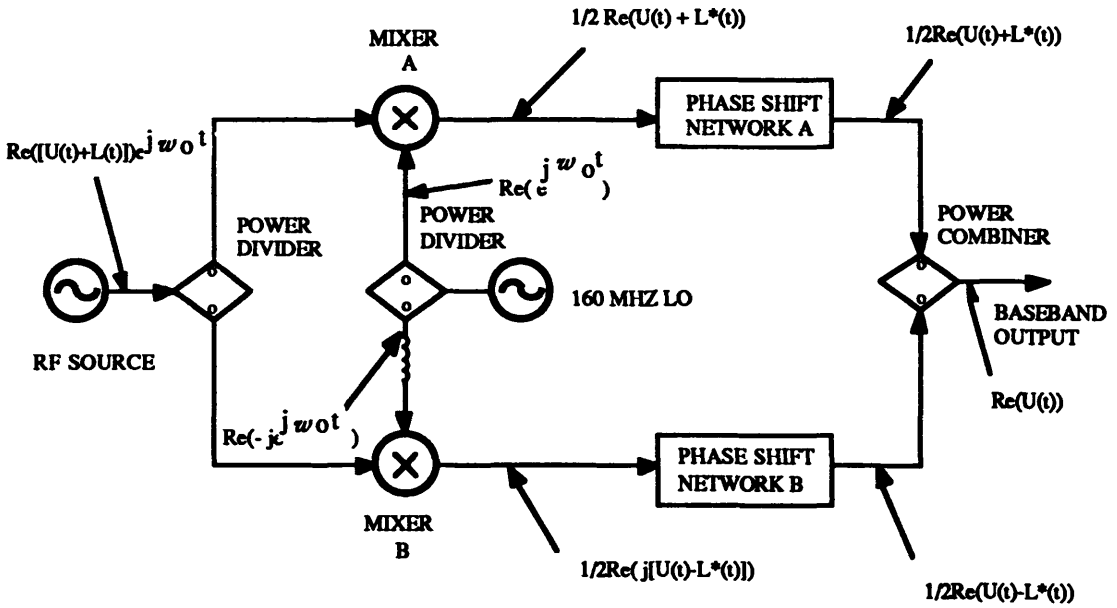


Figure 1 SSB Demodulator Block Diagram.

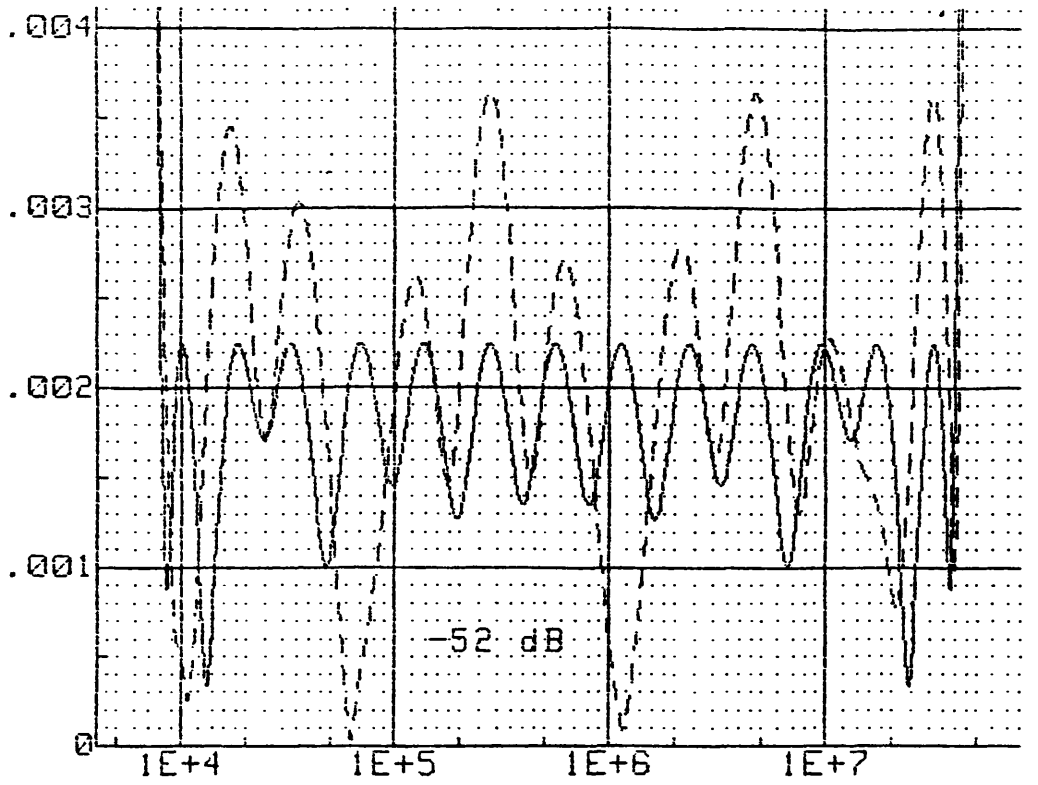


Figure 2 Theoretical Image Response of SSB Demodulator.

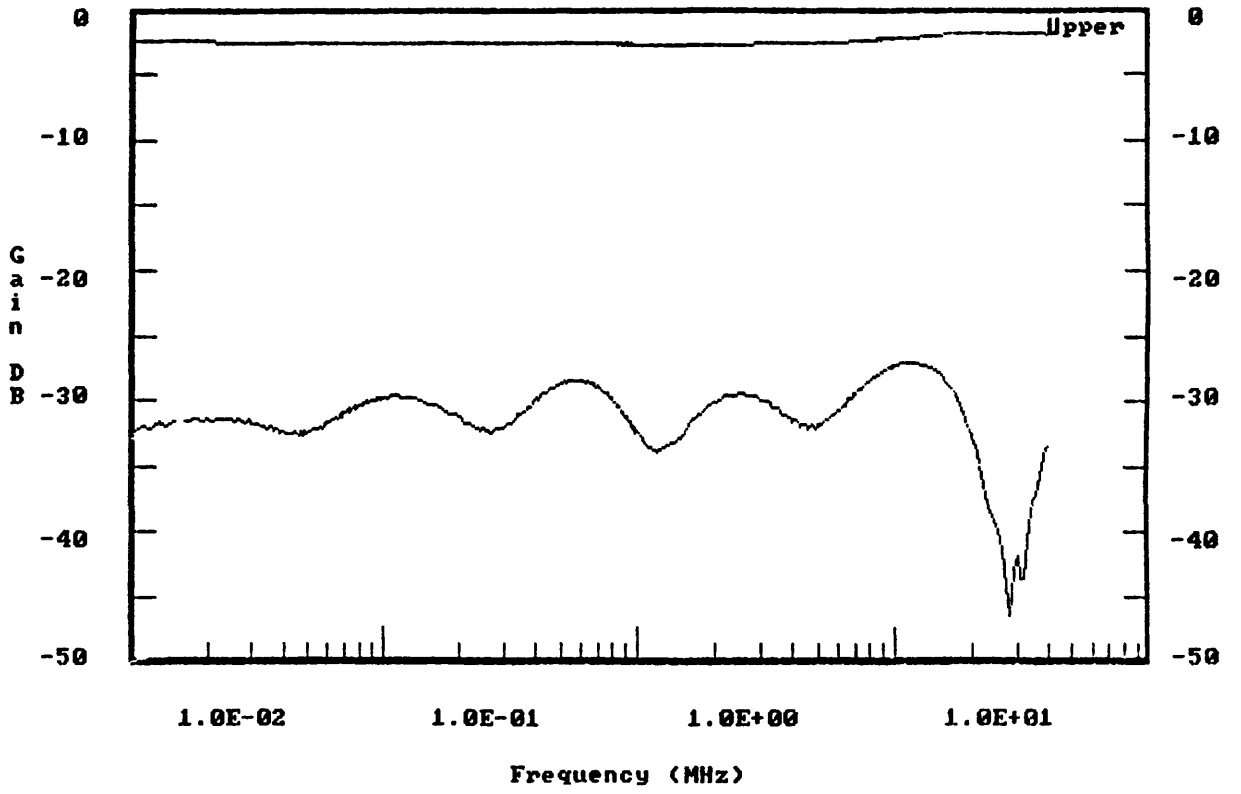


Figure 3 Typical Image Response : Unit 9 11/20/89.

3. Filter Bank and Relay Tree

The circuit diagram for the relay tree and filter bank is shown in Figure 11. The circuit is designed with 3 DB attenuators and 18 DB amplifiers such that the output level is constant for any bandwidth selected. The amplifiers are MC 1733 video amplifiers. The digital card is designed to select the proper relays for the filter chosen.

4. Interference Detector

The circuit diagram for the interference detector is shown in figure 12. The input is amplified 30 DB by a MC 1733 video amplifier. The output amplifier has a dual output where one output is input to the analog to digital amplifier and the other output is square law detected by a BD-4 tunnel diode. The power input to the tunnel diode is given by:

$$P_{diode}\,[DBm] = P_{out}\,[DBm] - 24.4\,[DB] \qquad [1]$$

The diode voltage in the square law region can be predicted by the equation:

$$V_{diode}[DCV] = P_{diode}[\mu W]\ \xi\,[\mu V/\mu W] \qquad [2]$$

where $\xi = 2.03\ [\mu V/\mu W]$ is the conversion constant. When the output power level is -8 DBm, the power input to the detector diode is 0.575 μW. The detected voltage is 1 mV. Because an op-amp circuit amplifies the signal by -240, the output to the voltage-to-frequency converter is -0.240 V.

The detected signal is also filtered by a lowpass filter and then amplified by two separate op-amp circuits. The output of the one op-amp is input into a fast integrator, and the output of the other op-amp circuit is input to a slow integrator. The slow

integrator provides a reference for a differentiating difference amplifier so that slight changes in the power level will not cause false detection of interference. The slow integrator has 9 time constants selectable by external relays. The values of RC time constants available for the slow integrator are 1×10^{-4} s, 3×10^{-4} s, 1×10^{-3} s, 3×10^{-3} s, 1×10^{-2} s, 3×10^{-2} s, 1×10^{-1} s, 3×10^{-1} s, 1 s. The RC time constants for the fast integrator are 1×10^{-6} s, 3×10^{-6} s, 1×10^{-5} s, 3×10^{-5} s, 1×10^{-4} s, 3×10^{-4} s, 1×10^{-3} s, 3×10^{-3} s, 1×10^{-2} s. An external dc level is input to the slow integrator through a germanium diode which clips the detected signal and prevents the slow integrator from saturating. When a pulse is detected, the long time constant of the slow integrator lengthens the rise time of the pulse. Since the rise time of the detected interference from the fast integrator is faster, a difference signal is detected and then amplified by the differentiating amplifier. The differentiating amplifier configuration was selected to avoid problems of DC offset. The pulse width at the output of the differentiating amplifier is proportional to the difference in time constants of the two integrators. A CMP-01 comparator with hysteresis generates a pulse from the output of the difference amplifier. An external dc level input to the comparator determines the amplitude of the detected interference necessary to produce a detection pulse. The comparator output is input to a differential TTL line driver.

The noise voltages at various nodes in the circuit can be predicted by equations for square law detection of Gaussian noise.[3] The detected rms noise at the output of the op-amp circuit is given by:

$$V_{rms} = A_o V_{diode} / (\sqrt{\Delta \upsilon_{hf}\ 2\tau_{lf}}) \qquad [3]$$

where $\Delta \upsilon_{hf}$ is the predetection bandwidth, τ_{lf} is the postdetection time constant, and A_o is the gain of the the op-amp circuit. The predetection bandwidth is determined by the filter bank, the postdetection time constant is 4.44×10^{-7}s, and A_o is 20. The clipper voltage can be set by the equation:

$$V_{clipper}[DCV] = V_{offset} - V_{rms}(2.05) - \Delta V_{margin} + V_{ger} \quad [4]$$

where $V_{germ} = 0.2$ V, ΔV_{margin} is the voltage limit of the signal to be clipped, and $V_{offset} = 20(V_{diode} + V_{nom})$ with V_{nom} being a DC offset of the op-amp circuit of 1.34×10^{-3} V. The DC offset is introduced so the DC output of the op-amp is zero when an output power level of -8 DBm exists. The noise level at the output of the differentiating difference amplifier can be determined from the geometric mean of the slow integrator noise and the fast integrator noise. The equation was determined from theoretical predictions of the noise and empirically from data taken for gain of the integrators and amplifiers. The equation for threshold level will produce a digital signal with a duty cycle less than 1%. The equation is:

$$V_{threshold}[DCV] = [\, V_{diode}(582) \;/\; (\sqrt{\Delta \upsilon_{hf}}\,)\,] \times \sqrt{(1/\tau_s + 1/\tau_f)}\,. \quad [5]$$

where τ_s and τ_f are the time constants for the slow and fast integrators respectively.

The comparator has a hysteresis loop that is 50 mV to reduce edge jitter on the output pulse.

The equations for the comparator are :

$$V_1 = V_{threshold}(R_2 \;/\; R_2 + R_1) + V_{ol}(R_1 \;/\; R_2 + R_1) \quad [6]$$

$$V_2 = V_{threshold}(R_2 \;/\; R_2 + R_1) + V_{oh}(R_1 \;/\; R_2 + R_1) \quad [7]$$

$$V_m = (V_2 - V_1)/2 \quad [8]$$

where $V_{ol} = 0.41$ V, $V_{oh} = 5.0$ V, $R_1 = 10$ KΩ, and $R_2 = 1$MΩ. Then $V_m = 24$ mV. Therefore a threshold level of $-V_m$ will produce a digital signal with a 50 % duty cycle.

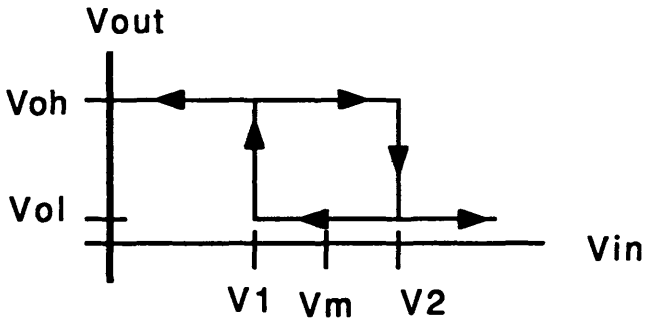


Figure 4 Comparator Transfer Function

5. Analog to Digital Amplifier (AD Amp)

The circuit diagram for the AD amp is shown in Figure 13. The AD amplifier is a two stage amplifier with the first stage being a shunt current feedback amplifier and the output stage being a class A push pull amplifier. The circuit was designed for maximum power output with minimum distortion. The loaded gain of the circuit is 12.8 DB with a 1 DB compression point at 13.47 DBm. The amplifier specifications for distortion levels measured at a + 5 DBm output level is -60 DBc for the second harmonic and -58 DBc for the third harmonic.The return loss at the input port is -38 DB and -33 DB at the output port for frequencies less than 40 MHZ.

6. Voltage to Frequency Converter and Total Power Monitor

The circuit diagram for the V/F converter and the TP monitor are shown in Figure 14. The V/F converter produces a 10 KHZ digital signal with an input voltage of -0.240V. The voltage to frequency conversion is accurate to 1% over a± 6 DB range. The design equations are:

$$C_1\ [pf] = [33 \times 10^6/f_{max}] - 30 \qquad [9]$$

$$f_o\ [HZ] = V_{in}/7.5(R_1)(C_1) \qquad [10]$$

$$C_2\ [\mu f] = 10^2/f_{max} \qquad [11]$$

where f_{max} = 30 KHZ, V_{in} = -0.240 V, and f_o = 10 KHZ. The LO is divided by 256

by a Motorola MC 12074 ECL chip. The output is level shifted and converted to a differential TTL signal.

7. Logarithmic Amplifier

The schematic for the Log amp is shown in Figure 15. The RF input is divided and square law detected by a BD-4 diode. The detected voltage is processed by the Log amp and level shifted in order to display the power in DBm. The equation for the Log amp is:

$$V_{log} = 25.7 \text{ mV } (R_1 + R_2)/R_2 \ln [(V_{diode} / V_{ref})(R_3/R_4)]. \quad [12]$$

From equation 2, the expression for the diode can be written as:

$$P_{in} = 10 \text{ Log}[V_{diode}/\xi(1 \text{ mW})] \text{ [DBm]}.$$

Also,

$$\text{Log } x = \ln x / \ln 10 .$$

Therefore,

$$(R_1 + R_2)/R_2 = 16.90 \quad [13]$$

and

$$V_{ref} = (R_3/R_4)\xi(1 \text{ mW}) \quad [14]$$

which gives $V_{ref} = 1.0$ V with $(R_3/R_4) = 2$. The values then can be solved and levels adjusted in order to produce a voltage which has a numerical value equal to the power level in DBm. This value then can be displayed on an LCD meter.

8. Frequency Synthesizer

Either an external or an internal frequency synthesizer can be selected. The circuit diagram for the selector is shown in Figure 16. The internal frequency synthesizer is the same as used in the Mark III IF to video converter. Due to the unavailability of parts and a change in frequency range for the SSB downconverter, the VCO and amplifier were changed.

The VCO changes included a replacement of three MV109 with two ZC803 varacter tunnel diodes. The low VCO now tunes over a range from 170 MHZ to 290 MHZ. Thus, the switch over point is 270 MHZ.

The amplifier for the synthesizer is shown in figure 17. The amplifier has a minicircuits doubler which is switched into the circuit for frequencies from 500 MHZ to 660 MHZ. An external 4-pole elliptical bandpass filter was need to filter the unwanted harmonics of the doubler. The circuit diagram and frequency response is shown in Figure 18. The power output of the frequency synthesizer is +7 DBm ±2 DB with the highest harmonic less than -30 DBc.

9. Digital Card

Each IF drawer contains a "LARGE SHALLOWAY CARD" connected to the IF drawer address and data bus through a 40 pin ribbon connector attached to the top of the card.

The basic function of the card is to decode the address bus and if it finds it is being addressed then it will read or write data to the data bus. In addition the card contains logic to store a copy of the setup data to be displayed by a front panel display.

The upper left hand corner of page 1 of Figure 19 contains the logic that decodes the address. The three least significant bits of the address select one of 6 data words. The four most significant bits of the address select which drawer is being addressed. Each drawer address is selected through the power connector on the IF drawer. After all decoding there are six write strobes generated, WR0- to WR5- and one read strobe RD0-.

The logic at the bottom of page 1 is used to control the front panel display through the use of a digi-switch.

Page 2 of the logic contains the data bus bi-directional transceivers (U48 & u52) and the 4 X 4 register files that store a copy of the setup data to be displayed by the front panel display. At the bottom of page 2 you will find the logic that will put two status bits on the data bus, overload and lock. An led driver is also provided to indicate this status on the front panel.

Latches for data word 5 will be found on page 3. Three functions are controlled by

this word. The first half of the word (D0-D7) is used for integrator control, D8-D11 controls the bandwidth.

Setup words 0,3 and 4 will be found on page 4. Setup word 0 controls several things. The first six bits D0-D5 are used to control the attenuation. Three more bits of word 0, D8-D10 control intermode filter, upper/lower sideband and int/ext synthesizer. All other bits of word 0 are unused. Words 3 & 4 control two D/A's, one for threshold control (wd3) and one for clipper control (wd4). Both D/A's are set up for an output of plus or minus 2.5 volts.

The last page of the logic drawings contain the latches for control of the frequency synthesizer, data words 1 and 2. It should be pointed out that due to the nature of the synthesizer (ecl logic running on +5V) the latches must be cmos, in this case we used FCT374's.

References

1. J.W. Archer, J. Granlund, and R.E. Mauzy, "A Broad-Band UHF Mixer Exhibiting High Image Rejection over a Multidecade Baseband Frequency Range," *IEEE Journal of Solid-State Circuits,* VOL. SC-16, No. 4,pp. 385-391, Aug. 1981.

2. R.E. Mauzy, "Model IV Correlator IF System," *NRAO Internal Reports of the Electronics Division,* No. 227, March 1982.

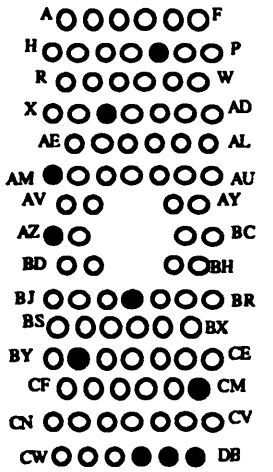
3. J.D. Kraus, *Radio Astronomy.* pp. 7-0 - 7-11, 2 ed. Cygnus-Quasar Books 1986.

Table 1. Power Requirements				
IF Module	Voltages			
	+ 5 V	+ 15 V	+ 24 V	- 15 V
RF Conv	0	170 ma	0	1.8 ma
Attn	0	0	84 ma (max)	0
Synth	1.2 A	400 ma	31.2 ma	12.6 ma
Synth Select	0	120 ma	0	0
SSB	0	92 ma	0	14 ma
Relay Tree	0	136 ma	0	0
Interfer Det	100 ma	47 ma	0	32 ma
ADC Amp	0	12 ma	0	9.6 ma
V/F LO Div	85 ma	62 ma	0	550 ma
Dig Card	1.5 A	0	0	10 ma
Power Meter	0	12 ma	0	10 ma
LCD Meter	3 ma	0	0	0
Dig Pan Meter	300 ma	0	0	0
LED's (5)	200 ma	0	0	0
Totals	3.20 A	1.06 A	0.115 A	0.630A
8 X	25.60 A	8.48 A	0.922 A	5.04 A
160 PLL	0	605 ma	0	270 ma
Dig Interface	0.800 A	0	0	0
DC Totals	26.40 A	9.09 A	0.922 A	5.31 A
DC Power	132.00 W	136.4 W	22.13 W	79.65 A
Supply eff.	45%	55%	60%	55%
AC TOTAL	293.33 W	248.00 W	36.88W	144.82 W
TOTAL POWER	723.03 W	115 ACVrms @ 6.29 A		

Table 2 DC Power Drawer Connector

90 Pin Elco

Voltage	Color	Pin Assignment
+5 V	Orange	A,B,C,D,E,F H,J,K,L
Black	+5 V Ret	N,P R,S,T,U,V,W X,Y
+15 V	Red	AA,AB,AC,AD AE,AF,AG,AH,AJ,AL
+ 15 V Ret	Black	AN,AP,AR,AS,AT,AU AV,AW,AX,AY
- 15 V	Violet	BA,BB,BC BD,BE,BF,BH BJ,BK,BL
- 15 Ret	Black	BN,BP,BR BS,BT,BU,BV,BW,BX,BY
+ 24 V	Red/White	CA,CB,CC,CD,CE CF,CH,CJ,CK,CL
+ 24 V Ret	Black	CN,CP,CR,CS,CT,CU,CV CW,CX,CY
Empty		N,Z,AM,AZ,BM,BZ,CM CZ,DA,DB



● - Empty

Table 3 SSB Downconverter Connector Assignments.

20 pin Elco (Exposed)

	Signal	Color	Pin
Power	+ 5 V	orange	A
	+ 5 V ret	black	D
	+ 15 V	red	E
	+ 15 V ret	black	J
	+ 24 V	red\white	K
	+ 24 V ret	black	L
	- 15 V	violet	M
	- 15 V ret	black	R
Address	Drawer Select A0		T
	Drawer Select A1		U
	Drawer Select A2		V
	Drawer Select A3		W
	Drawer Select Gnd		X

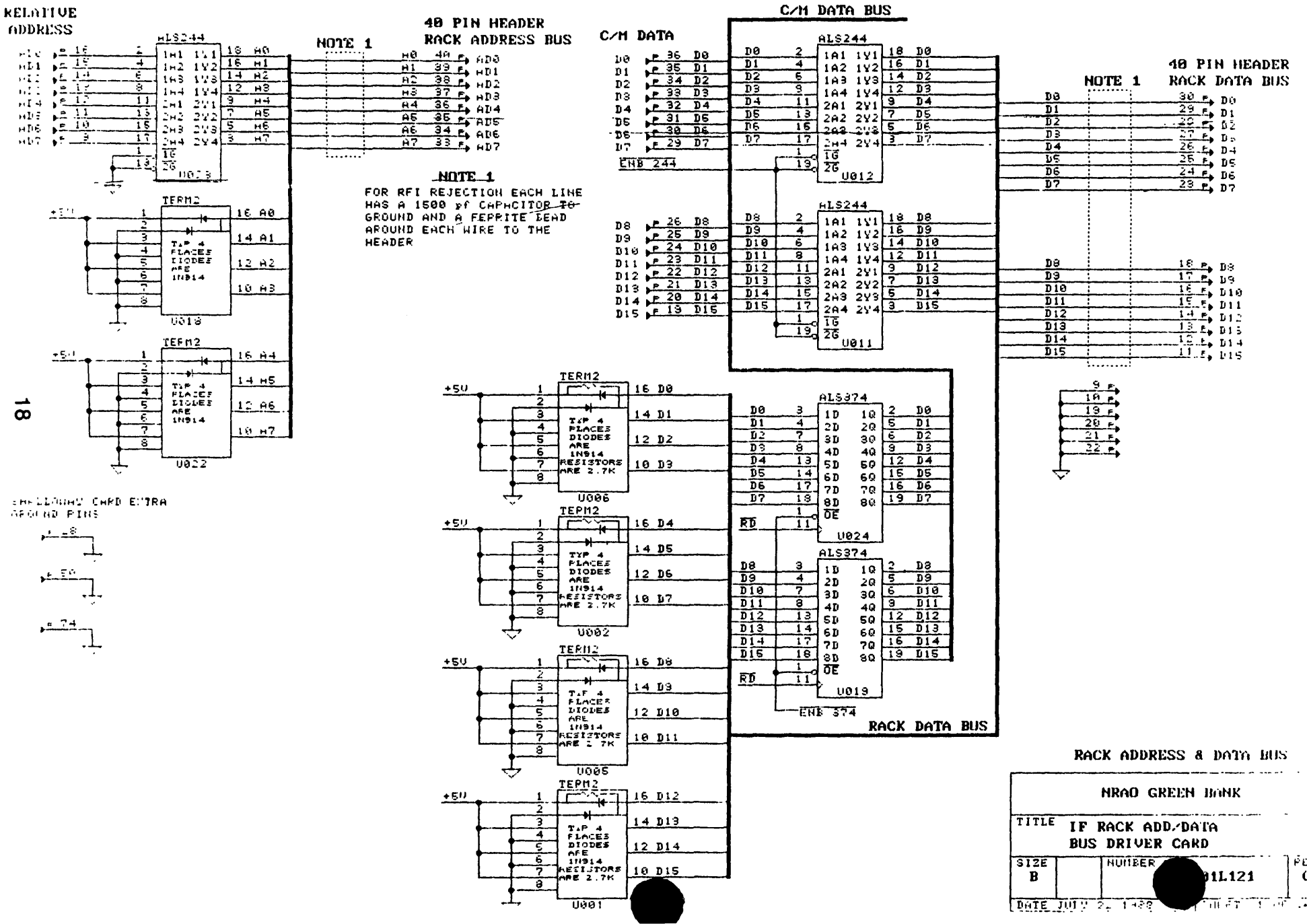
20 Pin Elco (Recessed)

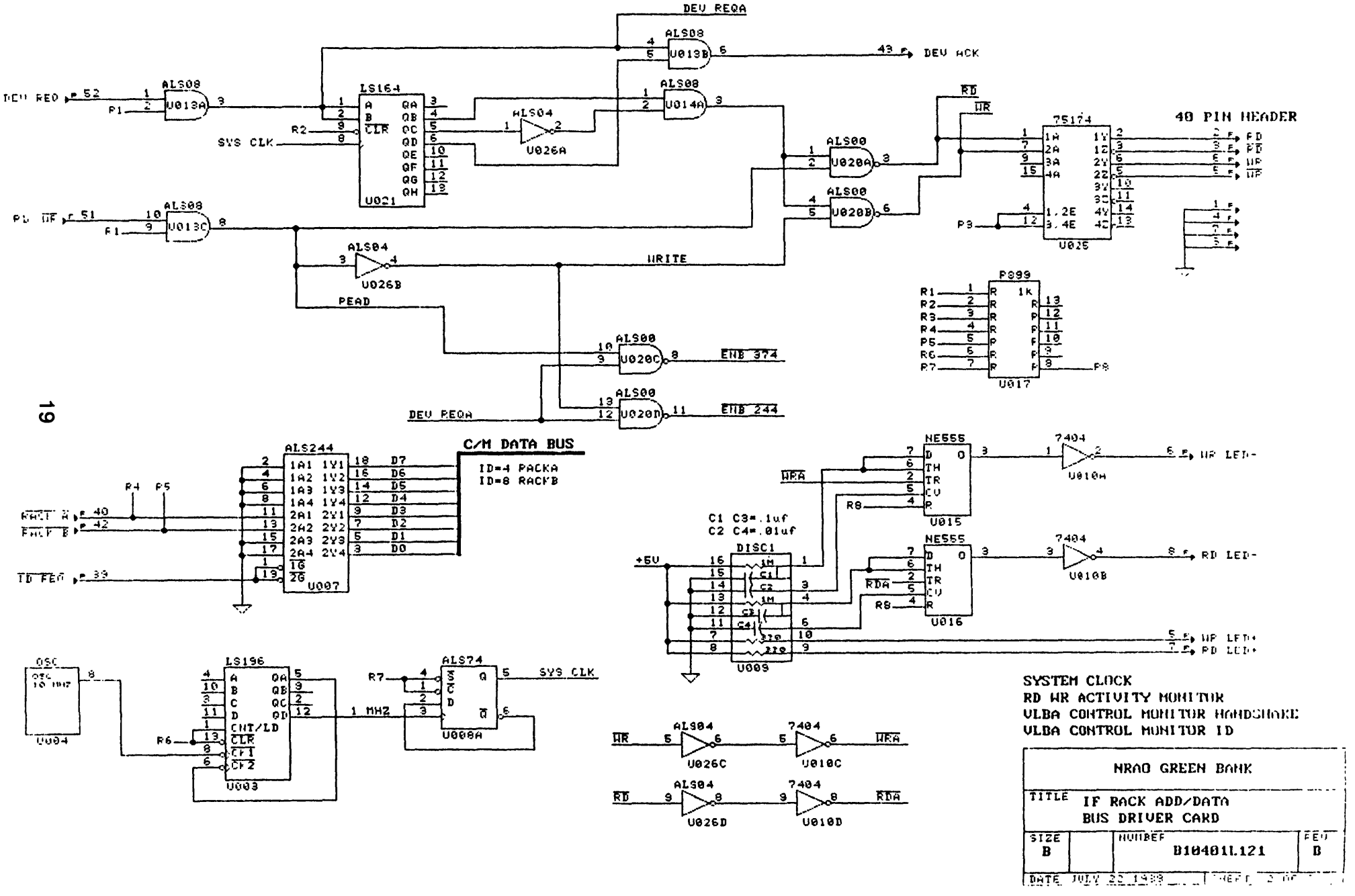
Drawer	Pins Jumpered Together
0	T,U,V,W,X
1	U,V,W,X
2	T,V,W,X
3	V,W,X
4	T,U,W,X
5	U,W,X
6	T,W,X
7	W,X

D Connector

Signal	Pin
RFIX -	3
RFIX +	7
Power Monitor Out +	4
Power Monitor Out -	8
Synth Monitor Out +	5
Synth Monitor Out -	9

Figure 5 Bus Driver Circuit Diagram.





SYSTEM CLOCK
RD WR ACTIVITY MONITOR
VLBA CONTROL MONITOR HANDSHAKE
VLBA CONTROL MONITOR ID

NRAO GREEN BANK		
TITLE: IF RACK ADD/DATA BUS DRIVER CARD		
SIZE: B	NUMBER: B104011121	REV: B
DATE: JULY 22 1988	SHEET 2 OF	

Figure 6 160 MHZ PLL Circuit Diagram.

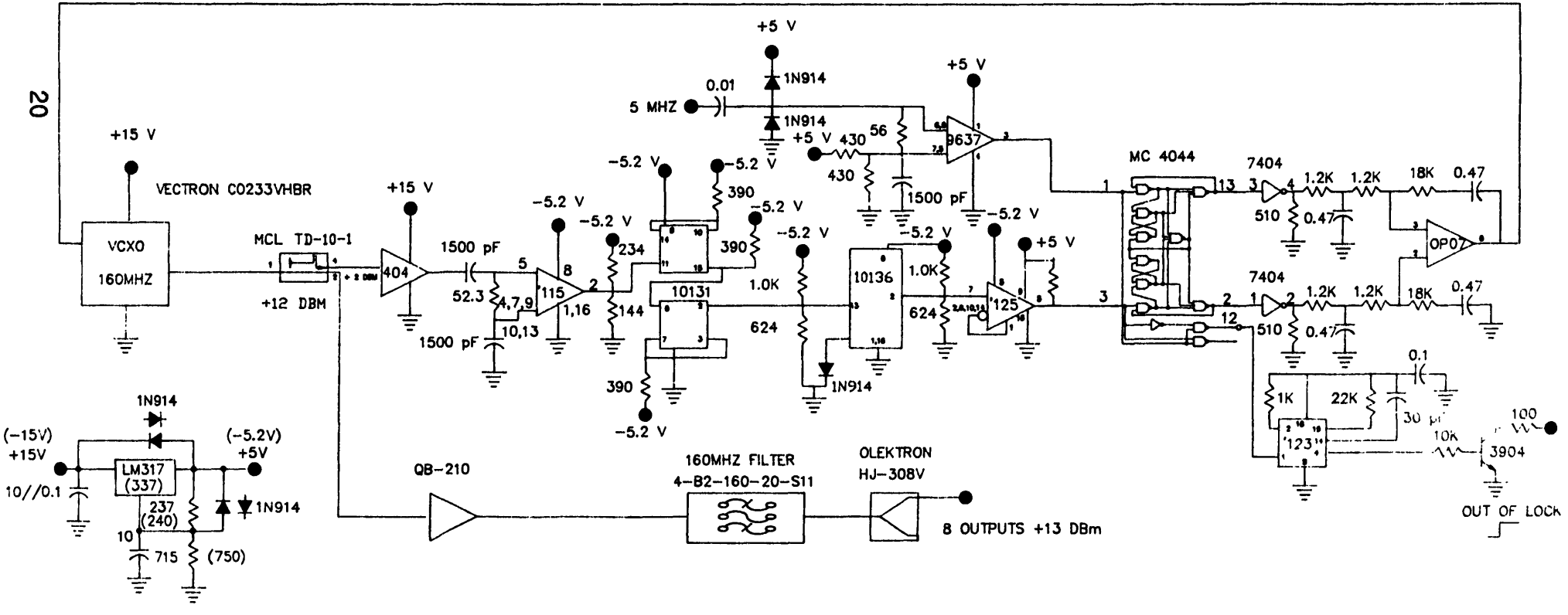


Figure 7 5 MHZ Buffer Circuit Diagram.

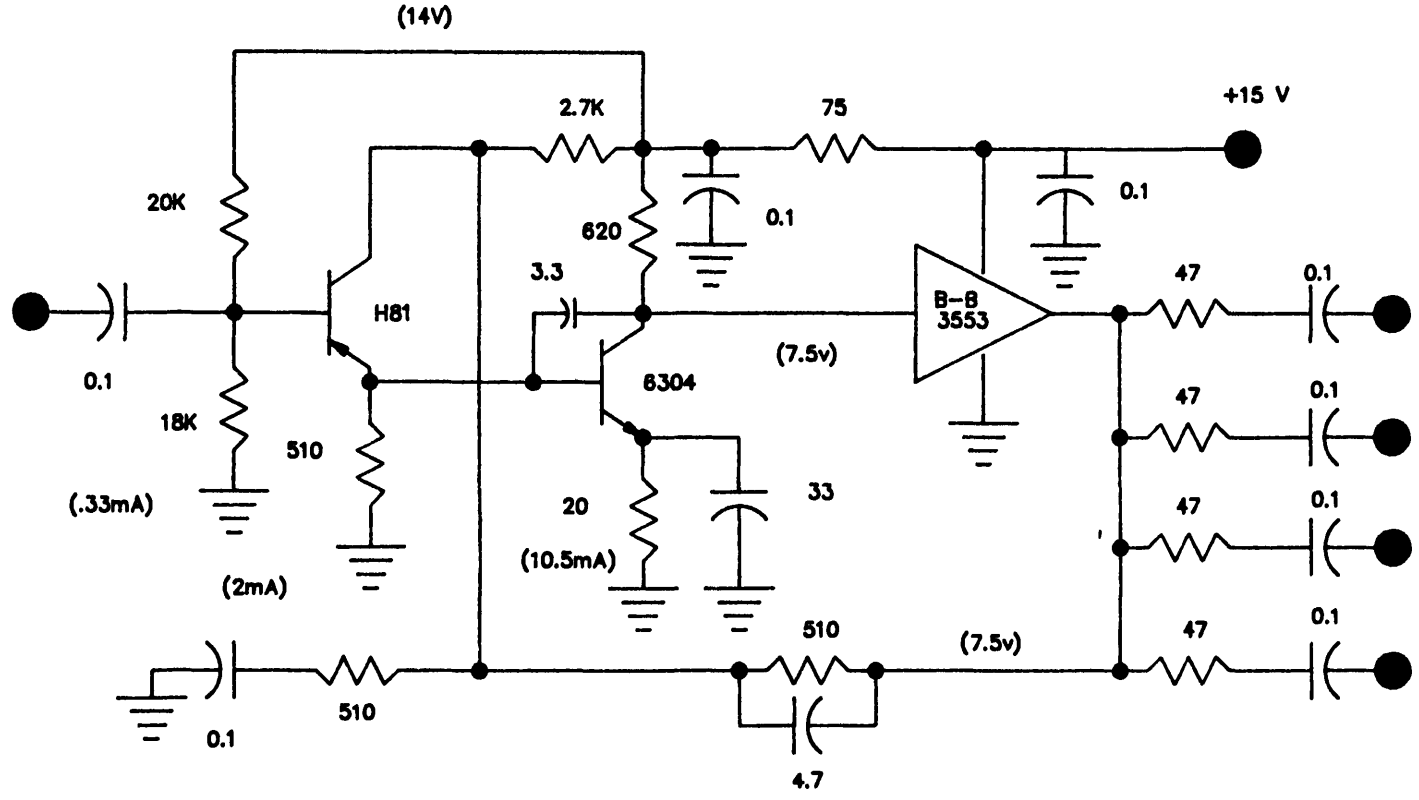


Figure 8 SSB Downconverter Block Diagram.

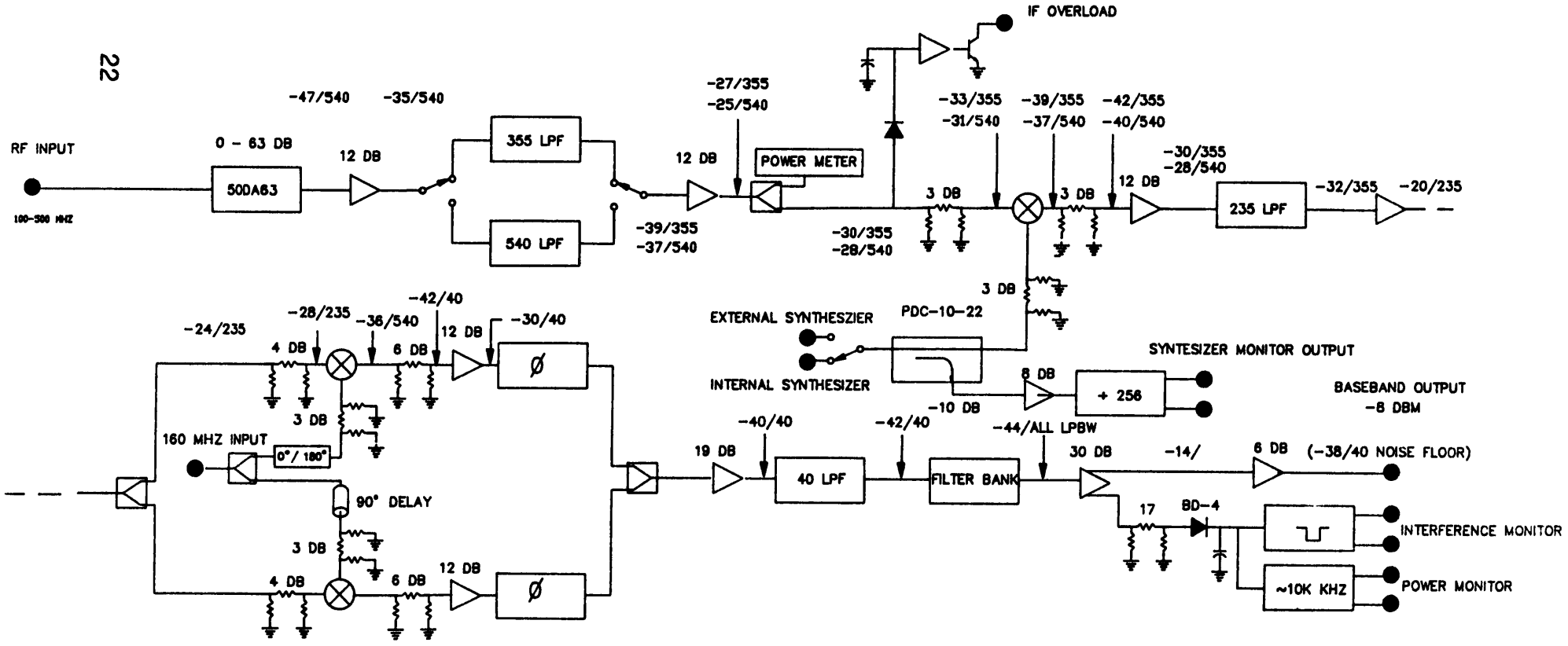


Figure 9 RF Downconverter Circuit Diagram.

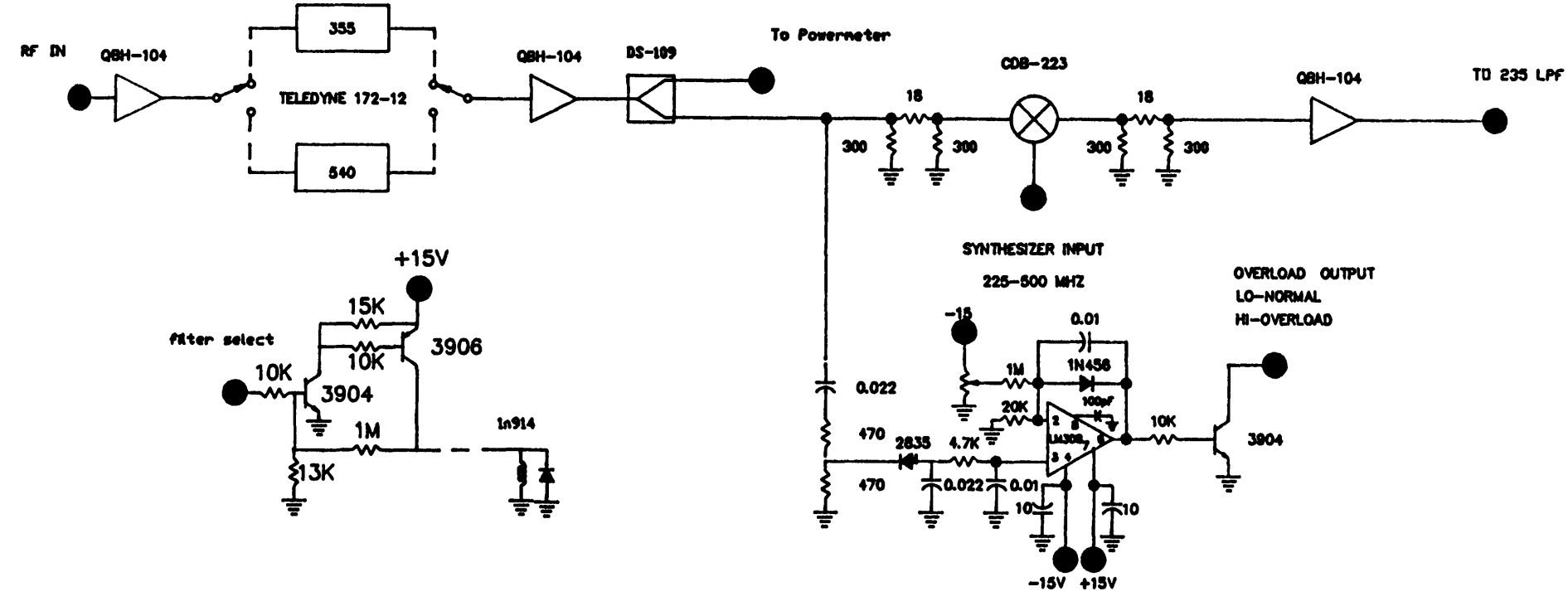


Figure 10 SSB Demodulator Circuit Diagram.

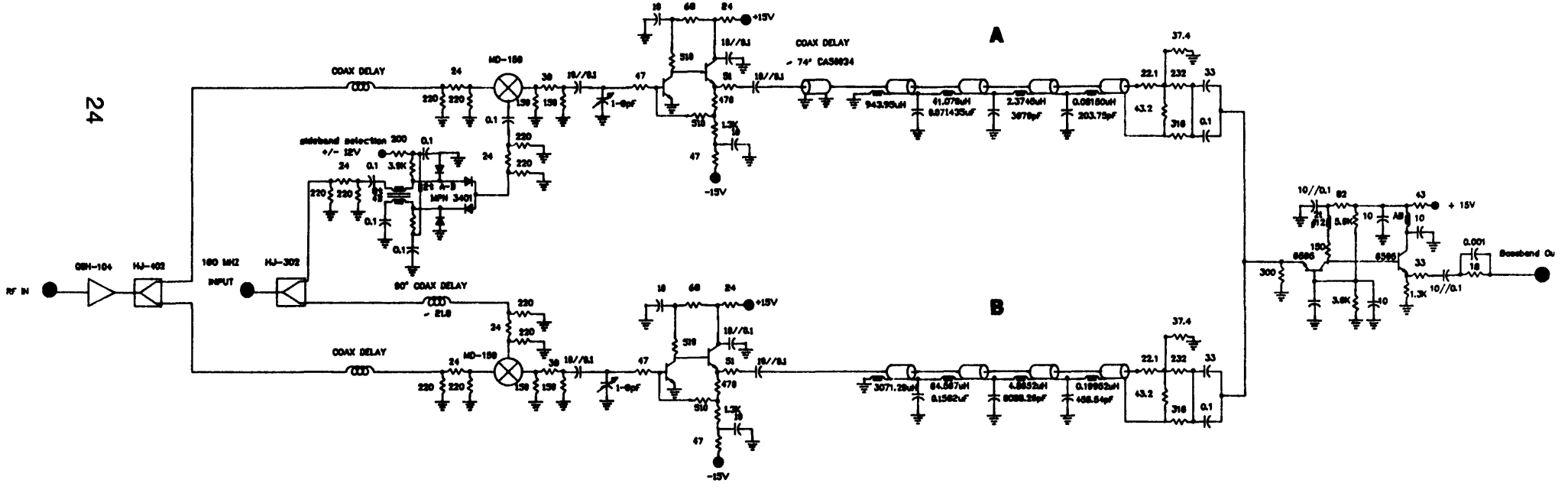


Figure 11 Filter Bank and Relay Tree Circuit Diagram.

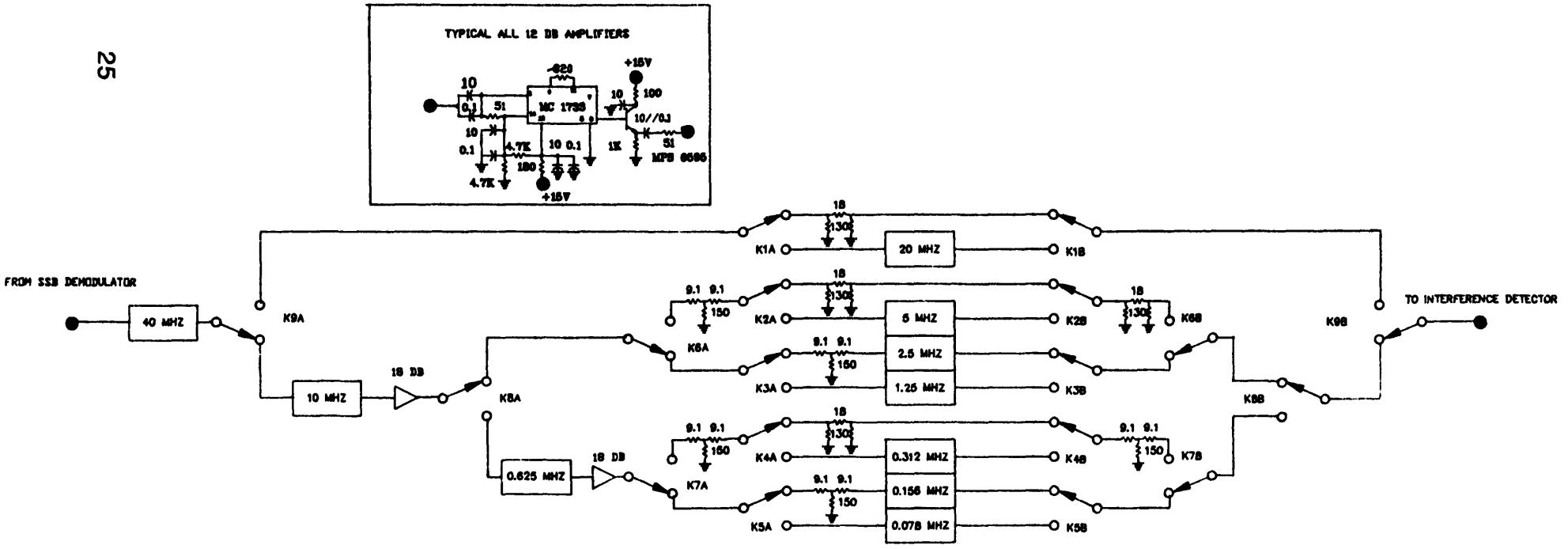


Figure 12 Interference Detector Circuit Diagram.

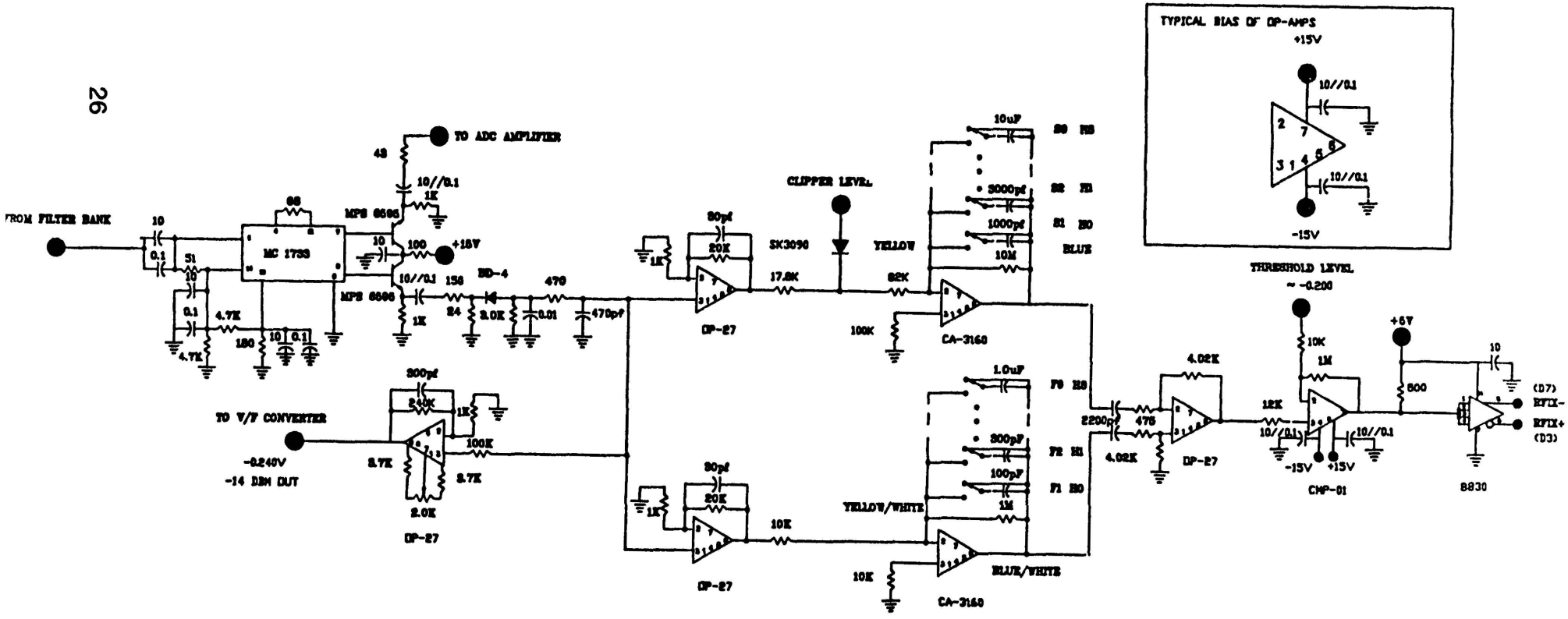


Figure 13 AD Amplifier Circuit Diagram.

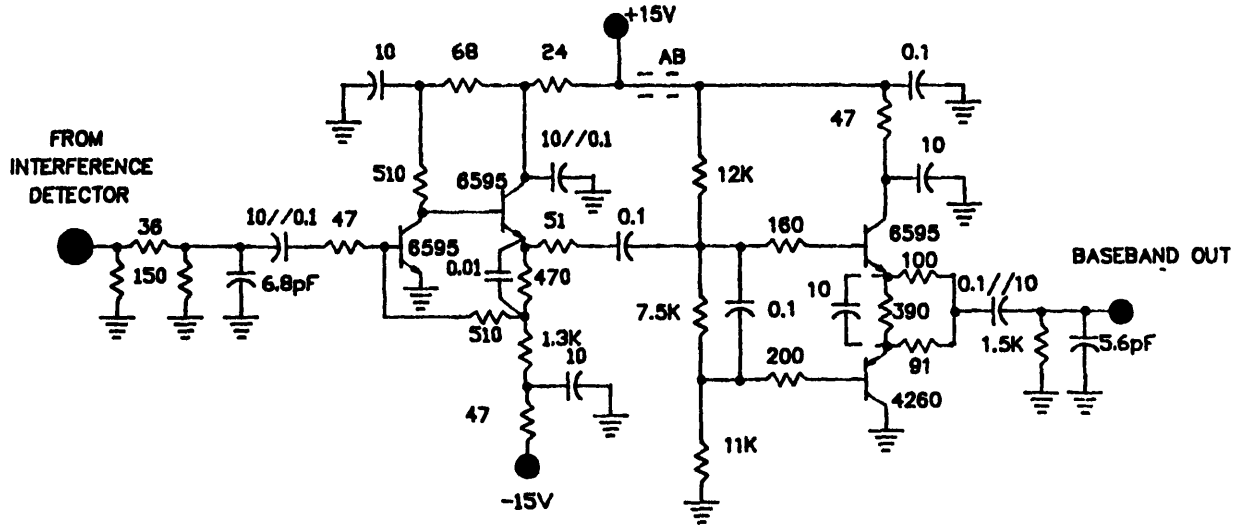


Figure 14 V/F Converter and TP Monitor Circuit Diagram.

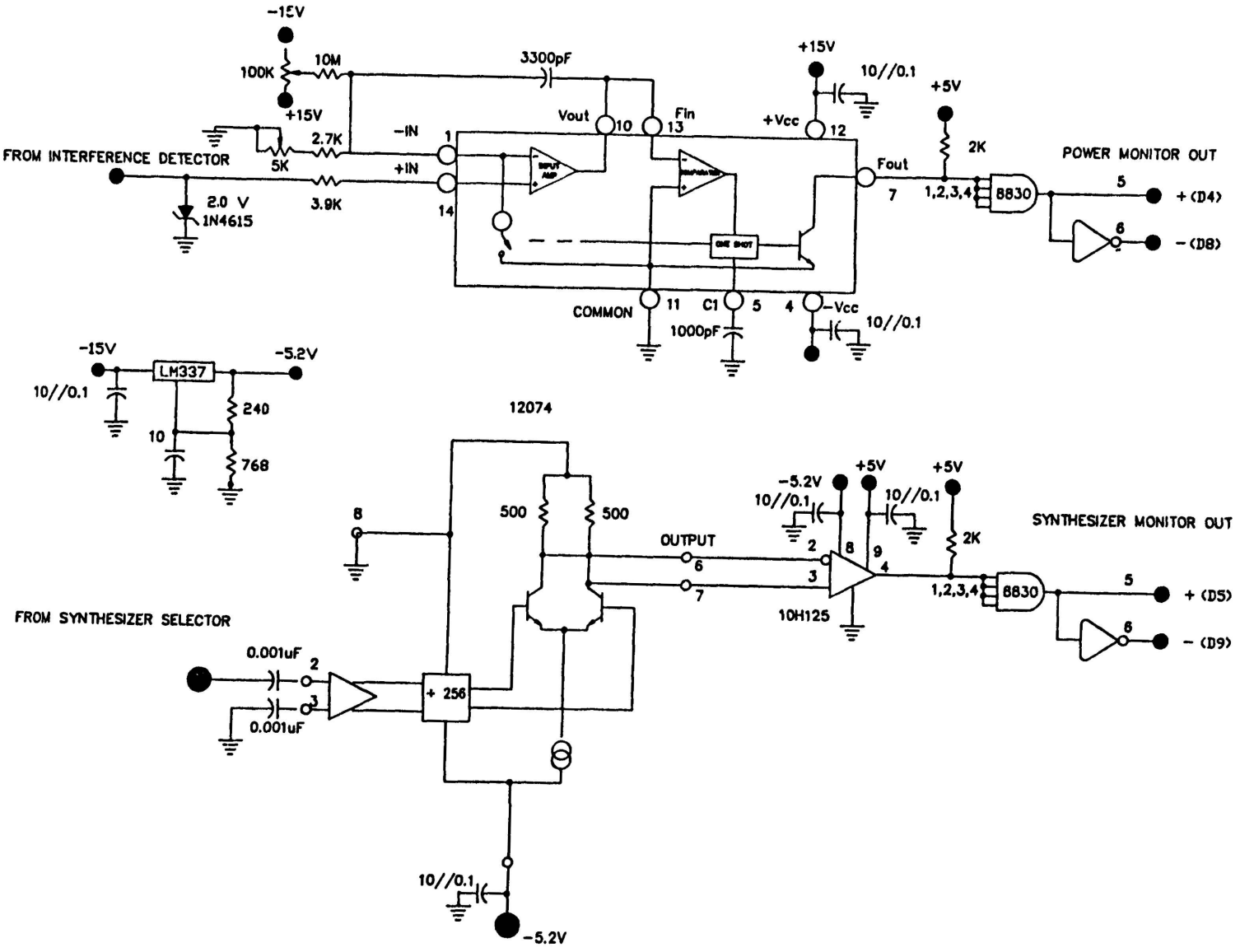


Figure 15 Logarithmic Amplifier Circuit Diagram.

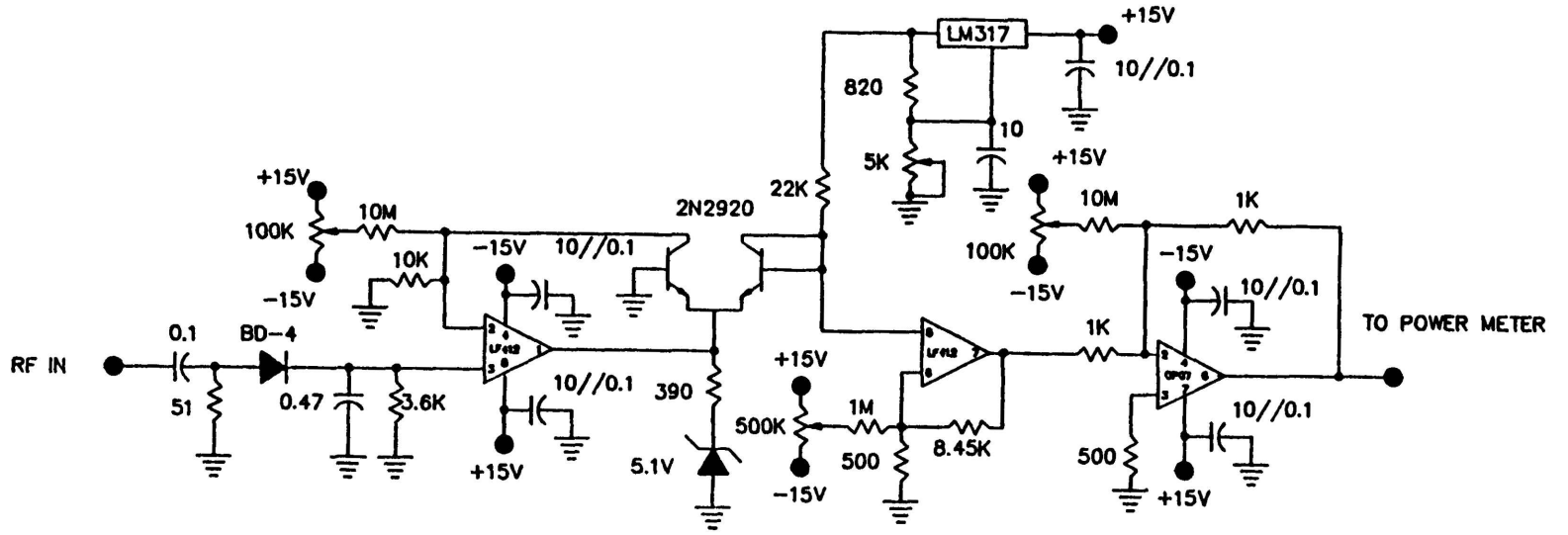


Figure 16 Synthesizer Selector Circuit Diagram.

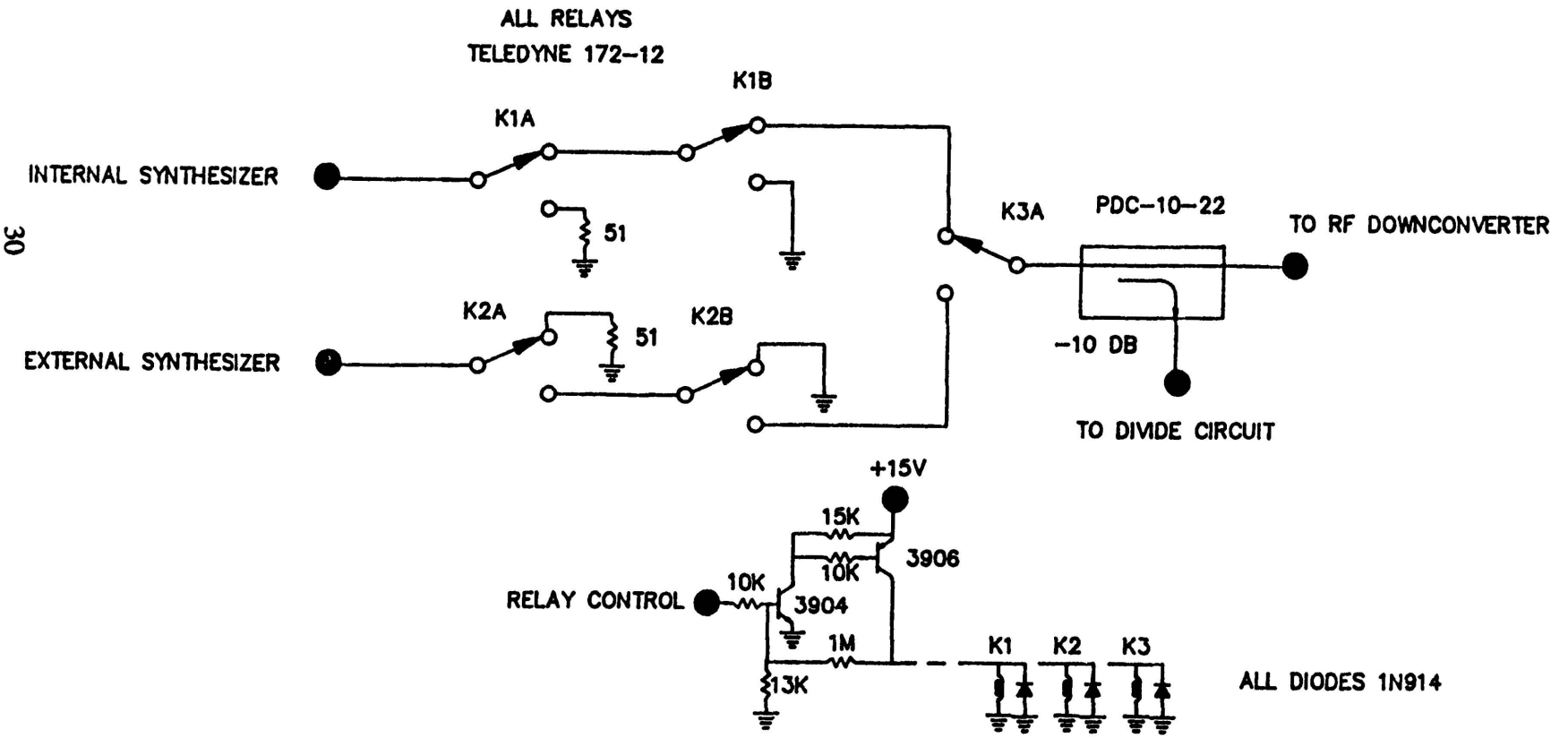


Figure 17 Synthesizer Amplifier Circuit Diagram.

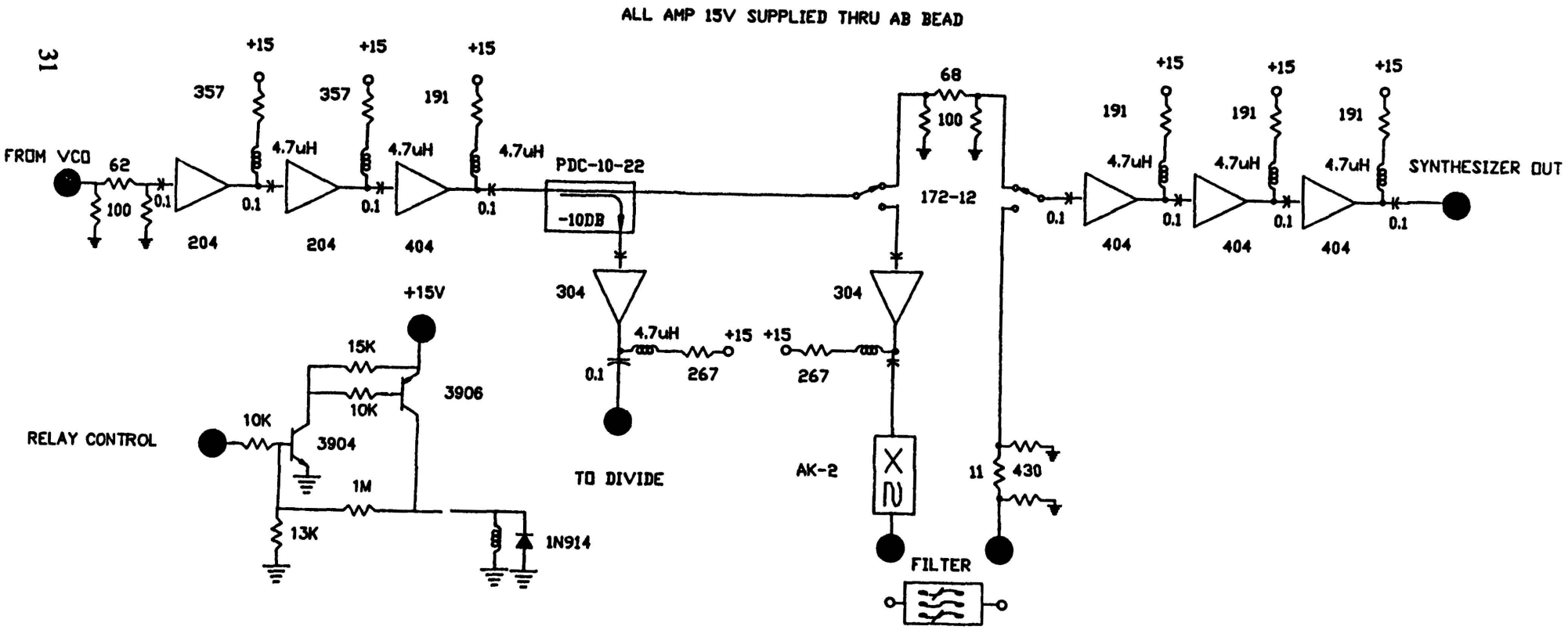
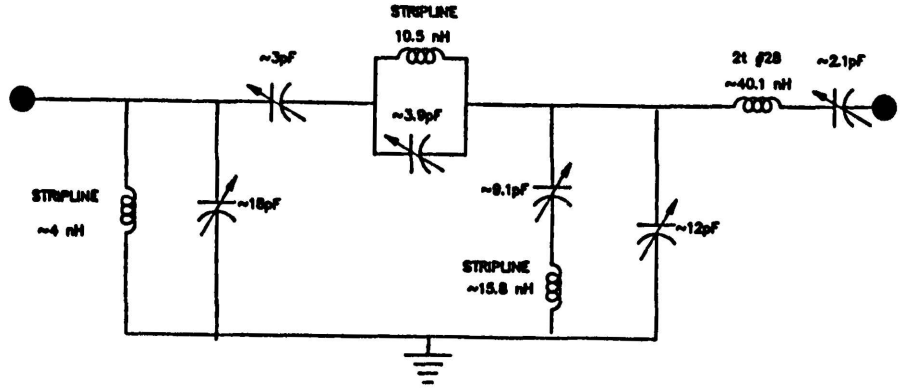


Figure 18 Elliptical Filter Circuit Diagram and Frequency Response.



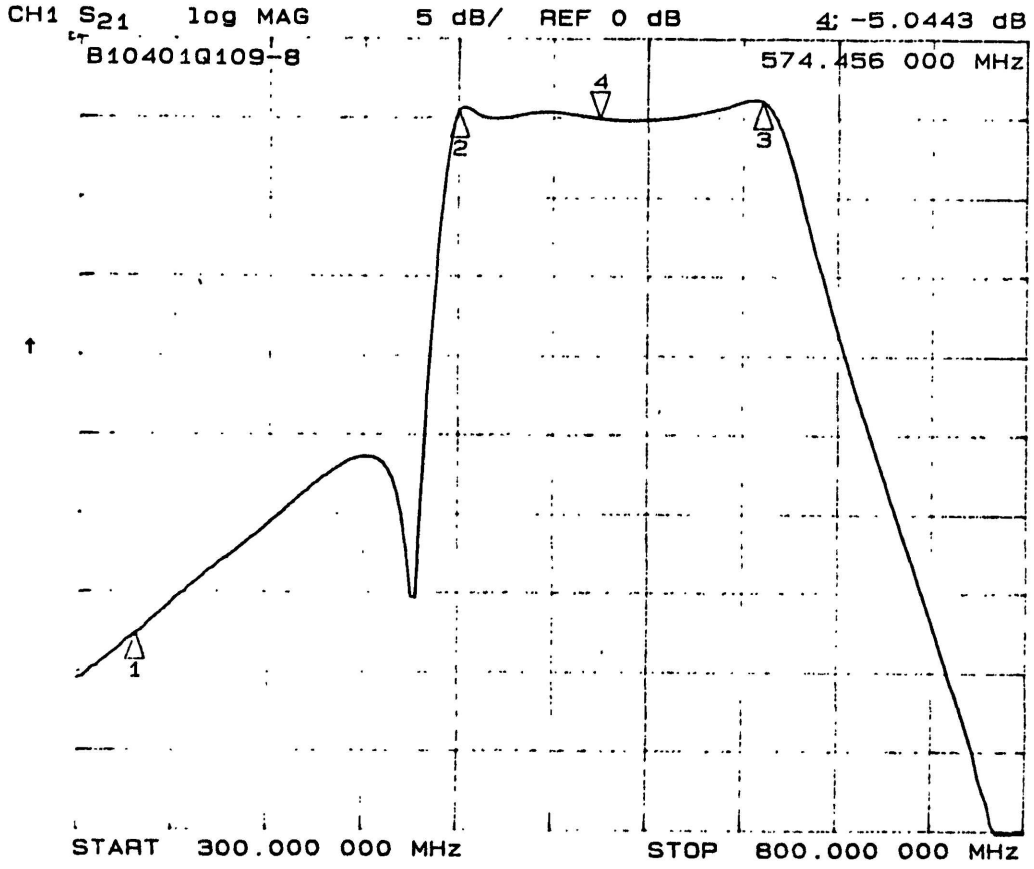
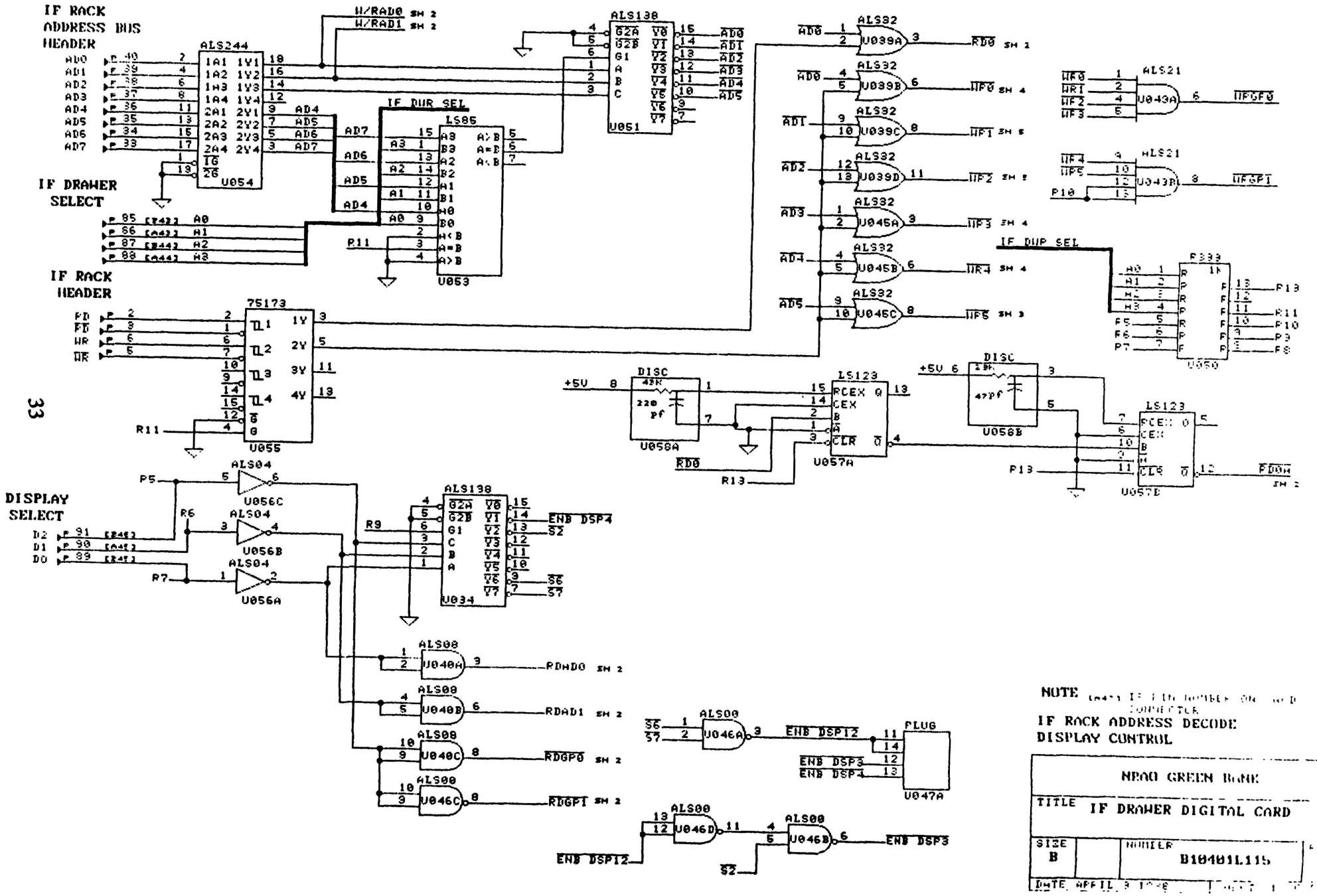
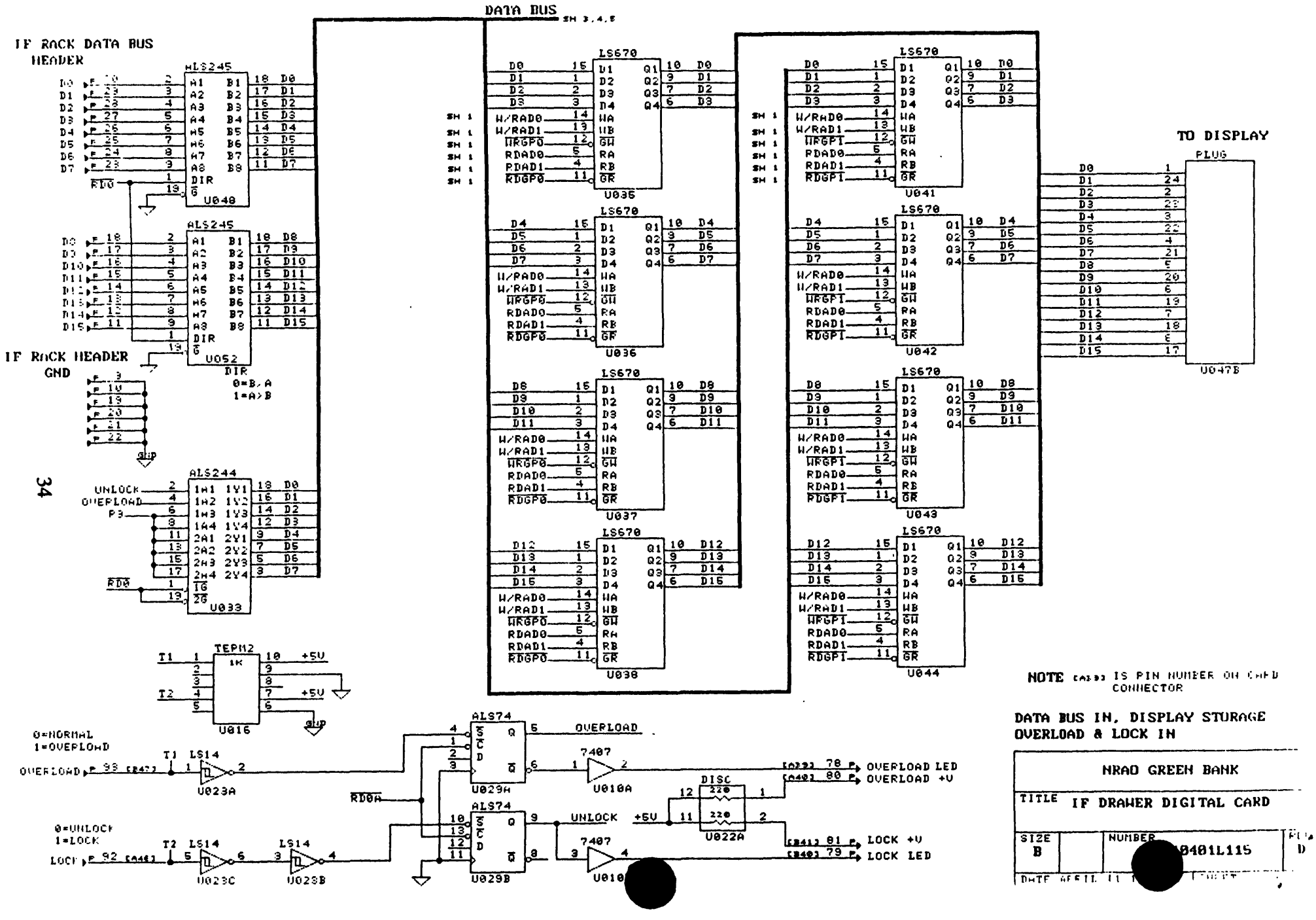
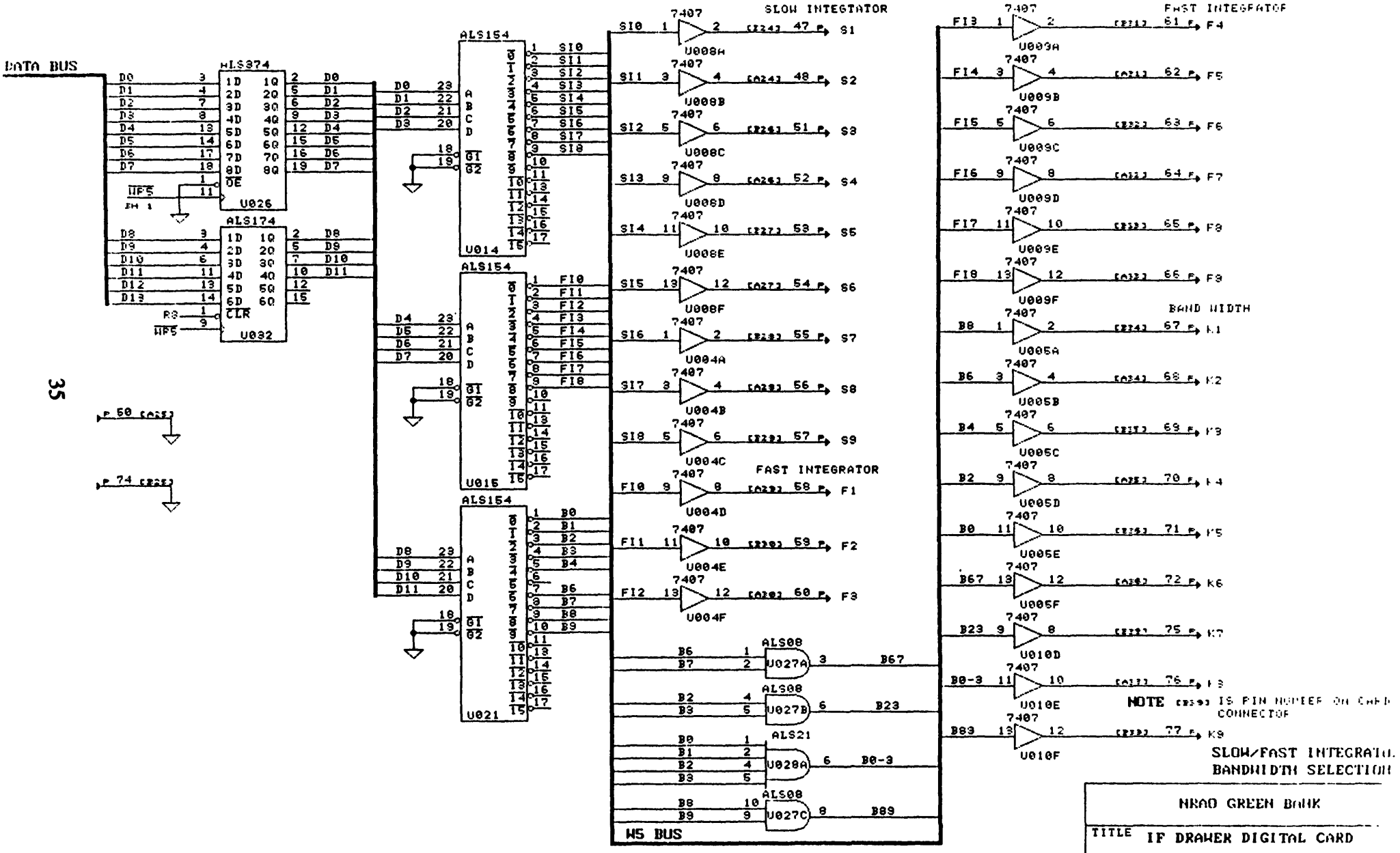
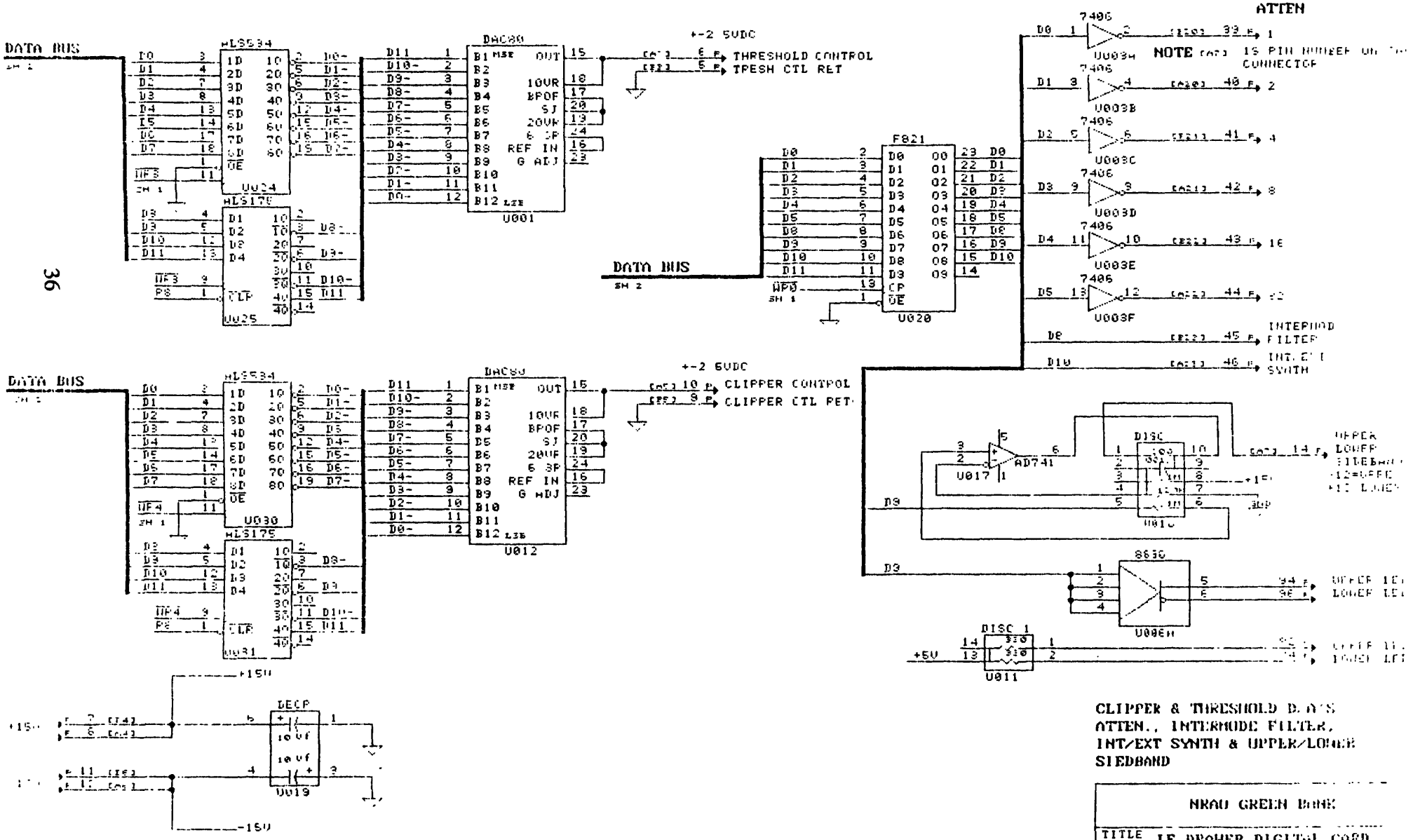


Figure 19 SSB Downcoverter Digital Card Circuit Diagram.



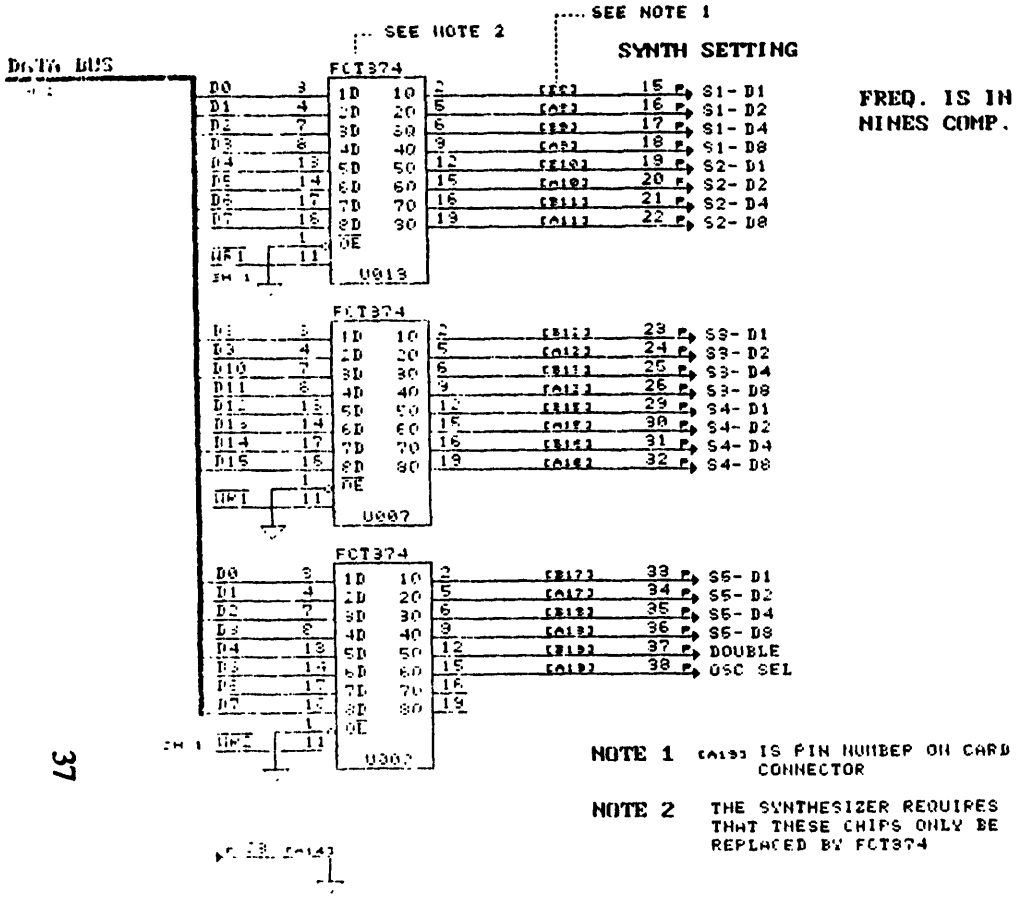

DATA BUS
IF RACK DATA BUS HEADER
HLS245
U040
ALS245
U052
IF RACK HEADER GND
0=B>A
1=A>B
ALS244
U033
TEPM2
U016
LS670
U035
U036
U037
U038
U041
U042
U043
U044
TO DISPLAY
PLUG
U047B
0=NORMAL
1=OVERLOAD
OVERLOAD
ALS74
U029A
7407
U010A
OVERLOAD LED
OVERLOAD +V
RD0A
DISC
U022A
0=UNLOCK
1=LOCK
LOCK
U023C
U023B
UNLOCK
U029B
LOCK +V
LOCK LED
NOTE (A23) IS PIN NUMBER ON CARD CONNECTOR
DATA BUS IN, DISPLAY STORAGE
OVERLOAD & LOCK IN
NRAO GREEN BANK
TITLE IF DRAWER DIGITAL CARD
SIZE B
NUMBER 0401L115
REV D


DATA BUS
ALS374
U026
ALS174
U032
ALS154
U014
U015
U021
SLOW INTEGRATOR
FAST INTEGRATOR
BAND WIDTH
7407
U008A
U008B
U008C
U008D
U008E
U008F
U004A
U004B
U004C
U004D
U004E
U004F
U009A
U009B
U009C
U009D
U009E
U009F
U005A
U005B
U005C
U005D
U005E
U005F
U010D
U010E
U010F
ALS08
U027A
U027B
U027C
ALS21
U028A
W5 BUS
NOTE (###) IS PIN NUMBER ON CARD CONNECTOR
SLOW/FAST INTEGRATOR BANDWIDTH SELECTION
NRAO GREEN BANK
TITLE IF DRAWER DIGITAL CARD
SIZE B
NUMBER B10401L115



CLIPPER & THRESHOLD D.A.C'S
ATTEN., INTERMODE FILTER,
INT/EXT SYNTH & UPPER/LOWER
SIDEBAND

	NRAO GREEN BANK
TITLE	IF DRAWER DIGITAL CARD
SIZE B	[illegible] 1011L115



FREQ. IS IN NINES COMP.

NOTE 1 (A19) IS PIN NUMBER ON CARD CONNECTOR

NOTE 2 THE SYNTHESIZER REQUIRES THAT THESE CHIPS ONLY BE REPLACED BY FCT374

FREQUENCY SYNTH. CONTROL

NRAO GREEN BANK			
TITLE: IF DRAWER DIGITAL CARD			
SIZE: B		NUMBER: B1E4011.115	REV: D
DATE: WEEK 15 19[illegible]			