Digital Transmission System Signaling Protocol

EVLA Memorandum No. 33

Version 3

1 version of "Digital Transmission System Signaling Protocol",
Written by Robert W. Freund, September 25, 2000.

Prepared by Steven Durand
November, 2001

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1. ABSTRACT

Built on the infrastructure of the current VLA, including its twenty-seven, 25-meter diameter antennas, the EVLA project will install new electronics and fiber optics to enhance the VLA performance. The current receiver plan specifies the simultaneous reception of two pair of orthogonally polarized IF signals. The four IF signals will be digitized at the antenna and transmitted through a fiber optic system to the central control building. Each receiver-IF will provide an instantaneous bandwidth of 4 GHz per polarization, partitioned into two 2 GHz wide sub-bands by the IF system, for a total of eight sub-bands. Each sub-band is harmonically sampled at 4 GHz, and quantized to 3 bits. This produces three synchronized high-speed serial optical fiber transmission channels per polarization and a total of 12 channels per antenna. The data is formatted into 160-bit frames and transmitted at 10 Gbits/second/channel. The frame consists of a sync word, a sequence word, a time stamps, the payload, and a checksum. Modulo-2 addition with a specific pattern scrambles the frame information to provide timing information and minimizes the low frequency content. End–of–life error rates of less than 10^{-6} are required. This EVLA memo is based on a NRAO memo "Digital Transmission System Signaling Protocol", written by Robert W. Freund, 2000 September 25 for the ALMA project.

2. INTRODUCTION

The EVLA IF Digital Transmission System (DTS) uses a format similar to the ALMA project, [1]. The IF DTS samples two pair of IF polarizations at each antenna and transmits the data to a centrally located correlator. There are eight 4-GHz, 3-bit IF digitizers, two per IF signal polarization. The formatter adds a header and reconfigures the data into 12 output channels that are transmitted at 10 Gbits/second and Dense Wavelength Division Multiplexed (DWDM) on to a single fiber.

The serial protocol requirements for the DTS were derived from the end-of-life bit error rate required to support good astronomy. Typically the minimum bit error rate for good astronomy is 10^{-4} divided by the number of bits in the sync word. The EVLA sync word is 10 bits long, thus the minimum bit error rate for good science is about 10^{-5}. Since there are three serial optical channels per IF polarization and 4 polarizations per antenna, each channel must also provide enough multi-channel synchronization to recreate the original data. Each channel also has a number of bits for parity, and time codes.

The intent of this memo is to describe the format each optical channel. No attempt is made to describe a detailed hardware design. However, the initial design was formulated considering the required hardware. Therefore, example block diagrams of representative hardware are used throughout to illustrate the design.

3. SYSTEM CONFIGURATION

Figure 1 shows a conceptual diagram for the signal data paths from an antenna to the lasers. The receivers will simultaneous provide of two pair of orthogonally polarized signals. Each receiver-IF provides an instantaneous bandwidth of over 8 GHz which is partitioned into two 2 GHz wide partitions per polarization by the IF system. Both partitions are harmonically sampled at 4 GHz, and quantized to 3 bits. This produces a data stream of 24 Gbits/second per IF polarization, (two 3-bit samplers operating at 4 Gbits).

The digitizers incorporate a de-multiplexer that reduces the clocking rate while increasing the number of bits. The output of each de-multiplexer is a 48-bit wide parallel output word clocked at a 125 MHz rate. When two de-multiplexers are paired together, the parallel word to each formatter is 48 bits clocked at 250 MHz, an aggregate of 12 Gbits/s. This corresponds to a 24 Gbits/second data rate per IF polarization.

At each antenna, the DTS will sample four IF polarizations. The data from each polarization is formatted into three data streams. The 2^0-bits are placed on one fiber, the 2^1-bits are placed on the second fiber, and the 2^2-bits are placed on third fiber. The total formatted data rate is 30 Gbits/s per base band and 120 Gbits/second per antenna.

At the control building, the de-formatter will supply a 192-bit wide word clocked at 125 MHz to the correlator. This requires exact synchronization across all optical and electrical components within the DTS. The DTS will compensate for changes in the optical fiber propagation times due to variations in environmental factors. With skew and propagation effects eliminated, correct timing sequence is maintained from every digitizer to the correlator.

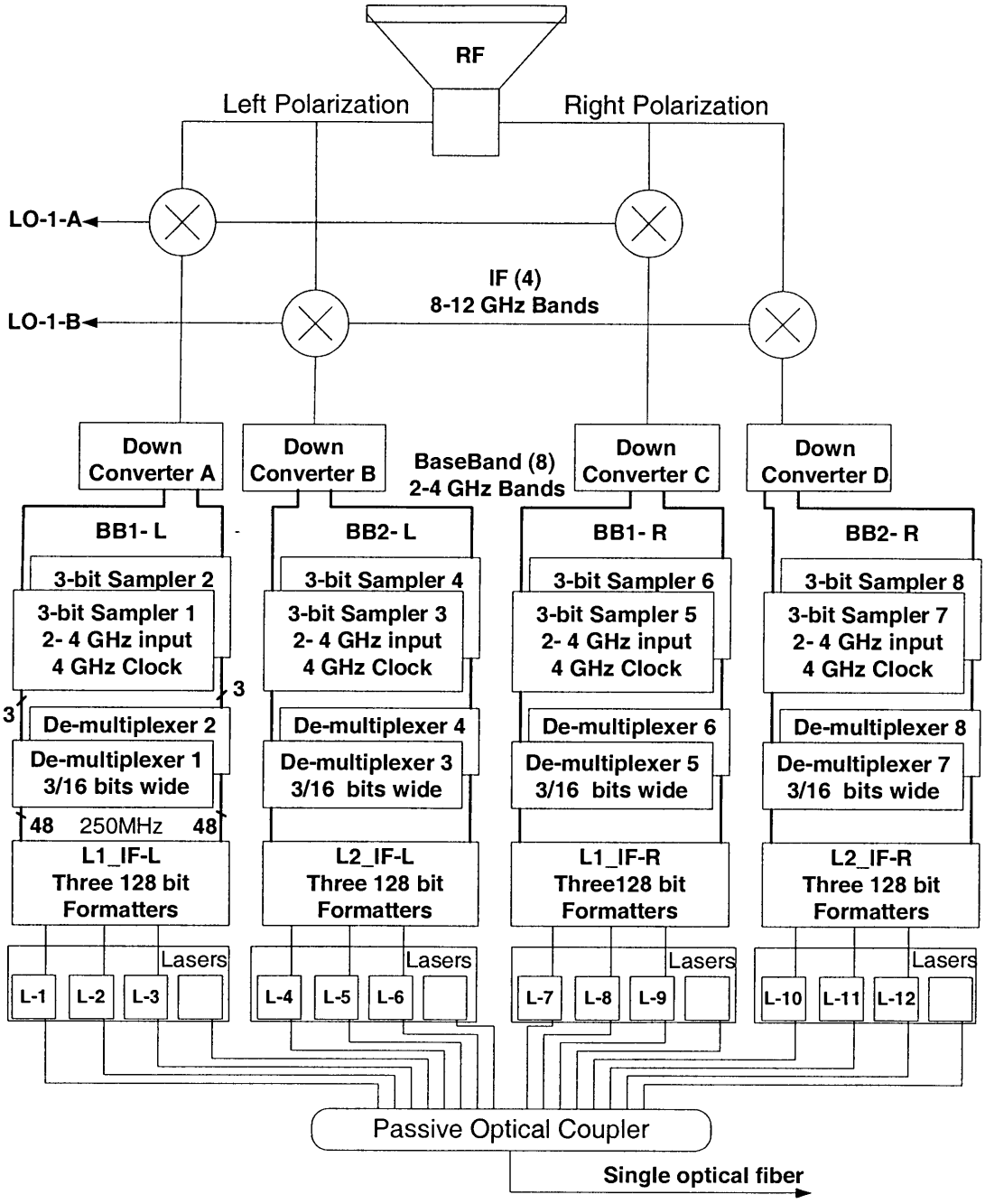

Figure 1 Conceptual Diagram

4. DESIGN CONSIDERATIONS

The fiber optic industry is being asked by the telecommunication industry to supply economical fiber optic components to support upcoming high-speed systems. To provide compatibility between multiple vendors standards for these upcoming systems have been developed. One such standard is SONET OC-192, which describes the payload and transport overhead characteristics of an amplitude modulated optical carrier transported on fiber at a signaling rate of 9.95328 Gbits/second. For the EVLA, the signaling rate was increased to 10 Gbits/second. The payload of 24 Gbits/second per IF polarization is distributed between three optical parallel channels. Because the 10 Gbits/second channel signaling rate is faster than the required 8 Gbits/second to transmit the data, the remaining bits are used for format and error checking. Sixteen additional bits are added to every 64 data bits to produce an 80-bit word. Figure 2 shows the 160-bit frame. The frame is composed of a divided 10-bit sync word, 1-bit meta-frame index, a 5-bit sequence count, a 1PPS bit, a 1 pulse per 10 second bit, a data valid bit, 5 non dedicated bits, a 8-bit checksum. The first 4 payload bits are carried in locations 12 through 19 with the remaining 124 contiguous bits beginning with the bit location 20.

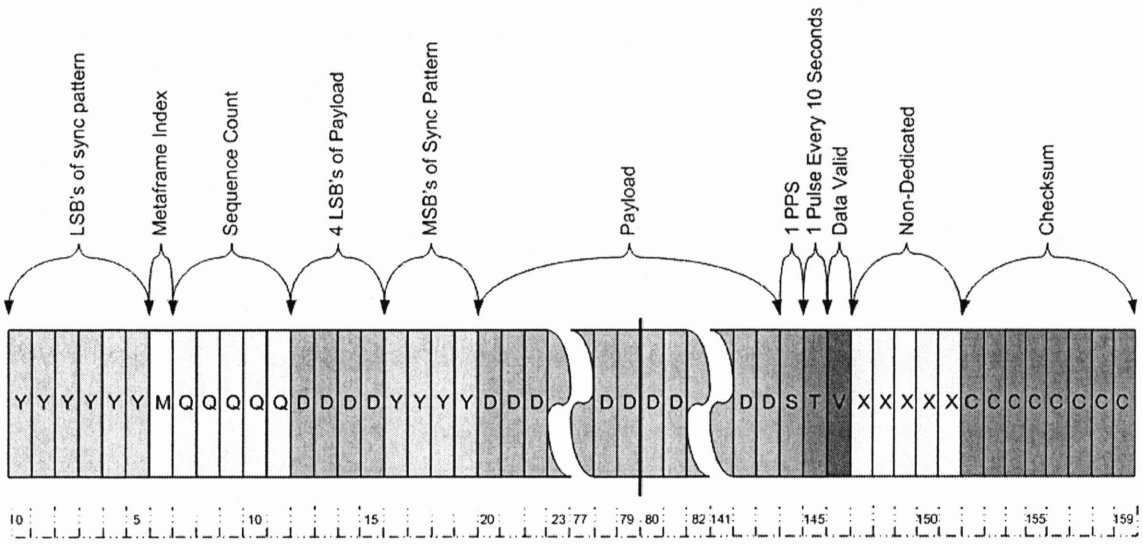

Figure 2. EVLA Frame

Channel coding is used to modify each 10 Gbits/second optical channel to facilitate proper reception. Channel coding provides better timing information and minimizes low frequency content. The EVLA uses a channel coding technique that produces almost an equal number of ones and zeros per frame. This not only reduces systematic jitter but also minimizes the low frequency content.

5. EVLA FRAME IMPLEMENTATION

The 250 MHz to 10 GHz rate conversions produces a natural 80 bit wide word. This word consists of 16 format bits and 64 data bits. Two consecutive 80-bit words are combined to produce a 160-bit frame. The 160-bit frame is produced at an effective 62.5 MHz clock rate and time division multiplexed by 160. To maintain the order of the frame a 16-bit partitioning and re-ordering circuit is used. It is placed between the input selector and the two 5:1 output multiplexers inside the formatter chip. This re-ordering is necessary to correct for the shuffling of the output selector.

A simplified formatter block diagram showing a 32-bit input bus, input selector, partition and re-ordering circuit, the addition 16 overhead bits, the times 5 multiplexers, the output selector and the final times 16 multiplexer is shown in Figure 3. Sixteen overhead bits are associated with each 64 data bit group. These bits are used for frame and Meta-frame synchronization, timing bits and transmission of the checksum word.

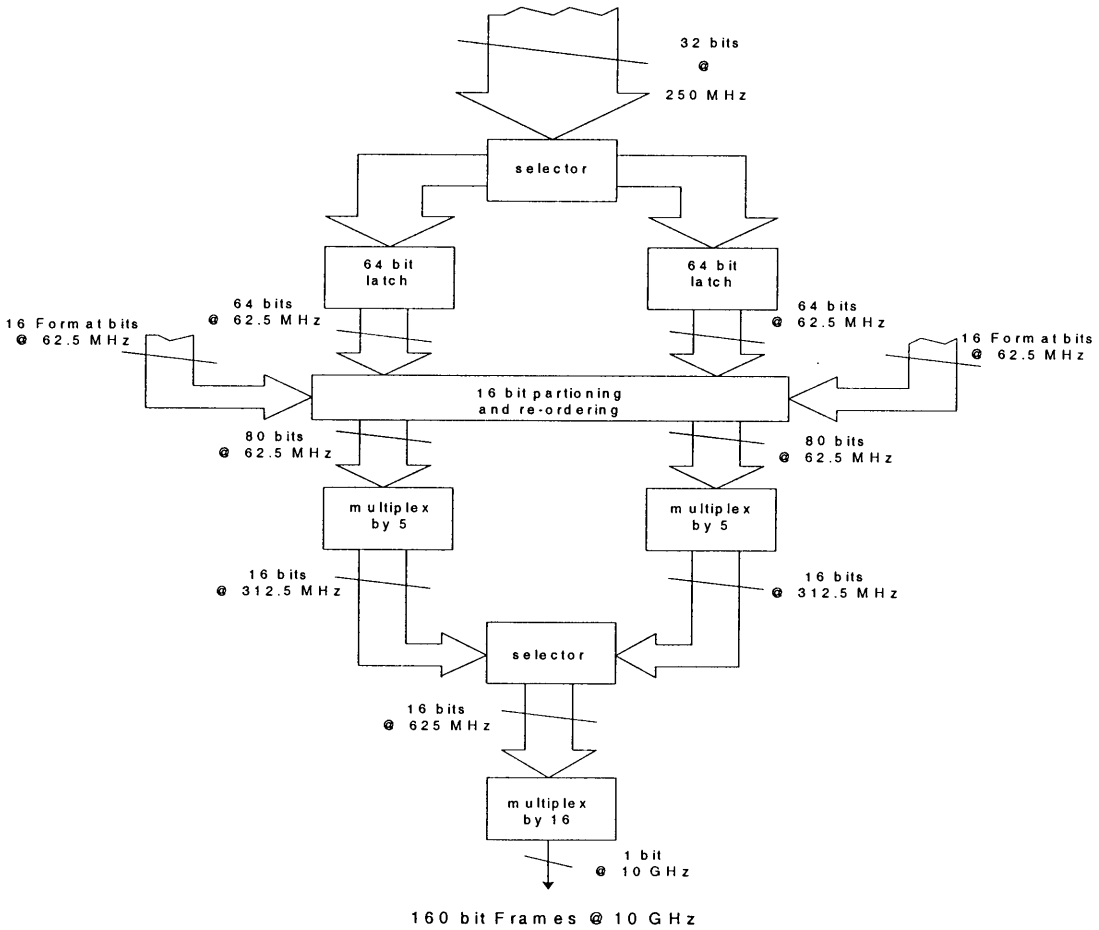

Figure 3 Simplified Formatter Block Diagram

6. FRAME SYNCHRONIZATION

The sync word pattern is located at the same location in each frame although it is divided into two separate locations. The sync word is composed of ten bits of a unique pattern. The selected 10-bit pattern is similar to the seven-bit Barker sequence (binary 0100111). The order of the pattern is not important.

As with the transmitter, the receiver implementation utilizes a 16-bit wide data selector. This data selector follows the high-speed 1 to 16 de-multiplexer and shuffles the incoming 16-bit words. By partitioning the sync word, it is possible to correctly locate the beginning of a frame and determine the data shuffling. The location of the first six bits of the sync word corresponds to the least significant bits of the 160-bit frame.

Frame synchronization moves through three stages: the search stage, the check stage and the monitoring stage. A 160-bit candidate frame is selected from the incoming serial bit stream. The ten sync location bits are checked for the pattern. If unsuccessful, a subsequent frame delayed by one bit time is selected and the comparison repeated. This process of changing the frame selection delay and sync pattern comparison repeats until a candidate frame is located. If no delay produces a match, the alternate shuffled possibility is checked according to the same algorithm. The matching criterion for the pattern comparison requires that all ten bits must match.

Once a candidate frame is located, the synchronization process enters the check stage. With a fixed pattern of only ten bits in length, it is possible to correctly detect the sync pattern in a data stream; thus, "false" sync detection is likely. The presence of the check stage is needed to improve the accuracy of detecting the true sync pattern. At least seven out-of-eight frame sync patterns must successfully identify that the true frame has been located. The possibility of a transmission bit error must be permitted. If this procedure fails, the system returns to the search phase and begins a new search.

In the monitoring stage, the system continually monitors the sync pattern for sync errors. If sync error is detected in two sequential frames or if an error is detected in two or more of eight sequential frames the system will return to the search stage. The search begins as soon as an sync error has been detected. In any situation where the search stage is re-entered, the search begins from the current shift value and not from a zero shift.

7. Meta-frame Implementation

To maintain frame concurrence across the three optical channels used to transmit each IF polarization, the formatter inserts an identical incrementing count into each frame. This count is extracted by the three optical receivers, compared, and delays applied to the early arriving channels. The result is three simultaneously clocked 160-bit frames with the identical incrementing count. Therefore, the received word will be identical to the transmitted word.

Together with the Metaframe index, the sequence number creates a large virtual frame or meta-frame. The duration in time of the meta-frame is larger than the largest expected propagation time differences between channels. These differences arise due to inherent fiber characteristics and variations in dispersion and group delay with environment. Representative dispersion values for the Conventional band (C band: 1530 nm - 1565 nm) of single mode optical fiber optimized for use in Dense Wavelength Division Multiplexing (DWDM) applications are about 16 ps/nm/km to 18 ps/nm/km [3]. With 25 km of fiber, and assuming a worst-case situation of two optical carriers separated by the maximum of 24 nm (the reddest red to the bluest blue), this only amounts to 2.4 ns (24 bit times). The maximum calculated delay is about 10.1 ns (101 bits). These values scale linearly with distance. For the assumed distance and fiber types, a Meta-frame consisting of two 160-bit frames would be satisfactory. This implementation sets the Meta-frame size to two frames.

8. DATA INTEGRITY

The intrinsic bit error rate of the electro-optical components in the fiber transmission system is expected to be extremely low. However, in addition to the laser diode source, high-speed modulator, photo-diode detector, AGC amplifier, and the clock and data recovery electronics associated with each channel, the EVLA system also includes a large number of manually re-configurable optical fibers and connectors. With each individual channel comprised of a number of complex high-speed components and multiple fiber segments, the need for continuous performance monitoring is obvious.

Eight bits of each frame are used as a checksum of the previous 152 bits. This method detects all odd numbers of errors introduced in each 19-bit group.

9. SCRAMBLING

Channel coding is the process of modifying the source data stream to facilitate proper reception. The source is composed of both payload information, whose characteristics are known only in a statistical sense, and overhead information. The sync pattern and sequence count parameters of the overhead are known, but not the other overhead bits. Thus channel coding is essential to provide adequate timing and to minimize low frequency content of each frame. Sufficient timing information is necessary to permit regeneration of the original data and to ensure low systematic jitter [2]. Data recovery and symbol timing is determined by a phase locked loop system operating on the high-speed channel data stream. It requires sufficient transitions per reciprocal loop bandwidth to properly operate. More data transitions produce less jitter and lower recovered bit error rates due to clock extraction timing errors.

Low frequency content should be minimized to maintain low bit error rates. An equal numbers of ones and zeros produce a balanced signal with minimal low frequency content. This is important in AC coupled systems.

Frame Synchronous Scrambling (FSS) will be is used in the EVLA to provide adequate timing and to minimize low frequency content. The entire frame, except for the ten sync bits, will be scrambled by a static random pattern. A selected scrambling pattern is added modulo 2 to the remaining bits of the frame with the first generated scrambling bit added to the eighth frame bit. A Shift Register Generator (SRG) produces the scrambling pattern and the pattern "runs" continuously throughout the 153 bits of the pattern. A seven stage SRG producing a 127-bit length sequence is used. The 153-bit pattern produced with a generator polynomial of 1 + X^6 + X^7 and a seed or initial value of hexadecimal 46 has the required randomness properties [4]. The scrambling pattern has 77 ones and 76 zeros achieving almost perfect DC balance. Table 2 shows the run length distribution of ones and zeros.

Run length	Number of Ones	Number of Zeros
1	19	20
2	11	10
3	5	6
4	2	2
5	1	1
6	0	1
7	1	0

Table 2, Run length distribution of ones and zeros for 153-bit scramble pattern.

Table 2 also indicates the small amount of low frequency content in the pattern. The pattern has a total of only 4 runs of length greater than 4 bits with the longest one being only 7 bits. With a frame static pattern, the scrambling operation is performed in parallel across all frame bits from a single pre-loaded 153-bit long register. This register is implemented as an array of 20 byte-sized words, which are dynamically loaded with the desired pattern.

10. SELF TEST METHODS

Self-testing mechanisms are essential for the operational success of the EVLA DTS. These capabilities are different from the continuous error monitoring afforded by the inclusion of the checksum. Once a basic system fault has been detected, self-testing mechanisms will be provided to enable maintenance personnel to quickly isolate and repair the fault. The MCB will control the test pattern generator located in each transmitter formatter.

To check the clock recovery circuitry, a simple alternating pattern of ones and zeros is transmitted. In this mode, no frame or meta-frame synchronization, checksum calculation, or scrambling operations occur. Adding the ten-bit sync pattern to the test pattern allows frame detection diagnostics. Enabling the five-bit incrementing sequence number provides multiple channel synchronization testing. Enabling the scrambler with fixed payloads of all zeros or all ones tests scrambling. In the previous two cases, the checksum generation is disabled.

The final diagnostics evaluates the checksum system. Pattern 6 involves the checksum generation and checking of a 128-bit pattern of all zeros. Pattern 7 uses a pattern of all ones. The remaining test patterns involve forcing an error in the checksum generation using the previous simple payload patterns. Table 3 summarizes these diagnostics patterns.

Pattern 1	10 GHz clock Recovery	160 bits of alternating ones and zeros
Pattern 2	Frame Detection	Sync pattern + 153 bits of alt. ones & zeros
Pattern 3	Multiple channel synch	Sequence word + 148 bits ones and zeros
Pattern 4	Scramble + data pat #1	enable scrambler plus 148 bits of zeros
Pattern 5	Scramble + data pat #2	enable scrambler plus 148 bits of ones
Pattern 6	chksum with pattern #1	checksum of 128 + 3 bits of zeros
Pattern 7	chksum with pattern #2	checksum of 128 + 3 bits of ones
Pattern 8	forced chksum error #1	erroneous checksum of 128 + 3 bits of zeros
Pattern 9	forced chksum error #2	erroneous checksum of 128 + 3 bits of ones

Table 3. Minimum suggested diagnostic modes.

Most of these diagnostic tests patterns use a twenty (20) byte dynamically loadable scrambling register. By combining the ability to disable the two 64-bit input words and changing the scrambling pattern all tests all of the above patterns can be generated, except those involving checksum generation.

11. IF Channel Wavelengths

Each receiver -IF will provide an instantaneous bandwidth of 4 GHz per polarization, partitioned into two 2 GHz wide sub-bands by the IF system, for a total of eight sub-bands. Each sub-band is bandpass sampled at 4 GHz, and quantized to 3 bits and transmitted on 3 discrete laser wavelengths. This produces three synchronized high-speed serial optical fiber transmission channels. There are a total of twelve channels per antenna. Each channel is transmitted at a specific laser wavelength, table 4, and multiplexed onto a single fiber.

Channel Number	Frequency (THz)	Wavelength (nm)	Signal
21	192.1	1560.61	
23	192.3	1558.98	
25	192.5	1557.36	
27	192.7	1555.75	
29	192.9	1554.13	
31	193.1	1552.52	
33	193.3	1550.92	
35	193.5	1549.32	
37	193.7	1547.72	
39	193.9	1546.12	
41	194.1	1544.53	
43	194.3	1542.94	
45			
47			
49			
51			

Table 4, DWDM Laser Frequencies and Wavelengths

12. CONCLUSION

The signaling protocol for the serial channels of the EVLA Digital Transmission System has been described. It is based upon a structure of 160 bits organized as a frame. The frame configuration consists of a sync word, a sequence word, an index, some capacity for future expansion, 128 bits of payload, and a checksum. Frame synchronization is achieved by a Barker pattern located at a known location within the frame. Cross channel synchronization is obtained by inserting an identical incrementing 5-bit binary value cycling through 32 discrete values. To monitor system performance, an 8-bit checksum check value is inserted into the frame. In addition, a method of line coding has been described which provides adequate timing information and reduces low frequency content. Scrambling the frame data by the modulo-2 addition with a prescribed pattern achieves these desired results.

ACKNOWLEDGEMENT

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