EVLA Memo 34

EVLA MONITOR AND CONTROL SYSTEM
Monitor and Control Points

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PROGRESS REPORT – March 12, 2002

This report summarizes the information gathered so far about monitor and control points for the EVLA. Some of this information will change as the design of the EVLA evolves.

Ethernet, at 100 Mbits/sec, will be the fieldbus between the antenna control computer and EVLA modules. The same fieldbus is planned for control of modules in the control building. A faster link of 1Gbit/second is planned for the monitor and control fiber between the control building and each antenna.

The structure of the field bus will allow digital commands to be sent to modules, and will allow digital monitor points to be read from the modules. A/D conversions will be carried out as needed by the individual modules, and will be considered as digital monitor points.

So far, the estimated data rate at the antenna is 148.9 Kbits/second for monitor/control.

LO SYSTEM

The first LO will be tunable between 12 and 20 GHZ., in steps of 512 MHZ. A small additional offset is to be added by a FTS. Two of these are required per antenna. The 2nd LO will be produced by a 10.8 – 14.8 GHZ. synthesizer, tunable in steps of 128 MHZ. A small additional offset will also be added to this synthesizer by a FTS. Four of these will be required

SOME GENERAL SUGGESTIONS CONCERNING THE LO SYSTEM

Monitor LO in all modules where they are present. This will aid in troubleshooting.

Monitor the purity of LO signals. Here, the idea is to be sure that there is significant power only at the desired frequency. With the aid of filters, the power level could be checked at the desired frequency, and away from the desired frequency. A wideband monitor of power with the desired frequency filtered out could detect power in the signal at undesired frequencies.

L/S/C to X-Band Converter

ESTIMATED DATA RATE 168 BITS/SECOND

Digital Monitor Points

LO #1 Power Detector	16 Bits
LO #2 Power Detector	16 Bits
Module Serial Number	8 Bits

Monitor power supplies	64 Bits
Total Power Output #1	16 Bits
Total Power Output #2	16 Bits
Total Power Output #3	16 Bits
Total Power Output #4	16 Bits

4/P to L-Band Converter

ESTIMATED DATA RATE 136 BITS/SECOND

Digital Monitor Points

Module Serial Number	8 Bits
Monitor power supplies	64 Bits
Total Power Output #1	16 Bits
Total Power Output #2	16 Bits
Total Power Output #3	16 Bits
Total Power Output #4	16 Bits

1st LO Synthesizer (Quantity 2)

ESTIMATED DATA RATE 182 BITS/SECOND (X2)

There are about 16 possible settings of the 1st LO Synthesizer, between 12 and 20 GHz. The frequency the synthesizer is multiplied times 2 for K and U bands, and is multiplied times 3 for Q and Ka bands.

Digital Monitor Points

Monitor +15 Volts	16 Bits
Monitor -15 Volts	16 Bits
Monitor +5 Volts	16 Bits
Monitor +28 Volts	16 Bits
Monitor Power of Input Reference Signal	16 Bits
Monitor Power Out	16 Bits
Monitor Frequency Control DDS	48 Bits
Monitor FTS	5 Bits
Monitor AGC DAC	16 Bits
Monitor Prescaler	
Lock Indicator	1 Bit
Phase Error	16 Bits

Commands

Frequency Control DDS	48 Bits
FTS Control	5 Bits
AGC DAC	16 Bits
Prescaler Control	

2nd LO synthesizer (Quantity 4)

ESTIMATED DATA RATE 166 BITS/SECOND (X4)

There are 800 possible settings of the 2nd LO Synthesizer, between 10.8 and 14.8 GHz., in steps of 50 MHZ.

Digital Monitor Points

+15 Volts	16 Bits
-15 Volts	16 Bits
+5 Volts	16 Bits
Power of Input Reference Signal	16 Bits
Power Out	16 Bits
Monitor Frequency Control DDS	48 Bits
FTS Frequency	5 Bits
AGC DAC	16 Bits
Prescaler	16 Bits
Lock Indicator	1 bit
Phase Error	16 Bits

Commands

Frequency Control DDS	48 bits
FTS Control	5 bits
AGC DAC	16 Bits
Prescaler Control	

X-Band IF-Switch/Amplifier

ESTIMATED DATA RATE 129 BITS/SECOND

All band switches are controlled by this module.

Digital Monitor Points

Monitor Power Supplies	64 Bits	
Monitor Band Select Switch	3 Bits	
Power In to Band Switch	16 Bits	
Power Out of Band Switch	16 Bits	
LO #1 Switch	3 Bits	
LO #2 Switch	3 Bits	
1 – 8 GHz. Band Switch #1		3 Bits
1 – 8 GHz. Band Switch #2		3 Bits
1 – 8 GHz. Band Switch #3		3 Bits
1 – 8 GHz. Band Switch #4		3 Bits
8 – 18 GHz. Band Switch	3 Bits	
8 – 12 GHz. Band Switch #1	3 Bits	
8 – 12 GHz. Band Switch #2	3 Bits	
8 – 12 GHz. Band Switch #3	3 Bits	
8 – 12 GHz. Band Switch #4	3 Bits	

Commands

LO #1 Switch	3 Bits	
LO #2 Switch	3 Bits	
1 – 8 GHz. Band Switch #1		3 Bits
1 – 8 GHz. Band Switch #2		3 Bits
1 – 8 GHz. Band Switch #3		3 Bits
1 – 8 GHz. Band Switch #4		3 Bits
8 – 18 GHz. Band Switch	3 Bits	
8 – 12 GHz. Band Switch #1	3 Bits	

8 – 12 GHz. Band Switch #2	3 Bits
8 – 12 GHz. Band Switch #3	3 Bits
8 – 12 GHz. Band Switch #4	3 Bits

Downconverter (Quantity 4)

There will be 4 downconverter modules. The input to each module comes from the X band IF switch/amplifier. Each module outputs 2 IFs. One of the IFs is 2-4 GHZ., and the other can be either 2-4 GHZ. or 1-2 GHZ. There is a total power detector associated with each IF. There will be a separate MIB associated with these total power detectors, due to the relatively high data rate.

ESTIMATED DATA RATE 105 BITS/SECOND (X4)

Digital Monitor Points

Monitor Variable Attenuator #1	8 Bits
Monitor Variable Attenuator #2	8 Bits
Monitor Variable Attenuator #3	8 Bits
Monitor Variable Attenuator #4	8 Bits
Monitor Switch #1	1 Bit
Monitor Switch #2	1 Bit
Monitor Switch #3	1 Bit
Monitor Switch #4	3 Bits
Monitor Switch #5	3 Bits
Monitor +12 Volts	16 Bits
Monitor +15 Volts	16 Bits
Monitor +5 Volts	16 Bits
Monitor -5 Volts	16 Bits

Commands

Variable Attenuator #1	8 Bits
Variable Attenuator #2	8 Bits
Variable Attenuator #3	8 Bits
Variable Attenuator #4	8 Bits
Switch #1	1 Bit
Switch #2	1 Bit
Switch #3	1 Bit
Switch #4	3 Bits
Switch #5	3 Bits

Total Power Monitor of Baseband Channels

ESTIMATED DATA RATE 128 KBITS/SEC

There will be a synchronous detector that will be used to calculate the system temperature, for each baseband channel. There will also be power detectors to monitor the signal as it goes through the system.

There will also be a power detector for each baseband that is separate from the synchronous detector. It appears that the main scientific requirements, however, are for system temperature (which involves the synchronous detector). Therefore, the data rate for power detector (analogous to the present "balanced detector") is not great.

It has been suggested that the EVLA design for Total Power Measurements at a 1 ms rate. In this case, t data rate would be: 8 basebands * 16 bits * 1000 measurements/second => 128 Kbits/second/antenna.

The total power data may be used to adjust attenuators within the same downconverter module as well a different downconverter modules.

Digital Monitors	
Total Power Digitizer #1	16 Bits
Total Power Digitizer #2	16 Bits
Total Power Digitizer #3	16 Bits
Total Power Digitizer #4	16 Bits
Total Power Digitizer #1 Internal Registers	128 Bits
Total Power Digitizer #2 Internal Registers	128 Bits
Total Power Digitizer #3 Internal Registers	128 Bits
Total Power Digitizer #4 Internal Registers	128 Bits
Commands	
Set Up Total Power Digitizer #1	16 Bits
Set Up Total Power Digitizer #2	16 Bits
Set Up Total Power Digitizer #3	16 Bits
Set Up Total Power Digitizer #4	16 Bits

Pulse Cal Generator

It is not yet decided if this will be needed

LO Reference Receiver

ESTIMATED DATA RATE 65 BITS/SECOND

Digital Monitors	
Power Supplies	64 Bits
PLL Lock Indicator	1 Bit
Commands	
Open PLL	1 Bit

LO Reference Generator

ESTIMATED DATA RATE 257 BITS/SECOND

Digital Monitors	
+3.3 Volt Power Supply	16 Bits
+5 Volt Power Supply	16 Bits
+15 Volt Power Supply	16 Bits
–15 Volt Power Supply	16 Bits
4 GHz. Phase Monitor	16 Bits
128 MHZ Lock Indicator	1 Bit
128 MHz Control Voltage	16 Bits
128 MHz Power Detector	16 Bits
256 MHz Power Detector	16 Bits
512 MHz Power Detector	16 Bits
1.024 GHz. Power Detector	16 Bits
2.046 GHz. Power Detector	16 Bits

4.096 GHz. Power Detector	16 Bits
19.2 Hz Power Detector	16 Bits
9.6 Hz Power Detector	16 Bits
1.0 Hz Power Detector	16 Bits
0.1 Hz Power Detector	16 Bits

Digitizer DTS Module (Quantity 4)

ESTIMATED DATA RATE 244 BITS/SECOND

The DTS module will contain 4 boards for digitizers, demultiplexers, formatters, and laser controllers.

The 3-bit Samplers are expected to run always at the rate of 4.096 gsamples/second.
Each Digitizer module contains 2 3-bit samplers and 1 8-bit sampler. Each sampler is input to a multiplexer (48-bit for the 3-bit samplers, and 64-bit for the 8-bit samplers). The 3x128 formatter selec the 2 3-bit samplers or the 8 bit sampler as its input.

Digital Monitors

Threshold Voltages	16 Bits
Power Supply Voltages	64 Bits
Power Level of Clock	16 Bits
Input Clock Detector	16 Bits

8-Bit Digitizers for low frequency receivers

The 8-bit samplers will run at 2.048 gsamples/second. . No control points are needed. Some monitor points are desirable, although the sampler modules presently used in the VLA and VLBA are not monitored.

Digital Monitors

Threshold Voltages	16 Bits
Power Supply Voltages	16 Bits
Power Level of Clock	16 Bits
Input Clock Detector	16 Bits

Formatter

Digital Monitors

Select test pattern/astronomical data	4 Bits

Commands

Select test pattern/astronomical data	4 Bits

Laser controller

Digital Monitors

Laser Temperature	16 Bits
Laser Temperature Setpoint	16 Bits
Laser Power	16 Bits
Laser Current	16 Bits

Commands

Temperature Setpoint	16 Bits
Turn Laser On/Off	1 Bit

Laptop Port (Quantity 10)

It has been suggested that laptop port be present at each antenna to interface with the EVLA monitor and control system.

ACU

ESTIMATED DATA RATE 1.5 KBITS/SECOND

The ACU may be a single board computer, or it may be a separate unit. The current plan is that commands and monitor points have 32 bits reserved, even if they are not all used. This is enough resolution to see the noise in the electronics. The azimuth and elevation encoders will use 25 bits, and will be capable of position readouts from 0 to 720 degrees, even though the antenna will not move within this entire range.

Analog Monitor Points (Digitized in ACU) (Each Monitor is 16 Bits)

	Scale	Range (volts)	Range (at scale)	Res	Freq
Azimuth Motor #2 Current3.2 A		-9.375/9.375	-30 A/30 A	1 mA	500 ms
Azimuth Motor #1 Current3.2 A		-9.375/9.375	-30 A/30 A	1 mA	500 ms
Elevation Motor #2 Current	3.2 A	-9.375/9.375	-30 A/30 A	1 mA	500 ms
Elevation Motor #1 Current	3.2 A	-9.375/9.375	-30 A/30 A	1 mA	500 ms
Azimuth Velocity Command	6.0 °/min	0/6.67	0/40 °/min	6.8as/m	500 ms
Azimuth Current Command	3.2 A	-9.375/9.375	-30 A/30 A	1 mA	500 ms
Elevation Velocity Command	3.0 °/min	0/6.67	0/20 °/min	3.4 as/m	500 ms
Elevation Current Command	3.2 A	-9.375/9.375	-30 A/30 A	1 mA	500 ms
Wind Speed Readout					

Digital Monitor Points

	Bits Required	Range	Resolution	Freq
Azimuth Position	25	0/720 degrees	0.08 arcsec	100 ms
Elevation Position	25	0/720 degrees	0.08 arcsec	100 ms
Main Field Breaker Fault	1			
Elevation Motor #2 Field Breaker Fault	1			
Elevation Motor #2 Armature Breaker Fault	1			
Elevation Motor #2 Elect Breaker Fault	1			
Elevation Motor #2 Brake Breaker Fault	1			
Elevation Motor #1 Field Breaker Fault	1			
Elevation Motor #1 Armature Breaker Fault	1			

Elevation Motor #1 Elect Breaker Fault	1
Elevation Motor #1 Brake Breaker Fault	1
Azimuth Motor #2 Field Breaker Fault	1
Azimuth Motor #2 Armature Breaker Fault	1
Azimuth Motor #2 Elect Breaker Fault	1
Azimuth Motor #2 Brake Breaker Fault	1
Azimuth Motor #1 Field Breaker Fault	1
Azimuth Motor #1 Armature Breaker Fault	1
Azimuth Motor #1 Elect Breaker Fault	1
Azimuth Motor #1 Brake Breaker Fault	1
Azimuth Gearbox Lube Pump Pressure Low	1
Elevation Final Limit Down	1
Elevation Final Limit Up	1
Elevation First Limit Down	1
Elevation First Limit Up	1
Digital Position Mode	1
* Elevation Parity Error	1
Azimuth Final Limit CCW	1
Azimuth Final Limit CW	1
Azimuth First Limit CCW	1
Azimuth Final Limit CW	1
Computer/Manual Control	1
Azimuth Parity Error	1
Azimuth #2 Motor Over Temperature	1
Azimuth #1 Motor Over Temperature	1
Elevation #2 Motor Over Temperature	1
Elevation #1 Motor Over Temperature	1
Encoder Heater/Blower Ckt Breaker Fault	1
100 A Drive Cabinet Ckt Breaker Fault	1
Drive Cabinet Over Temperature	1
Field Fault – Azimuth #2 Motor	1
Field Fault – Azimuth #1 Motor	1
Field Fault – Elevation #2 Motor	1
Field Fault – Elevation #1 Motor	1
Stow Pin In/Out	1
Emergency Stop On/Off	1
* Mode Parity Error	1
Fan Fault – No Air Flow	1
Ped Room Temperature Too High	1
Elevation Limit Override On/Off	1
Azimuth Limit Override On/Off	1
Fire Detection System Malfunction	1

Commands

	Bits Required	Range	Resolution	Freq
Azimuth Position	25	0/720 degrees	0.08 arcsec	100 n
Elevation Position	25	0/720 degrees	0.08 arcsec	100 n
Motor Fault Override ? All motors or none?	1			
Digital Position Mode	1			
Stand-by	1			
Auto Stow Enable	1			
Elevation First Limit Override	1			
Elevation Motor #2 Disable	1			
Elevation Motor #1 Disable	1			

Azimuth First Limit Override	1
Azimuth Motor #2 Disable	1
Azimuth Motor #1 Disable	1

* These monitor points will probably disappear because these functions will be done by the fieldbus for all commands and monitors.

FRM Subsystem

ESTIMATED DATA RATE 1.1 KBITS/SECOND

The Expanded VLA FRM subsystem will have to be dealt with twice; once for Phase I and again for Phase II. The Phase II effort of course depends upon the future goals of re-designing the subreflector and its mechanical system, as well as operational requirements. Therefore this system should evolve from its current state into an intermediate state. Whether it evolves again, would be determined by Phase II goals.

The Monitor and Control System would consist of:

Power Supply Monitors - Local power supply monitoring for preventive maintenance.
A. Ground - 5mV or better resolution. Rate 5 seconds.
B. +5V - 5mV or better resolution. Rate 5 seconds.
C. +15V - 5mV or better resolution. Rate 5 seconds.
D. -15V - 5mV or better resolution. Rate 5 seconds.

FRM Rotation and Focus Positions (Command and Monitor)
Both Digital 16 bits wide. Rate could approach .1 seconds

FRM Rotation and Focus Nap Command
Both Digital at least 1 bit wide.

FRM Rotation and Focus Software Reset Command
Both Digital at least 1 bit wide.
Both Digital at least 1 bit wide.

FRM Rotation and Focus Manual Override Command
Both Digital at least 1 bit wide.

FRM Rotation and Focus Actual Position Monitor
Both Digital 16 bits wide. Rate could approach .1 seconds

FRM Rotation and Focus Position Error Monitor
Both Digital 16 bits wide. Rate could approach .1 seconds

FRM Rotation and Focus Status Monitors
Width could vary depending upon individual Status Flags or packed Status Flags. Rate 1 second.

Dichroic Interface

The Dichroic Interface would control the insertion of a dicroic that reflects one frequency to a different receiver, and lets another frequency pass through. This would be used for dual frequency observations such as S/X. This is for possible future expansion. The module may never exist.

Pointing Model Interface

The Pointing Model Interface would gather physical data from the antenna structure so that pointing corrections could be applied. This is for possible future expansion, and may never exist.

FRONT END SYSTEM

The Front End system currently includes the receiver electronics, as well as the electronics where the frequency conversions take place to produce IF signals. This report is a best effort to define the monitor and control points, even though there does not yet exist a complete block diagram of the front end system.

There are 10 receivers in the plan, including 8 receivers secondary focus, and 2 receivers (74 MHZ and 327 MHZ) at the image of the prime focus.

Secondary Focus Receivers

Band	Freq Range (GHZ.)
L	1.0 - 2.0
S	2.0 - 4.0
C	4.0 - 8.0
X	8.0 - 12.0
U	12.0 - 18.0
K	18.0 - 26.0
K_a	26.0 - 40.0
Q	40.0 - 50.0

Prime Focus Receivers

74 MHZ (400 cm)
327 MHZ (90 cm)
Two Additional In Future

There needs to be provision for monitor and control of the feed heaters (de-icers). It may be desirable to monitor the current and voltage. A control point will be necessary to turn the heaters on and off. Monitor and control points for the refrigerators may be moved from this section to the Cryo section in the future.

W-Band Front End

ESTIMATED DATA RATE 1.5 KBITS/SECOND

Digital Monitor Points

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Solar Switch 1	1 Bit
Solar Switch 2	1 Bit
Solar Step Attenuator	5 Bits
Solenoid Valve	1 Bit
Pump Request	1 Bit
Fridge Request	1 Bit

Manual/Computer	1 Bit
Band Code	4 Bits
Receiver Serial Number	6 Bits
Receiver Modification Level	2 Bits
RCP LNA Stage 1 VD1	16 Bits
RCP LNA Stage 1 ID1	16 Bits
RCP LNA Stage 1 VG1	16 Bits
RCP LNA Stage 2 VD2	16 Bits
RCP LNA Stage 2 ID2	16 Bits
RCP LNA Stage 2 VG2	16 Bits
RCP LNA Stage 3 VD3	16 Bits
RCP LNA Stage 3 ID3	16 Bits
RCP LNA Stage 3 VG3	16 Bits
RCP LNA Stage 4 VD4	16 Bits
RCP LNA Stage 4 ID4	16 Bits
RCP LNA Stage 4 VG4	16 Bits
LCP LNA Stage 1 VD1	16 Bits
LCP LNA Stage 1 ID1	16 Bits
LCP LNA Stage 1 VG1	16 Bits
LCP LNA Stage 2 VD2	16 Bits
LCP LNA Stage 2 ID2	16 Bits
LCP LNA Stage 2 VG2	16 Bits
LCP LNA Stage 3 VD3	16 Bits
LCP LNA Stage 3 ID3	16 Bits
LCP LNA Stage 3 VG3	16 Bits
LCP LNA Stage 4 VD4	16 Bits
LCP LNA Stage 4 ID4	16 Bits
LCP LNA Stage 4 VG4	16 Bits
OPTIONAL RCP LNA Stage 1 VD1	16 Bits
OPTIONAL RCP LNA Stage 1 ID1	16 Bits
OPTIONAL RCP LNA Stage 1 VG1	16 Bits
OPTIONAL RCP LNA Stage 2 VD2	16 Bits
OPTIONAL RCP LNA Stage 2 ID2	16 Bits
OPTIONAL RCP LNA Stage 2 VG2	16 Bits
OPTIONAL RCP LNA Stage 3 VD3	16 Bits
OPTIONAL RCP LNA Stage 3 ID3	16 Bits
OPTIONAL RCP LNA Stage 3 VG3	16 Bits
OPTIONAL RCP LNA Stage 4 VD4	16 Bits
OPTIONAL RCP LNA Stage 4 ID4	16 Bits
OPTIONAL RCP LNA Stage 4 VG4	16 Bits
OPTIONAL LCP LNA Stage 1 VD1	16 Bits
OPTIONAL LCP LNA Stage 1 ID1	16 Bits
OPTIONAL LCP LNA Stage 1 VG1	16 Bits
OPTIONAL LCP LNA Stage 2 VD2	16 Bits
OPTIONAL LCP LNA Stage 2 ID2	16 Bits
OPTIONAL LCP LNA Stage 2 VG2	16 Bits
OPTIONAL LCP LNA Stage 3 VD3	16 Bits
OPTIONAL LCP LNA Stage 3 ID3	16 Bits
OPTIONAL LCP LNA Stage 3 VG3	16 Bits
OPTIONAL LCP LNA Stage 4 VD4	16 Bits
OPTIONAL LCP LNA Stage 4 ID4	16 Bits
OPTIONAL LCP LNA Stage 4 VG4	16 Bits
15K Temperature	16 Bits
50K Temperature	16 Bits
300K Temperature	16 Bits
Dewar Vacuum Pressure	16 Bits

Pump Vacuum Pressure	16 Bits
Noise Source Cal Voltage	16 Bits
Noise Source Cal Current	16 Bits
Solar Noise Cal Voltage	16 Bits
Solar Noise Cal Current	16 Bits
+15 Volts	16 Bits
-15 Volts	16 Bits
+5 Volts	16 Bits
+28 Volts	16 Bits
RCP LED	16 Bits
LCP LED	16 Bits
Optional Power Detector RCP-IF	16 Bits
Optional Power Detector LCP-IF	16 Bits
Optional Power Detector LO	16 Bits
Spare Analog Monitor 1	16 Bits
Spare Analog Monitor 2	16 Bits
Spare Analog Monitor 3	16 Bits
Readback of RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of LCP LNA Stage 2 VD2 Bias	12 Bits
Readback of LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of LCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 ID4 Bias	12 Bits

ıands

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit

Cryo Vacuum Pumping	1 Bit
Set Solar Switch 1	1 Bit
Set Solar Switch 2	1 Bit
Set Solar Step Attenuator	5 Bits
RCP LNA Stage 1 VD1 Bias	12 Bits
RCP LNA Stage 1 ID1 Bias	12 Bits
RCP LNA Stage 2 VD2 Bias	12 Bits
RCP LNA Stage 2 ID2 Bias	12 Bits
RCP LNA Stage 3 VD3 Bias	12 Bits
RCP LNA Stage 3 ID3 Bias	12 Bits
RCP LNA Stage 4 VD4 Bias	12 Bits
RCP LNA Stage 4 ID4 Bias	12 Bits
LCP LNA Stage 1 VD1 Bias	12 Bits
LCP LNA Stage 1 ID1 Bias	12 Bits
LCP LNA Stage 2 VD2 Bias	12 Bits
LCP LNA Stage 2 ID2 Bias	12 Bits
LCP LNA Stage 3 VD3 Bias	12 Bits
LCP LNA Stage 3 ID3 Bias	12 Bits
LCP LNA Stage 4 VD4 Bias	12 Bits
LCP LNA Stage 4 ID4 Bias	12 Bits
Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Optional LCP LNA Stage 4 ID4 Bias	12 Bits

Q-Band Front End

ESTIMATED DATA RATE 1.5 KBITS/SECOND

Digital Monitor Points

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Solar Switch 1	1 Bit
Solar Switch 2	1 Bit
Solar Step Attenuator	5 Bits
Solenoid Valve	1 Bit
Pump Request	1 Bit
Fridge Request	1 Bit

Manual/Computer	1 Bit
Band Code	4 Bits
Receiver Serial Number	6 Bits
Receiver Modification Level	2 Bits
RCP LNA Stage 1 VD1	16 Bits
RCP LNA Stage 1 ID1	16 Bits
RCP LNA Stage 1 VG1	16 Bits
RCP LNA Stage 2 VD2	16 Bits
RCP LNA Stage 2 ID2	16 Bits
RCP LNA Stage 2 VG2	16 Bits
RCP LNA Stage 3 VD3	16 Bits
RCP LNA Stage 3 ID3	16 Bits
RCP LNA Stage 3 VG3	16 Bits
RCP LNA Stage 4 VD4	16 Bits
RCP LNA Stage 4 ID4	16 Bits
RCP LNA Stage 4 VG4	16 Bits
LCP LNA Stage 1 VD1	16 Bits
LCP LNA Stage 1 ID1	16 Bits
LCP LNA Stage 1 VG1	16 Bits
LCP LNA Stage 2 VD2	16 Bits
LCP LNA Stage 2 ID2	16 Bits
LCP LNA Stage 2 VG2	16 Bits
LCP LNA Stage 3 VD3	16 Bits
LCP LNA Stage 3 ID3	16 Bits
LCP LNA Stage 3 VG3	16 Bits
LCP LNA Stage 4 VD4	16 Bits
LCP LNA Stage 4 ID4	16 Bits
LCP LNA Stage 4 VG4	16 Bits
OPTIONAL RCP LNA Stage 1 VD1	16 Bits
OPTIONAL RCP LNA Stage 1 ID1	16 Bits
OPTIONAL RCP LNA Stage 1 VG1	16 Bits
OPTIONAL RCP LNA Stage 2 VD2	16 Bits
OPTIONAL RCP LNA Stage 2 ID2	16 Bits
OPTIONAL RCP LNA Stage 2 VG2	16 Bits
OPTIONAL RCP LNA Stage 3 VD3	16 Bits
OPTIONAL RCP LNA Stage 3 ID3	16 Bits
OPTIONAL RCP LNA Stage 3 VG3	16 Bits
OPTIONAL RCP LNA Stage 4 VD4	16 Bits
OPTIONAL RCP LNA Stage 4 ID4	16 Bits
OPTIONAL RCP LNA Stage 4 VG4	16 Bits
OPTIONAL LCP LNA Stage 1 VD1	16 Bits
OPTIONAL LCP LNA Stage 1 ID1	16 Bits
OPTIONAL LCP LNA Stage 1 VG1	16 Bits
OPTIONAL LCP LNA Stage 2 VD2	16 Bits
OPTIONAL LCP LNA Stage 2 ID2	16 Bits
OPTIONAL LCP LNA Stage 2 VG2	16 Bits
OPTIONAL LCP LNA Stage 3 VD3	16 Bits
OPTIONAL LCP LNA Stage 3 ID3	16 Bits
OPTIONAL LCP LNA Stage 3 VG3	16 Bits
OPTIONAL LCP LNA Stage 4 VD4	16 Bits
OPTIONAL LCP LNA Stage 4 ID4	16 Bits
OPTIONAL LCP LNA Stage 4 VG4	16 Bits
15K Temperature	16 Bits
50K Temperature	16 Bits
300K Temperature	16 Bits
Dewar Vacuum Pressure	16 Bits

Pump Vacuum Pressure	16 Bits
Noise Source Cal Voltage	16 Bits
Noise Source Cal Current	16 Bits
Solar Noise Cal Voltage	16 Bits
Solar Noise Cal Current	16 Bits
+15 Volts	16 Bits
-15 Volts	16 Bits
+5 Volts	16 Bits
+28 Volts	16 Bits
RCP LED	16 Bits
LCP LED	16 Bits
Optional Power Detector RCP-IF	16 Bits
Optional Power Detector LCP-IF	16 Bits
Optional Power Detector LO	16 Bits
Spare Analog Monitor 1	16 Bits
Spare Analog Monitor 2	16 Bits
Spare Analog Monitor 3	16 Bits
Readback of RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of LCP LNA Stage 2 VD2 Bias	12 Bits
Readback of LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of LCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 ID4 Bias	12 Bits

ands

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit

Cryo Vacuum Pumping	1 Bit
Set Solar Switch 1	1 Bit
Set Solar Switch 2	1 Bit
Set Solar Step Attenuator	5 Bits
RCP LNA Stage 1 VD1 Bias	12 Bits
RCP LNA Stage 1 ID1 Bias	12 Bits
RCP LNA Stage 2 VD2 Bias	12 Bits
RCP LNA Stage 2 ID2 Bias	12 Bits
RCP LNA Stage 3 VD3 Bias	12 Bits
RCP LNA Stage 3 ID3 Bias	12 Bits
RCP LNA Stage 4 VD4 Bias	12 Bits
RCP LNA Stage 4 ID4 Bias	12 Bits
LCP LNA Stage 1 VD1 Bias	12 Bits
LCP LNA Stage 1 ID1 Bias	12 Bits
LCP LNA Stage 2 VD2 Bias	12 Bits
LCP LNA Stage 2 ID2 Bias	12 Bits
LCP LNA Stage 3 VD3 Bias	12 Bits
LCP LNA Stage 3 ID3 Bias	12 Bits
LCP LNA Stage 4 VD4 Bias	12 Bits
LCP LNA Stage 4 ID4 Bias	12 Bits
Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Optional LCP LNA Stage 4 ID4 Bias	12 Bits

Ka-Band Front End

ESTIMATED DATA RATE 1.5 KBITS/SECOND

Digital Monitor Points

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Solar Switch 1	1 Bit
Solar Switch 2	1 Bit
Solar Step Attenuator	5 Bits
Solenoid Valve	1 Bit
Pump Request	1 Bit
Fridge Request	1 Bit
Manual/Computer	1 Bit
Band Code	4 Bits

Receiver Serial Number	6 Bits
Receiver Modification Level	2 Bits
RCP LNA Stage 1 VD1	16 Bits
RCP LNA Stage 1 ID1	16 Bits
RCP LNA Stage 1 VG1	16 Bits
RCP LNA Stage 2 VD2	16 Bits
RCP LNA Stage 2 ID2	16 Bits
RCP LNA Stage 2 VG2	16 Bits
RCP LNA Stage 3 VD3	16 Bits
RCP LNA Stage 3 ID3	16 Bits
RCP LNA Stage 3 VG3	16 Bits
RCP LNA Stage 4 VD4	16 Bits
RCP LNA Stage 4 ID4	16 Bits
RCP LNA Stage 4 VG4	16 Bits
LCP LNA Stage 1 VD1	16 Bits
LCP LNA Stage 1 ID1	16 Bits
LCP LNA Stage 1 VG1	16 Bits
LCP LNA Stage 2 VD2	16 Bits
LCP LNA Stage 2 ID2	16 Bits
LCP LNA Stage 2 VG2	16 Bits
LCP LNA Stage 3 VD3	16 Bits
LCP LNA Stage 3 ID3	16 Bits
LCP LNA Stage 3 VG3	16 Bits
LCP LNA Stage 4 VD4	16 Bits
LCP LNA Stage 4 ID4	16 Bits
LCP LNA Stage 4 VG4	16 Bits
OPTIONAL RCP LNA Stage 1 VD1	16 Bits
OPTIONAL RCP LNA Stage 1 ID1	16 Bits
OPTIONAL RCP LNA Stage 1 VG1	16 Bits
OPTIONAL RCP LNA Stage 2 VD2	16 Bits
OPTIONAL RCP LNA Stage 2 ID2	16 Bits
OPTIONAL RCP LNA Stage 2 VG2	16 Bits
OPTIONAL RCP LNA Stage 3 VD3	16 Bits
OPTIONAL RCP LNA Stage 3 ID3	16 Bits
OPTIONAL RCP LNA Stage 3 VG3	16 Bits
OPTIONAL RCP LNA Stage 4 VD4	16 Bits
OPTIONAL RCP LNA Stage 4 ID4	16 Bits
OPTIONAL RCP LNA Stage 4 VG4	16 Bits
OPTIONAL LCP LNA Stage 1 VD1	16 Bits
OPTIONAL LCP LNA Stage 1 ID1	16 Bits
OPTIONAL LCP LNA Stage 1 VG1	16 Bits
OPTIONAL LCP LNA Stage 2 VD2	16 Bits
OPTIONAL LCP LNA Stage 2 ID2	16 Bits
OPTIONAL LCP LNA Stage 2 VG2	16 Bits
OPTIONAL LCP LNA Stage 3 VD3	16 Bits
OPTIONAL LCP LNA Stage 3 ID3	16 Bits
OPTIONAL LCP LNA Stage 3 VG3	16 Bits
OPTIONAL LCP LNA Stage 4 VD4	16 Bits
OPTIONAL LCP LNA Stage 4 ID4	16 Bits
OPTIONAL LCP LNA Stage 4 VG4	16 Bits
15K Temperature	16 Bits
50K Temperature	16 Bits
300K Temperature	16 Bits
Dewar Vacuum Pressure	16 Bits
Pump Vacuum Pressure	16 Bits
Noise Source Cal Voltage	16 Bits

Noise Source Cal Current	16 Bits
Solar Noise Cal Voltage	16 Bits
Solar Noise Cal Current	16 Bits
+15 Volts	16 Bits
-15 Volts	16 Bits
+5 Volts	16 Bits
+28 Volts	16 Bits
RCP LED	16 Bits
LCP LED	16 Bits
Optional Power Detector RCP-IF	16 Bits
Optional Power Detector LCP-IF	16 Bits
Optional Power Detector LO	16 Bits
Spare Analog Monitor 1	16 Bits
Spare Analog Monitor 2	16 Bits
Spare Analog Monitor 3	16 Bits
Readback of RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of LCP LNA Stage 2 VD2 Bias	12 Bits
Readback of LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of LCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 ID4 Bias	12 Bits

ands

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Set Solar Switch 1	1 Bit

Set Solar Switch 2	1 Bit
Set Solar Step Attenuator	5 Bits
RCP LNA Stage 1 VD1 Bias	12 Bits
RCP LNA Stage 1 ID1 Bias	12 Bits
RCP LNA Stage 2 VD2 Bias	12 Bits
RCP LNA Stage 2 ID2 Bias	12 Bits
RCP LNA Stage 3 VD3 Bias	12 Bits
RCP LNA Stage 3 ID3 Bias	12 Bits
RCP LNA Stage 4 VD4 Bias	12 Bits
RCP LNA Stage 4 ID4 Bias	12 Bits
LCP LNA Stage 1 VD1 Bias	12 Bits
LCP LNA Stage 1 ID1 Bias	12 Bits
LCP LNA Stage 2 VD2 Bias	12 Bits
LCP LNA Stage 2 ID2 Bias	12 Bits
LCP LNA Stage 3 VD3 Bias	12 Bits
LCP LNA Stage 3 ID3 Bias	12 Bits
LCP LNA Stage 4 VD4 Bias	12 Bits
LCP LNA Stage 4 ID4 Bias	12 Bits
Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Optional LCP LNA Stage 4 ID4 Bias	12 Bits

K-Band Front End

ESTIMATED DATA RATE 1.5 KBITS/SECOND

Digital Monitor Points

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Solar Switch 1	1 Bit
Solar Switch 2	1 Bit
Solar Step Attenuator	5 Bits
Solenoid Valve	1 Bit
Pump Request	1 Bit
Fridge Request	1 Bit
Manual/Computer	1 Bit
Band Code	4 Bits
Receiver Serial Number	6 Bits

Receiver Modification Level	2 Bits
RCP LNA Stage 1 VD1	16 Bits
RCP LNA Stage 1 ID1	16 Bits
RCP LNA Stage 1 VG1	16 Bits
RCP LNA Stage 2 VD2	16 Bits
RCP LNA Stage 2 ID2	16 Bits
RCP LNA Stage 2 VG2	16 Bits
RCP LNA Stage 3 VD3	16 Bits
RCP LNA Stage 3 ID3	16 Bits
RCP LNA Stage 3 VG3	16 Bits
RCP LNA Stage 4 VD4	16 Bits
RCP LNA Stage 4 ID4	16 Bits
RCP LNA Stage 4 VG4	16 Bits
LCP LNA Stage 1 VD1	16 Bits
LCP LNA Stage 1 ID1	16 Bits
LCP LNA Stage 1 VG1	16 Bits
LCP LNA Stage 2 VD2	16 Bits
LCP LNA Stage 2 ID2	16 Bits
LCP LNA Stage 2 VG2	16 Bits
LCP LNA Stage 3 VD3	16 Bits
LCP LNA Stage 3 ID3	16 Bits
LCP LNA Stage 3 VG3	16 Bits
LCP LNA Stage 4 VD4	16 Bits
LCP LNA Stage 4 ID4	16 Bits
LCP LNA Stage 4 VG4	16 Bits
OPTIONAL RCP LNA Stage 1 VD1	16 Bits
OPTIONAL RCP LNA Stage 1 ID1	16 Bits
OPTIONAL RCP LNA Stage 1 VG1	16 Bits
OPTIONAL RCP LNA Stage 2 VD2	16 Bits
OPTIONAL RCP LNA Stage 2 ID2	16 Bits
OPTIONAL RCP LNA Stage 2 VG2	16 Bits
OPTIONAL RCP LNA Stage 3 VD3	16 Bits
OPTIONAL RCP LNA Stage 3 ID3	16 Bits
OPTIONAL RCP LNA Stage 3 VG3	16 Bits
OPTIONAL RCP LNA Stage 4 VD4	16 Bits
OPTIONAL RCP LNA Stage 4 ID4	16 Bits
OPTIONAL RCP LNA Stage 4 VG4	16 Bits
OPTIONAL LCP LNA Stage 1 VD1	16 Bits
OPTIONAL LCP LNA Stage 1 ID1	16 Bits
OPTIONAL LCP LNA Stage 1 VG1	16 Bits
OPTIONAL LCP LNA Stage 2 VD2	16 Bits
OPTIONAL LCP LNA Stage 2 ID2	16 Bits
OPTIONAL LCP LNA Stage 2 VG2	16 Bits
OPTIONAL LCP LNA Stage 3 VD3	16 Bits
OPTIONAL LCP LNA Stage 3 ID3	16 Bits
OPTIONAL LCP LNA Stage 3 VG3	16 Bits
OPTIONAL LCP LNA Stage 4 VD4	16 Bits
OPTIONAL LCP LNA Stage 4 ID4	16 Bits
OPTIONAL LCP LNA Stage 4 VG4	16 Bits
15K Temperature	16 Bits
50K Temperature	16 Bits
300K Temperature	16 Bits
Dewar Vacuum Pressure	16 Bits
Pump Vacuum Pressure	16 Bits
Noise Source Cal Voltage	16 Bits
Noise Source Cal Current	16 Bits

Solar Noise Cal Voltage	16 Bits
Solar Noise Cal Current	16 Bits
+15 Volts	16 Bits
-15 Volts	16 Bits
+5 Volts	16 Bits
+28 Volts	16 Bits
RCP LED	16 Bits
LCP LED	16 Bits
Optional Power Detector RCP-IF	16 Bits
Optional Power Detector LCP-IF	16 Bits
Optional Power Detector LO	16 Bits
Spare Analog Monitor 1	16 Bits
Spare Analog Monitor 2	16 Bits
Spare Analog Monitor 3	16 Bits
Readback of RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of LCP LNA Stage 2 VD2 Bias	12 Bits
Readback of LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of LCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 ID4 Bias	12 Bits

ands

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Set Solar Switch 1	1 Bit
Set Solar Switch 2	1 Bit

Set Solar Step Attenuator	5 Bits
RCP LNA Stage 1 VD1 Bias	12 Bits
RCP LNA Stage 1 ID1 Bias	12 Bits
RCP LNA Stage 2 VD2 Bias	12 Bits
RCP LNA Stage 2 ID2 Bias	12 Bits
RCP LNA Stage 3 VD3 Bias	12 Bits
RCP LNA Stage 3 ID3 Bias	12 Bits
RCP LNA Stage 4 VD4 Bias	12 Bits
RCP LNA Stage 4 ID4 Bias	12 Bits
LCP LNA Stage 1 VD1 Bias	12 Bits
LCP LNA Stage 1 ID1 Bias	12 Bits
LCP LNA Stage 2 VD2 Bias	12 Bits
LCP LNA Stage 2 ID2 Bias	12 Bits
LCP LNA Stage 3 VD3 Bias	12 Bits
LCP LNA Stage 3 ID3 Bias	12 Bits
LCP LNA Stage 4 VD4 Bias	12 Bits
LCP LNA Stage 4 ID4 Bias	12 Bits
Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Optional LCP LNA Stage 4 ID4 Bias	12 Bits

Ku-Band Front End

ESTIMATED DATA RATE 1.5 KBITS/SECOND

Digital Monitor Points

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Solar Switch 1	1 Bit
Solar Switch 2	1 Bit
Solar Step Attenuator	5 Bits
Solenoid Valve	1 Bit
Pump Request	1 Bit
Fridge Request	1 Bit
Manual/Computer	1 Bit
Band Code	4 Bits
Receiver Serial Number	6 Bits
Receiver Modification Level	2 Bits
RCP LNA Stage 1 VD1	16 Bits

RCP LNA Stage 1 ID1	16 Bits
RCP LNA Stage 1 VG1	16 Bits
RCP LNA Stage 2 VD2	16 Bits
RCP LNA Stage 2 ID2	16 Bits
RCP LNA Stage 2 VG2	16 Bits
RCP LNA Stage 3 VD3	16 Bits
RCP LNA Stage 3 ID3	16 Bits
RCP LNA Stage 3 VG3	16 Bits
RCP LNA Stage 4 VD4	16 Bits
RCP LNA Stage 4 ID4	16 Bits
RCP LNA Stage 4 VG4	16 Bits
LCP LNA Stage 1 VD1	16 Bits
LCP LNA Stage 1 ID1	16 Bits
LCP LNA Stage 1 VG1	16 Bits
LCP LNA Stage 2 VD2	16 Bits
LCP LNA Stage 2 ID2	16 Bits
LCP LNA Stage 2 VG2	16 Bits
LCP LNA Stage 3 VD3	16 Bits
LCP LNA Stage 3 ID3	16 Bits
LCP LNA Stage 3 VG3	16 Bits
LCP LNA Stage 4 VD4	16 Bits
LCP LNA Stage 4 ID4	16 Bits
LCP LNA Stage 4 VG4	16 Bits
OPTIONAL RCP LNA Stage 1 VD1	16 Bits
OPTIONAL RCP LNA Stage 1 ID1	16 Bits
OPTIONAL RCP LNA Stage 1 VG1	16 Bits
OPTIONAL RCP LNA Stage 2 VD2	16 Bits
OPTIONAL RCP LNA Stage 2 ID2	16 Bits
OPTIONAL RCP LNA Stage 2 VG2	16 Bits
OPTIONAL RCP LNA Stage 3 VD3	16 Bits
OPTIONAL RCP LNA Stage 3 ID3	16 Bits
OPTIONAL RCP LNA Stage 3 VG3	16 Bits
OPTIONAL RCP LNA Stage 4 VD4	16 Bits
OPTIONAL RCP LNA Stage 4 ID4	16 Bits
OPTIONAL RCP LNA Stage 4 VG4	16 Bits
OPTIONAL LCP LNA Stage 1 VD1	16 Bits
OPTIONAL LCP LNA Stage 1 ID1	16 Bits
OPTIONAL LCP LNA Stage 1 VG1	16 Bits
OPTIONAL LCP LNA Stage 2 VD2	16 Bits
OPTIONAL LCP LNA Stage 2 ID2	16 Bits
OPTIONAL LCP LNA Stage 2 VG2	16 Bits
OPTIONAL LCP LNA Stage 3 VD3	16 Bits
OPTIONAL LCP LNA Stage 3 ID3	16 Bits
OPTIONAL LCP LNA Stage 3 VG3	16 Bits
OPTIONAL LCP LNA Stage 4 VD4	16 Bits
OPTIONAL LCP LNA Stage 4 ID4	16 Bits
OPTIONAL LCP LNA Stage 4 VG4	16 Bits
15K Temperature	16 Bits
50K Temperature	16 Bits
300K Temperature	16 Bits
Dewar Vacuum Pressure	16 Bits
Pump Vacuum Pressure	16 Bits
Noise Source Cal Voltage	16 Bits
Noise Source Cal Current	16 Bits
Solar Noise Cal Voltage	16 Bits
Solar Noise Cal Current	16 Bits

+15 Volts	16 Bits
-15 Volts	16 Bits
+5 Volts	16 Bits
+28 Volts	16 Bits
RCP LED	16 Bits
LCP LED	16 Bits
Optional Power Detector RCP-IF	16 Bits
Optional Power Detector LCP-IF	16 Bits
Optional Power Detector LO	16 Bits
Spare Analog Monitor 1	16 Bits
Spare Analog Monitor 2	16 Bits
Spare Analog Monitor 3	16 Bits
Readback of RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of LCP LNA Stage 2 VD2 Bias	12 Bits
Readback of LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of LCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 ID4 Bias	12 Bits

ands

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Set Solar Switch 1	1 Bit
Set Solar Switch 2	1 Bit
Set Solar Step Attenuator	5 Bits
RCP LNA Stage 1 VD1 Bias	12 Bits

RCP LNA Stage 1 ID1 Bias	12 Bits
RCP LNA Stage 2 VD2 Bias	12 Bits
RCP LNA Stage 2 ID2 Bias	12 Bits
RCP LNA Stage 3 VD3 Bias	12 Bits
RCP LNA Stage 3 ID3 Bias	12 Bits
RCP LNA Stage 4 VD4 Bias	12 Bits
RCP LNA Stage 4 ID4 Bias	12 Bits
LCP LNA Stage 1 VD1 Bias	12 Bits
LCP LNA Stage 1 ID1 Bias	12 Bits
LCP LNA Stage 2 VD2 Bias	12 Bits
LCP LNA Stage 2 ID2 Bias	12 Bits
LCP LNA Stage 3 VD3 Bias	12 Bits
LCP LNA Stage 3 ID3 Bias	12 Bits
LCP LNA Stage 4 VD4 Bias	12 Bits
LCP LNA Stage 4 ID4 Bias	12 Bits
Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Optional LCP LNA Stage 4 ID4 Bias	12 Bits

Ku to X Band Converter

ESTIMATED DATA RATE 146 BITS/SECOND

Digital Monitor Points

Module Serial Number	16 Bits
Output Total Power Measurement #1	16 Bits
Output Total Power Measurement #2	16 Bits
Output Total Power Measurement #3	16 Bits
Output Total Power Measurement #4	16 Bits
Monitor Power Supplies	64 Bits
LO #1 In Lock	1 Bit
LO #2 In Lock	1 Bit

X-Band Front End

ESTIMATED DATA RATE 1.5 KBITS/SECOND

Digital Monitor Points

Cryo Off	1 Bit
Cryo Cool	1 Bit

Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Solar Switch 1	1 Bit
Solar Switch 2	1 Bit
Solar Step Attenuator	5 Bits
Solenoid Valve	1 Bit
Pump Request	1 Bit
Fridge Request	1 Bit
Manual/Computer	1 Bit
Band Code	4 Bits
Receiver Serial Number	6 Bits
Receiver Modification Level	2 Bits
RCP LNA Stage 1 VD1	16 Bits
RCP LNA Stage 1 ID1	16 Bits
RCP LNA Stage 1 VG1	16 Bits
RCP LNA Stage 2 VD2	16 Bits
RCP LNA Stage 2 ID2	16 Bits
RCP LNA Stage 2 VG2	16 Bits
RCP LNA Stage 3 VD3	16 Bits
RCP LNA Stage 3 ID3	16 Bits
RCP LNA Stage 3 VG3	16 Bits
RCP LNA Stage 4 VD4	16 Bits
RCP LNA Stage 4 ID4	16 Bits
RCP LNA Stage 4 VG4	16 Bits
LCP LNA Stage 1 VD1	16 Bits
LCP LNA Stage 1 ID1	16 Bits
LCP LNA Stage 1 VG1	16 Bits
LCP LNA Stage 2 VD2	16 Bits
LCP LNA Stage 2 ID2	16 Bits
LCP LNA Stage 2 VG2	16 Bits
LCP LNA Stage 3 VD3	16 Bits
LCP LNA Stage 3 ID3	16 Bits
LCP LNA Stage 3 VG3	16 Bits
LCP LNA Stage 4 VD4	16 Bits
LCP LNA Stage 4 ID4	16 Bits
LCP LNA Stage 4 VG4	16 Bits
OPTIONAL RCP LNA Stage 1 VD1	16 Bits
OPTIONAL RCP LNA Stage 1 ID1	16 Bits
OPTIONAL RCP LNA Stage 1 VG1	16 Bits
OPTIONAL RCP LNA Stage 2 VD2	16 Bits
OPTIONAL RCP LNA Stage 2 ID2	16 Bits
OPTIONAL RCP LNA Stage 2 VG2	16 Bits
OPTIONAL RCP LNA Stage 3 VD3	16 Bits
OPTIONAL RCP LNA Stage 3 ID3	16 Bits
OPTIONAL RCP LNA Stage 3 VG3	16 Bits
OPTIONAL RCP LNA Stage 4 VD4	16 Bits
OPTIONAL RCP LNA Stage 4 ID4	16 Bits
OPTIONAL RCP LNA Stage 4 VG4	16 Bits
OPTIONAL LCP LNA Stage 1 VD1	16 Bits
OPTIONAL LCP LNA Stage 1 ID1	16 Bits
OPTIONAL LCP LNA Stage 1 VG1	16 Bits
OPTIONAL LCP LNA Stage 2 VD2	16 Bits
OPTIONAL LCP LNA Stage 2 ID2	16 Bits
OPTIONAL LCP LNA Stage 2 VG2	16 Bits
OPTIONAL LCP LNA Stage 3 VD3	16 Bits

OPTIONAL LCP LNA Stage 3 ID3	16 Bits
OPTIONAL LCP LNA Stage 3 VG3	16 Bits
OPTIONAL LCP LNA Stage 4 VD4	16 Bits
OPTIONAL LCP LNA Stage 4 ID4	16 Bits
OPTIONAL LCP LNA Stage 4 VG4	16 Bits
15K Temperature	16 Bits
50K Temperature	16 Bits
300K Temperature	16 Bits
Dewar Vacuum Pressure	16 Bits
Pump Vacuum Pressure	16 Bits
Noise Source Cal Voltage	16 Bits
Noise Source Cal Current	16 Bits
Solar Noise Cal Voltage	16 Bits
Solar Noise Cal Current	16 Bits
+15 Volts	16 Bits
-15 Volts	16 Bits
+5 Volts	16 Bits
+28 Volts	16 Bits
RCP LED	16 Bits
LCP LED	16 Bits
Optional Power Detector RCP-IF	16 Bits
Optional Power Detector LCP-IF	16 Bits
Optional Power Detector LO	16 Bits
Spare Analog Monitor 1	16 Bits
Spare Analog Monitor 2	16 Bits
Spare Analog Monitor 3	16 Bits
Readback of RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of LCP LNA Stage 2 VD2 Bias	12 Bits
Readback of LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of LCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 VD4 Bias	12 Bits

Readback of Optional LCP LNA Stage 4 ID4 Bias	12 Bits

Commands

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Set Solar Switch 1	1 Bit
Set Solar Switch 2	1 Bit
Set Solar Step Attenuator	5 Bits
RCP LNA Stage 1 VD1 Bias	12 Bits
RCP LNA Stage 1 ID1 Bias	12 Bits
RCP LNA Stage 2 VD2 Bias	12 Bits
RCP LNA Stage 2 ID2 Bias	12 Bits
RCP LNA Stage 3 VD3 Bias	12 Bits
RCP LNA Stage 3 ID3 Bias	12 Bits
RCP LNA Stage 4 VD4 Bias	12 Bits
RCP LNA Stage 4 ID4 Bias	12 Bits
LCP LNA Stage 1 VD1 Bias	12 Bits
LCP LNA Stage 1 ID1 Bias	12 Bits
LCP LNA Stage 2 VD2 Bias	12 Bits
LCP LNA Stage 2 ID2 Bias	12 Bits
LCP LNA Stage 3 VD3 Bias	12 Bits
LCP LNA Stage 3 ID3 Bias	12 Bits
LCP LNA Stage 4 VD4 Bias	12 Bits
LCP LNA Stage 4 ID4 Bias	12 Bits
Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Optional LCP LNA Stage 4 ID4 Bias	12 Bits

C-Band Front End

ESTIMATED DATA RATE 1.5 KBITS/SECOND

Digital Monitor Points

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit

Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Solar Switch 1	1 Bit
Solar Switch 2	1 Bit
Solar Step Attenuator	5 Bits
Solenoid Valve	1 Bit
Pump Request	1 Bit
Fridge Request	1 Bit
Manual/Computer	1 Bit
Band Code	4 Bits
Receiver Serial Number	6 Bits
Receiver Modification Level	2 Bits
RCP LNA Stage 1 VD1	16 Bits
RCP LNA Stage 1 ID1	16 Bits
RCP LNA Stage 1 VG1	16 Bits
RCP LNA Stage 2 VD2	16 Bits
RCP LNA Stage 2 ID2	16 Bits
RCP LNA Stage 2 VG2	16 Bits
RCP LNA Stage 3 VD3	16 Bits
RCP LNA Stage 3 ID3	16 Bits
RCP LNA Stage 3 VG3	16 Bits
RCP LNA Stage 4 VD4	16 Bits
RCP LNA Stage 4 ID4	16 Bits
RCP LNA Stage 4 VG4	16 Bits
LCP LNA Stage 1 VD1	16 Bits
LCP LNA Stage 1 ID1	16 Bits
LCP LNA Stage 1 VG1	16 Bits
LCP LNA Stage 2 VD2	16 Bits
LCP LNA Stage 2 ID2	16 Bits
LCP LNA Stage 2 VG2	16 Bits
LCP LNA Stage 3 VD3	16 Bits
LCP LNA Stage 3 ID3	16 Bits
LCP LNA Stage 3 VG3	16 Bits
LCP LNA Stage 4 VD4	16 Bits
LCP LNA Stage 4 ID4	16 Bits
LCP LNA Stage 4 VG4	16 Bits
OPTIONAL RCP LNA Stage 1 VD1	16 Bits
OPTIONAL RCP LNA Stage 1 ID1	16 Bits
OPTIONAL RCP LNA Stage 1 VG1	16 Bits
OPTIONAL RCP LNA Stage 2 VD2	16 Bits
OPTIONAL RCP LNA Stage 2 ID2	16 Bits
OPTIONAL RCP LNA Stage 2 VG2	16 Bits
OPTIONAL RCP LNA Stage 3 VD3	16 Bits
OPTIONAL RCP LNA Stage 3 ID3	16 Bits
OPTIONAL RCP LNA Stage 3 VG3	16 Bits
OPTIONAL RCP LNA Stage 4 VD4	16 Bits
OPTIONAL RCP LNA Stage 4 ID4	16 Bits
OPTIONAL RCP LNA Stage 4 VG4	16 Bits
OPTIONAL LCP LNA Stage 1 VD1	16 Bits
OPTIONAL LCP LNA Stage 1 ID1	16 Bits
OPTIONAL LCP LNA Stage 1 VG1	16 Bits
OPTIONAL LCP LNA Stage 2 VD2	16 Bits
OPTIONAL LCP LNA Stage 2 ID2	16 Bits
OPTIONAL LCP LNA Stage 2 VG2	16 Bits
OPTIONAL LCP LNA Stage 3 VD3	16 Bits
OPTIONAL LCP LNA Stage 3 ID3	16 Bits

OPTIONAL LCP LNA Stage 3 VG3	16 Bits
OPTIONAL LCP LNA Stage 4 VD4	16 Bits
OPTIONAL LCP LNA Stage 4 ID4	16 Bits
OPTIONAL LCP LNA Stage 4 VG4	16 Bits
15K Temperature	16 Bits
50K Temperature	16 Bits
300K Temperature	16 Bits
Dewar Vacuum Pressure	16 Bits
Pump Vacuum Pressure	16 Bits
Noise Source Cal Voltage	16 Bits
Noise Source Cal Current	16 Bits
Solar Noise Cal Voltage	16 Bits
Solar Noise Cal Current	16 Bits
+15 Volts	16 Bits
-15 Volts	16 Bits
+5 Volts	16 Bits
+28 Volts	16 Bits
RCP LED	16 Bits
LCP LED	16 Bits
Optional Power Detector RCP-IF	16 Bits
Optional Power Detector LCP-IF	16 Bits
Optional Power Detector LO	16 Bits
Spare Analog Monitor 1	16 Bits
Spare Analog Monitor 2	16 Bits
Spare Analog Monitor 3	16 Bits
Readback of RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of LCP LNA Stage 2 VD2 Bias	12 Bits
Readback of LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of LCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 ID4 Bias	12 Bits

Commands

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Set Solar Switch 1	1 Bit
Set Solar Switch 2	1 Bit
Set Solar Step Attenuator	5 Bits
RCP LNA Stage 1 VD1 Bias	12 Bits
RCP LNA Stage 1 ID1 Bias	12 Bits
RCP LNA Stage 2 VD2 Bias	12 Bits
RCP LNA Stage 2 ID2 Bias	12 Bits
RCP LNA Stage 3 VD3 Bias	12 Bits
RCP LNA Stage 3 ID3 Bias	12 Bits
RCP LNA Stage 4 VD4 Bias	12 Bits
RCP LNA Stage 4 ID4 Bias	12 Bits
LCP LNA Stage 1 VD1 Bias	12 Bits
LCP LNA Stage 1 ID1 Bias	12 Bits
LCP LNA Stage 2 VD2 Bias	12 Bits
LCP LNA Stage 2 ID2 Bias	12 Bits
LCP LNA Stage 3 VD3 Bias	12 Bits
LCP LNA Stage 3 ID3 Bias	12 Bits
LCP LNA Stage 4 VD4 Bias	12 Bits
LCP LNA Stage 4 ID4 Bias	12 Bits
Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Optional LCP LNA Stage 4 ID4 Bias	12 Bits

S-Band Front End

ESTIMATED DATA RATE 1.5 KBITS/SECOND

Digital Monitor Points

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Solar Switch 1	1 Bit

Solar Switch 2	1 Bit
Solar Step Attenuator	5 Bits
Solenoid Valve	1 Bit
Pump Request	1 Bit
Fridge Request	1 Bit
Manual/Computer	1 Bit
Band Code	4 Bits
Receiver Serial Number	6 Bits
Receiver Modification Level	2 Bits
RCP LNA Stage 1 VD1	16 Bits
RCP LNA Stage 1 ID1	16 Bits
RCP LNA Stage 1 VG1	16 Bits
RCP LNA Stage 2 VD2	16 Bits
RCP LNA Stage 2 ID2	16 Bits
RCP LNA Stage 2 VG2	16 Bits
RCP LNA Stage 3 VD3	16 Bits
RCP LNA Stage 3 ID3	16 Bits
RCP LNA Stage 3 VG3	16 Bits
RCP LNA Stage 4 VD4	16 Bits
RCP LNA Stage 4 ID4	16 Bits
RCP LNA Stage 4 VG4	16 Bits
LCP LNA Stage 1 VD1	16 Bits
LCP LNA Stage 1 ID1	16 Bits
LCP LNA Stage 1 VG1	16 Bits
LCP LNA Stage 2 VD2	16 Bits
LCP LNA Stage 2 ID2	16 Bits
LCP LNA Stage 2 VG2	16 Bits
LCP LNA Stage 3 VD3	16 Bits
LCP LNA Stage 3 ID3	16 Bits
LCP LNA Stage 3 VG3	16 Bits
LCP LNA Stage 4 VD4	16 Bits
LCP LNA Stage 4 ID4	16 Bits
LCP LNA Stage 4 VG4	16 Bits
OPTIONAL RCP LNA Stage 1 VD1	16 Bits
OPTIONAL RCP LNA Stage 1 ID1	16 Bits
OPTIONAL RCP LNA Stage 1 VG1	16 Bits
OPTIONAL RCP LNA Stage 2 VD2	16 Bits
OPTIONAL RCP LNA Stage 2 ID2	16 Bits
OPTIONAL RCP LNA Stage 2 VG2	16 Bits
OPTIONAL RCP LNA Stage 3 VD3	16 Bits
OPTIONAL RCP LNA Stage 3 ID3	16 Bits
OPTIONAL RCP LNA Stage 3 VG3	16 Bits
OPTIONAL RCP LNA Stage 4 VD4	16 Bits
OPTIONAL RCP LNA Stage 4 ID4	16 Bits
OPTIONAL RCP LNA Stage 4 VG4	16 Bits
OPTIONAL LCP LNA Stage 1 VD1	16 Bits
OPTIONAL LCP LNA Stage 1 ID1	16 Bits
OPTIONAL LCP LNA Stage 1 VG1	16 Bits
OPTIONAL LCP LNA Stage 2 VD2	16 Bits
OPTIONAL LCP LNA Stage 2 ID2	16 Bits
OPTIONAL LCP LNA Stage 2 VG2	16 Bits
OPTIONAL LCP LNA Stage 3 VD3	16 Bits
OPTIONAL LCP LNA Stage 3 ID3	16 Bits
OPTIONAL LCP LNA Stage 3 VG3	16 Bits
OPTIONAL LCP LNA Stage 4 VD4	16 Bits
OPTIONAL LCP LNA Stage 4 ID4	16 Bits

OPTIONAL LCP LNA Stage 4 VG4	16 Bits
15K Temperature	16 Bits
50K Temperature	16 Bits
300K Temperature	16 Bits
Dewar Vacuum Pressure	16 Bits
Pump Vacuum Pressure	16 Bits
Noise Source Cal Voltage	16 Bits
Noise Source Cal Current	16 Bits
Solar Noise Cal Voltage	16 Bits
Solar Noise Cal Current	16 Bits
+15 Volts	16 Bits
-15 Volts	16 Bits
+5 Volts	16 Bits
+28 Volts	16 Bits
RCP LED	16 Bits
LCP LED	16 Bits
Optional Power Detector RCP-IF	16 Bits
Optional Power Detector LCP-IF	16 Bits
Optional Power Detector LO	16 Bits
Spare Analog Monitor 1	16 Bits
Spare Analog Monitor 2	16 Bits
Spare Analog Monitor 3	16 Bits
Readback of RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of LCP LNA Stage 2 VD2 Bias	12 Bits
Readback of LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of LCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 ID4 Bias	12 Bits

Commands

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Set Solar Switch 1	1 Bit
Set Solar Switch 2	1 Bit
Set Solar Step Attenuator	5 Bits
RCP LNA Stage 1 VD1 Bias	12 Bits
RCP LNA Stage 1 ID1 Bias	12 Bits
RCP LNA Stage 2 VD2 Bias	12 Bits
RCP LNA Stage 2 ID2 Bias	12 Bits
RCP LNA Stage 3 VD3 Bias	12 Bits
RCP LNA Stage 3 ID3 Bias	12 Bits
RCP LNA Stage 4 VD4 Bias	12 Bits
RCP LNA Stage 4 ID4 Bias	12 Bits
LCP LNA Stage 1 VD1 Bias	12 Bits
LCP LNA Stage 1 ID1 Bias	12 Bits
LCP LNA Stage 2 VD2 Bias	12 Bits
LCP LNA Stage 2 ID2 Bias	12 Bits
LCP LNA Stage 3 VD3 Bias	12 Bits
LCP LNA Stage 3 ID3 Bias	12 Bits
LCP LNA Stage 4 VD4 Bias	12 Bits
LCP LNA Stage 4 ID4 Bias	12 Bits
Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Optional LCP LNA Stage 4 ID4 Bias	12 Bits

L-Band Front End

ESTIMATED DATA RATE 1.5 KBITS/SECOND

Digital Monitor Points

Cryo Off	1 Bit
Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Solar Switch 1	1 Bit
Solar Switch 2	1 Bit
Solar Step Attenuator	5 Bits

Solenoid Valve	1 Bit
Pump Request	1 Bit
Fridge Request	1 Bit
Manual/Computer	1 Bit
Band Code	4 Bits
Receiver Serial Number	6 Bits
Receiver Modification Level	2 Bits
RCP LNA Stage 1 VD1	16 Bits
RCP LNA Stage 1 ID1	16 Bits
RCP LNA Stage 1 VG1	16 Bits
RCP LNA Stage 2 VD2	16 Bits
RCP LNA Stage 2 ID2	16 Bits
RCP LNA Stage 2 VG2	16 Bits
RCP LNA Stage 3 VD3	16 Bits
RCP LNA Stage 3 ID3	16 Bits
RCP LNA Stage 3 VG3	16 Bits
RCP LNA Stage 4 VD4	16 Bits
RCP LNA Stage 4 ID4	16 Bits
RCP LNA Stage 4 VG4	16 Bits
LCP LNA Stage 1 VD1	16 Bits
LCP LNA Stage 1 ID1	16 Bits
LCP LNA Stage 1 VG1	16 Bits
LCP LNA Stage 2 VD2	16 Bits
LCP LNA Stage 2 ID2	16 Bits
LCP LNA Stage 2 VG2	16 Bits
LCP LNA Stage 3 VD3	16 Bits
LCP LNA Stage 3 ID3	16 Bits
LCP LNA Stage 3 VG3	16 Bits
LCP LNA Stage 4 VD4	16 Bits
LCP LNA Stage 4 ID4	16 Bits
LCP LNA Stage 4 VG4	16 Bits
OPTIONAL RCP LNA Stage 1 VD1	16 Bits
OPTIONAL RCP LNA Stage 1 ID1	16 Bits
OPTIONAL RCP LNA Stage 1 VG1	16 Bits
OPTIONAL RCP LNA Stage 2 VD2	16 Bits
OPTIONAL RCP LNA Stage 2 ID2	16 Bits
OPTIONAL RCP LNA Stage 2 VG2	16 Bits
OPTIONAL RCP LNA Stage 3 VD3	16 Bits
OPTIONAL RCP LNA Stage 3 ID3	16 Bits
OPTIONAL RCP LNA Stage 3 VG3	16 Bits
OPTIONAL RCP LNA Stage 4 VD4	16 Bits
OPTIONAL RCP LNA Stage 4 ID4	16 Bits
OPTIONAL RCP LNA Stage 4 VG4	16 Bits
OPTIONAL LCP LNA Stage 1 VD1	16 Bits
OPTIONAL LCP LNA Stage 1 ID1	16 Bits
OPTIONAL LCP LNA Stage 1 VG1	16 Bits
OPTIONAL LCP LNA Stage 2 VD2	16 Bits
OPTIONAL LCP LNA Stage 2 ID2	16 Bits
OPTIONAL LCP LNA Stage 2 VG2	16 Bits
OPTIONAL LCP LNA Stage 3 VD3	16 Bits
OPTIONAL LCP LNA Stage 3 ID3	16 Bits
OPTIONAL LCP LNA Stage 3 VG3	16 Bits
OPTIONAL LCP LNA Stage 4 VD4	16 Bits
OPTIONAL LCP LNA Stage 4 ID4	16 Bits
OPTIONAL LCP LNA Stage 4 VG4	16 Bits
15K Temperature	16 Bits

50K Temperature	16 Bits
300K Temperature	16 Bits
Dewar Vacuum Pressure	16 Bits
Pump Vacuum Pressure	16 Bits
Noise Source Cal Voltage	16 Bits
Noise Source Cal Current	16 Bits
Solar Noise Cal Voltage	16 Bits
Solar Noise Cal Current	16 Bits
+15 Volts	16 Bits
-15 Volts	16 Bits
+5 Volts	16 Bits
+28 Volts	16 Bits
RCP LED	16 Bits
LCP LED	16 Bits
Optional Power Detector RCP-IF	16 Bits
Optional Power Detector LCP-IF	16 Bits
Optional Power Detector LO	16 Bits
Spare Analog Monitor 1	16 Bits
Spare Analog Monitor 2	16 Bits
Spare Analog Monitor 3	16 Bits
Readback of RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of LCP LNA Stage 2 VD2 Bias	12 Bits
Readback of LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of LCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Readback of Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Readback of Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Readback of Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Readback of Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Readback of Optional LCP LNA Stage 4 ID4 Bias	12 Bits

ands

Cryo Off	1 Bit

Cryo Cool	1 Bit
Cryo Stress	1 Bit
Cryo Heat	1 Bit
Cryo Vacuum Pumping	1 Bit
Set Solar Switch 1	1 Bit
Set Solar Switch 2	1 Bit
Set Solar Step Attenuator	5 Bits
RCP LNA Stage 1 VD1 Bias	12 Bits
RCP LNA Stage 1 ID1 Bias	12 Bits
RCP LNA Stage 2 VD2 Bias	12 Bits
RCP LNA Stage 2 ID2 Bias	12 Bits
RCP LNA Stage 3 VD3 Bias	12 Bits
RCP LNA Stage 3 ID3 Bias	12 Bits
RCP LNA Stage 4 VD4 Bias	12 Bits
RCP LNA Stage 4 ID4 Bias	12 Bits
LCP LNA Stage 1 VD1 Bias	12 Bits
LCP LNA Stage 1 ID1 Bias	12 Bits
LCP LNA Stage 2 VD2 Bias	12 Bits
LCP LNA Stage 2 ID2 Bias	12 Bits
LCP LNA Stage 3 VD3 Bias	12 Bits
LCP LNA Stage 3 ID3 Bias	12 Bits
LCP LNA Stage 4 VD4 Bias	12 Bits
LCP LNA Stage 4 ID4 Bias	12 Bits
Optional RCP LNA Stage 1 VD1 Bias	12 Bits
Optional RCP LNA Stage 1 ID1 Bias	12 Bits
Optional RCP LNA Stage 2 VD2 Bias	12 Bits
Optional RCP LNA Stage 2 ID2 Bias	12 Bits
Optional RCP LNA Stage 3 VD3 Bias	12 Bits
Optional RCP LNA Stage 3 ID3 Bias	12 Bits
Optional RCP LNA Stage 4 VD4 Bias	12 Bits
Optional RCP LNA Stage 4 ID4 Bias	12 Bits
Optional LCP LNA Stage 1 VD1 Bias	12 Bits
Optional LCP LNA Stage 1 ID1 Bias	12 Bits
Optional LCP LNA Stage 2 ID2 Bias	12 Bits
Optional LCP LNA Stage 3 VD3 Bias	12 Bits
Optional LCP LNA Stage 3 ID3 Bias	12 Bits
Optional LCP LNA Stage 4 VD4 Bias	12 Bits
Optional LCP LNA Stage 4 ID4 Bias	12 Bits

P-Band Front End

ESTIMATED DATA RATE 65 BITS/SECOND

Digital Monitor Points

23 dB Solar Attenuator Applied/Not Applied	1 Bit
Power Supply Voltages	64 Bits

Commands

4-Band Front End

ESTIMATED DATA RATE 65 BITS/SECOND

Digital Monitor Points

23 dB Solar Attenuator Applied/Not Applied	1 Bit
Power Supply Voltages	64 Bits

Commands

23 dB Solar Attenuator Applied/Not Applied	1 Bit

VHF/UHF Front End (for Phase II)

ESTIMATED DATA RATE 65 BITS/SECOND

Digital Monitor Points

23 dB Solar Attenuator Applied/Not Applied	1 Bit
Power Supply Voltages	64 Bits

Commands

23 dB Solar Attenuator Applied/Not Applied	1 Bit

Water Vapor Radiometer

ESTIMATED DATA RATE 640 BITS/SECOND

(Each Monitor Point stores up to 300,000 counts)(19 bits needed)
(data rate estimated to be 80 bytes/sec)
(All measurements done at LCP)
The design of the WVR for the EVLA probably will change from what it is now. Presently, mea are made just below, on, and just above the water vapor line at 22.235 GHZ. In the final design, measurements may be made at 5 places rather than the 3 just mentioned. A dynamic range of at must be achieved.

Digital Monitor Points

Below Water Vapor Line Cal On	19 Bits
Below Water Vapor Line Cal Off	19 Bits
On Water Vapor Line Cal On	19 Bits
On Water Vapor Line Cal Off	19 Bits
Above Water Vapor Line Cal On	19 Bits
Above Water Vapor Line Cal Off	19 Bits
IF Plate Temperatures (top, bottom, side of plate)	16 Bits
+15 Volt Power Supply Voltage	16 Bits
-15 Volt Power Supply Voltage	16 Bits

+5 Volt Power Supply Voltage	16 Bits
-5 Volt Power Supply Voltage	16 Bits
+28 Volt Power Supply Voltage	16 Bits
-28 Volt Power Supply Voltage	16 Bits
Ground Voltage	16 Bits
+15 Volt Power Supply Current	16 Bits
-15 Volt Power Supply Current	16 Bits
+5 Volt Power Supply Current	16 Bits
-5 Volt Power Supply Current	16 Bits
+28 Volt Power Supply Current	16 Bits
-28 Volt Power Supply Current	16 Bits
Ground Current	16 Bits

CRYO

Most monitor and control points for the refrigerators are currently listed under the receivers. These may be moved to the Cryo section, as it would be desirable to control all of the refrigerators from a single Cryo interface. It would be preferable to remove all of the high voltage switching from the digital card cages of the receivers. Monitor and control of the compressors may be desirable, and may be added to this section.

ESTIMATED DATA RATE 64 BITS/SECOND

Analog Monitor Points	Scale	Nom	Range (V)	Range (Units)	Resolution
Vacuum Pump Current	1 A				0.3 mA
Vacuum Valve Current	1 A				0.3 mA
Helium Supply Pressure	100psi	2.7	2.4/3.0	240/300 psi	0.03 psi
Helium Return Pressure	100psi	.75	.5/1.0	50/100 psi	0.03 psi

UTILITY INTERFACE

There is currently a completely separate monitor and control system at the VLA (the Wye Monitor) for certain operations that must be functional, even in the event of a power outage or waveguide failure. At the antennas, these functions include items such as emergency stops, reset of the ACU, and smoke alarms. In the control building, the functions include correlator UPS, computer UPS, generator monitor and control, HVAC for the correlator and computer systems, and status lines for the modcomp computers. At this time, more discussion is needed to determine how many of these functions, if any, need to be in a completely separate system. Any of these monitor and control points that do not need to be separate can be integrated into the EVLA monitor and control system.

A UPS at each EVLA antenna could protect the antenna computer and other circuits from power problems. If a separate fiber is run for safety critical items, it probably would have to follow the same path as the main fiber. If the main fiber is damaged, the safety critical fiber is likely to be damaged also. This brings into question the advantage of having a separate monitor and control system similar to the present Wye Monitor system.

CONTROL BUILDING MONITOR AND CONTROL

Maser

ESTIMATED DATA RATE 512 BITS/SECOND

The Swiss maser currently in use at the VLA will be replaced by a Sigma Tau Maser. The Sigma Tau Maser is expected to arrive in 2004. The new Sigma Tau maser is monitored and controlled by an RS-23 interface (Unlike the VLBA masers). When this maser is used for the EVLA, an interface must be built between the RS-232 of the Sigma Tau and the EVLA monitor and control system. One possibility is to use a MIB. Another option would be to directly connect the RS-232 port of the maser to the EVLA control computer.

It is desirable to monitor the maser once per second, and to record the monitor points in the monitor data once per minute. The data rate will be very low.

SIGMA TAU MASER MONITOR AND CONTROL POINTS

ANALOG MONITOR POINTS
405.7 KHZ Second IF Power
Cavity Register Voltage
10 MHZ VCXO Control Voltage
Right Ion Pump Current
Left Ion Pump Current
Upper Ion Pump Current
1400 MHZ Multiplier output Power Monitor
Battery Charging Current (Ich)
(typ = 0.05 A, max = 2.0 A)
10 MHZ VCXO Heater Monitor
Source (Hydrogen) pressure Control
Source Discharge Osc. Current (Is)
Main Magnetic Field Coil Current
Cavity Auto Tune Correction Averager
+5 Volts Supply To Receiver
+15 Volts Supply To Receiver
-15 Volts Supply To Receiver
Cavity Heater Voltage
Outer Oven Heater Voltage
Lower Support Heater Voltage
Top Plate Heater Voltage
Pirani Gauge Sensor Heater Voltage
Palladium Heater Voltage
Right Vac. Ion Pump Voltage (after fuse)
Left Vac. Ion Pump Voltage (after fuse)
Upper Vac. Ion Pump Voltage (after fuse)
+23.7 Volts Receiver Regulated Voltage
+18 Volts Receiver Regulated Voltage
Battery Voltage
(27.5 V => fully charged,
22 V => fully discharged)
DC Out From Right (AC1) Supply
DC Out From Left (AC2) Supply

Externally Supplied DC Input Voltage
(Used When Transporting or Backup)
Inter Shield Magnetic Servo Current

DIGITAL MONITOR/CONTROL POINTS

SYNTHESIZER FREQUENCY CONTROL

Mon/Con	Bit Pos	Function
Mon/Con	0-3	External Freq. Control Digit (0-9) In Step 4.66*10**-17 Of F (Maser Freq.)
Mon/Con	4-7	Internal Freq. Control Digit (0-9) In step 4.66*10**-17 Of F (Maser Freq.)
Mon/Con	0-3	External Freq. Control Digit (0-9) In Step 4.66*10**-16 Of F (Maser Freq.)
Mon/Con	4-7	Internal Freq. Control Digit (0-9) In step 4.66*10**-16 Of F (Maser Freq.)
Mon/Con	0-3	External Freq. Control Digit (0-9) In Step 4.66*10**-15 Of F (Maser Freq.)
Mon/Con	4-7	Internal Freq. Control Digit (0-9) In step 4.66*10**-15 Of F (Maser Freq.)
Mon/Con	0-3	External Freq. Control Digit (0-9) In Step 4.66*10**-14 Of F (Maser Freq.)
Mon/Con	4-7	Internal Freq. Control Digit (0-9) In step 4.66*10**-14 Of F (Maser Freq.)
Mon/Con	0-3	External Freq. Control Digit (0-9) In Step 4.66*10**-13 Of F (Maser Freq.)
Mon/Con	4-7	Internal Freq. Control Digit (0-9) In step 4.66*10**-13 Of F (Maser Freq.)
Mon/Con	0-3	External Freq. Control Digit (0-9) In Step 4.66*10**-12 Of F (Maser Freq.)
Mon/Con	4-7	Internal Freq. Control Digit (0-9) In step 4.66*10**-12 Of F (Maser Freq.)
Mon/Con	0-3	External Freq. Control Digit (0-9) In Step 4.66*10**-11 Of F (Maser Freq.)
Mon/Con	4-7	Internal Freq. Control Digit (0-9) In step 4.66*10**-11 Of F (Maser Freq.)
Mon/Con	0-3	External Freq. Control Digit (0-9) In Step 4.66*10**-10 Of F (Maser Freq.)
Mon/Con	4-7	Internal Freq. Control Digit (0-9) In step 4.66*10**-10 Of F (Maser Freq.)
Mon	0-7	Maser Serial Number (BCD)
Con	8	Select Synthesizer Setting (0 = External, 1 = Internal)
Mon		Various Status Indicators (Each One Bit)
		Maser Running On Battery Power (1 = True)
		10 MHZ VCXO Lock Indicator (1 = Lock, 0 = Unlock)
		Cavity Tuning Register Lower Limit (1 = In Range, 0 = At Limit)
		Cavity Tuning Register upper Limit (1 = In Range,) = At Limit)
		Hardware Switch To Control Synthesizer (1 = Internal, 0 = External)
		Software Control Of Synthesizer (1 = External, 0 = Internal)

Weather Station Subsystem

ESTIMATED DATA RATE 240 BITS\SECOND

The Expanded VLA Weather Station subsystem main function may be replaced by WVR Systems on the VLA Antennas. If the WVR system works then the Weather station would be similar to what we have currently with a central station. However, if the WVR system doesn't work, it is then conceivable that additional stations could be placed at certain locations on each arm to provide better atmospheric coverag
Digital Monitor Points

+5 Volt Power Supply	16 Bits
+15 Volt Power Supply	16 Bits
-15 Volt Power Supply	16 Bits
Ground	16 Bits
Wind Speed	16 Bits
Wind Direction	16 Bits
Barometric Pressure	16 Bits
Temperature	16 Bits
Dewpoint Temperature	16 Bits
High Temperature	16 Bits
Low Temperature	16 Bits

Rain Gauge	16 Bits
Snow Gauge	16 Bits
Status Flags	16 Bits

Commands

Reset Weather Station	1 Bit
Reset Various Weather Station Instruments	16 Bits

The instrumentation would consist of:

A. Wind Speed - 5mV or better resolution. Rate 1 second.
B. Wind Direction - 5mV or better resolution. Rate 1 second.
C. Barometer - Digital - +/-10-25mb resolution. Rate 1 second.
D. Temperature - 5mV or better resolution. Rate 1 second.
E. Dewpoint - 5mV or better resolution. Rate 1 second.
F. High Temperature - 5mV or better resolution. Rate 1 seconds.
G. Low Temperature - 5mV or better resolution. Rate 1 seconds.

Possible

H. Rain Gauge - Digital .1 inch resolution 16 bits wide. Rate 1 second.
I. Snow Gauge - 5mV or better resolution. Rate 1 second.

Weather Station Status Monitors
Width could vary depending upon individual Status Flags or packed Status Flags. Rate 1 second.

Weather Station Reset Commands
Digital at least 1 bit wide. Would reset various equipment such as Rain Gauge, High Temperature, Low Temperature, Barometer, etc.

On a related note, the Expanded VLA would still have at each antenna wind speed units. These would feed directly into the ACU in order to provide a high wind stow function.

Atmospheric Phase Interferometer

ESTIMATED DATA RATE 25 BYTES\SECOND

In the present VLA, the API has a separate, unique monitor and control system. A PC running windows is the interface between the API and the VLA control computer in the control building. This PC is an integral part of the API, since it correlates the data. It is not yet clear how to monitor/control the API for the EVLA.

It is desirable that the EVLA monitor and control system control the API, because separate systems should be kept to a minimum. This could be accomplished by building an interface between the windows PC and the EVLA monitor and control system. This approach would not require a modification to the API.

A more expensive approach would be to change the design of the API to include a built in monitor and control interface. There is probably some advantage in keeping equipment compatible throughout NRAO, so if this approach is taken it would be desirable to involve the Greenbank and Chile sites since they utilize the same design of API.

The data rate from the API is estimated to be 25 bytes/second.

Digital Monitor Points
- Amplitude
- Phase
- RMS of VCO Lock Voltage
- Monitor Points

Structure Function Data Products
Temperature (at 3 points)

CORRELATOR

The Correlator Monitor and Control system will not be detailed in this report.

Ionospheric Phase Monitor

Information not yet available.

UPS – Control Building

Digital Monitor Points

Reduce Input Limit Control	1 Bit
Battery Voltage Low Monitor	1 Bit
Battery Not Available Monitor	1 Bit
UPS Overload Alarm Monitor	1 Bit
Inlet Air Over Temperature Monitor	1 Bit
Transfer Not Available Monitor	1 Bit
Retransfer Not Available Monitor	1 Bit
UPS Available Monitor	1 Bit
UPS on Bypass Monitor	1 Bit
5-Minute Shutdown Warning Monitor	1 Bit
Summary Alarm Monitor	1 Bit
Minor Alarm Monitor	1 Bit
Major Alarm Monitor	1 Bit
UPS Input Failure Monitor	1 Bit

Commands

Reduce Input Limit Current

HVAC – Control Building

Digital Monitor Points

Chiller Temperature	16 Bits
Condenser Temperature	16 Bits
Computer Airflow Monitor	16 Bits
Correlator Airflow Monitor	16 Bits
Chiller Hot Monitor	1 Bit
Chiller Cold Monitor	1 Bit
Condenser Hot Monitor	1 Bit

EVLA Site Generators

Digital Monitor Points

Start Generators Control	1 Bit
Generator Tie Breaker Open	1 Bit
SEC Utility Breaker Open	1 Bit

AC Control Voltage Present	1 Bit
#1 Day Tank Low Fuel	1 Bit
#2 Day Tank Low Fuel	1 Bit
Voltage/Frequency Fault	1 Bit
Load Shed Activated	1 Bit
Alarm Horn	1 Bit
Generator Circuit Breaker Status	1 Bit
Engine Start	1 Bit
Engine Running	1 Bit
Battery Failure	1 Bit
Engine Over Cranking	1 Bit
Generator Not Synchronized	1 Bit
Low Lube Oil	1 Bit
High Water Temperature	1 Bit
Load Limit	1 Bit

Commands

Start Generators	1 Bit

GPS Interface

Information not yet available.

Rubidium Interface

Information not yet available.

Central Reference Interface (Quantity 2)

Information not yet available.

LO Transmitter Interface (Quantity 2)

Information not yet available.

Maser Offset Interface (Quantity 2)

Information not yet available.

Software Watchdogs

Information not yet available.

DTS Receiver (Quantity 4)

Information not yet available.

Round Trip Phase Interface

Information not yet available.

EVLA to VLA Transition Mo

Information not yet available.

Round Trip Phase Interface

Information not yet available.