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Operational Performance of the EVLA Digital Transmission System

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ABSTRACT

The Expanded Very Large Array (EVLA) uses fiber optic technologies for the Digital Data Transmission, the Local Oscillator and Reference distribution, and all Monitor/Control functions. These signals are sent on separate fibers to each of the twenty-seven EVLA antennas. The Data Transmission System (DTS) is used to transmit the four digitized IF signals from the antennas to the Central Electronics Building. A sustained data rate of 10.24 Gbits/s per channel and 122.88 Gbits formatted per antenna is supported. Each IF signal uses a parallel interface of three synchronized single bit high-speed serial optical fiber transmission channels. Each set of three channels, twelve channels in total, is wavelength division multiplexed onto a single fiber. The formatted data are received and de-formatted before the data are sent to the correlator. The system configuration includes a CW laser, an Erbium Doped Fiber Amplifier, passive optical multiplexers, up to 22 km of standard single mode fiber and an APD optical receiver. This paper presents a complete description of the EVLA fiber system including specific component specifications. The calculated performance of the IF system is compared to the actual performance and resulting "Lesson Learned" are presented.

Keywords : Data Transmission System, Fiber optics, DWDM, OC192 SONET, NRAO, EVLA

1. INTRODUCTION

The Very Large Array, one of the world's premier astronomical radio telescopes, consists of 27 radio antennas configured in the shape of a 35 km diameter "Y". The VLA is located on the Plains of San Agustin fifty miles west of Socorro, New Mexico. Each antenna is 25 meters (81 feet) in diameter. The data from the antennas are combined electronically to give the resolution of an antenna 36km (22 miles) across, with the sensitivity of a dish 130 meters (422 feet) in diameter. The VLA is a radio frequency interferometer. The data from each pair of telescopes are correlated together to form interference patterns. The structure of these interference patterns, and how they change with time as the earth rotates, reflect the structure of radio sources. The project is intended to increase the sensitivity and spatial resolution of the VLA [1]. The Expanded Very Large Array (EVLA) will use fiber optics to send the digitized radio signals from each of the twenty-seven antennas to the correlator located in the central electronics building. The data will be transmitted using Wavelength Division Multiplexing, (WDM) on standard single mode fiber. The system requirements for the IF Data Transmission System are shown in Table 1.

Table 1. Digital Transmission System Design Parameters

Bit Rate:	10.24 Gbits/second per channel
WDM Channels:	12 channels
Channel Spacing:	200 GHz spacing
Channel Wavelengths:	C Band
Bit Error Rate:	Initial - 10^{-9}; End of life - 10^{-6}
Digital RMS SNR (Q):	Initial - 6; End of life - 4.7
Maximum fiber length:	21.6 km
Minimum fiber Length:	0.625 km
Operating Temperature:	-12C to 35C

2. SYSTEM CONFIGURATION

Figure 1 is a block diagram of the EVLA data transmission system. This diagram shows the entire data flow from the outputs of the digitizers in the antennas, through the fiber distribution system, and into the Wideband Interferometric Digital Architecture (WIDAR) correlator in the central electronics building. The scheme of digitizing in the antenna and using digital links to transfer the data back to the correlator was chosen to maximize performance of the IF transmission system.

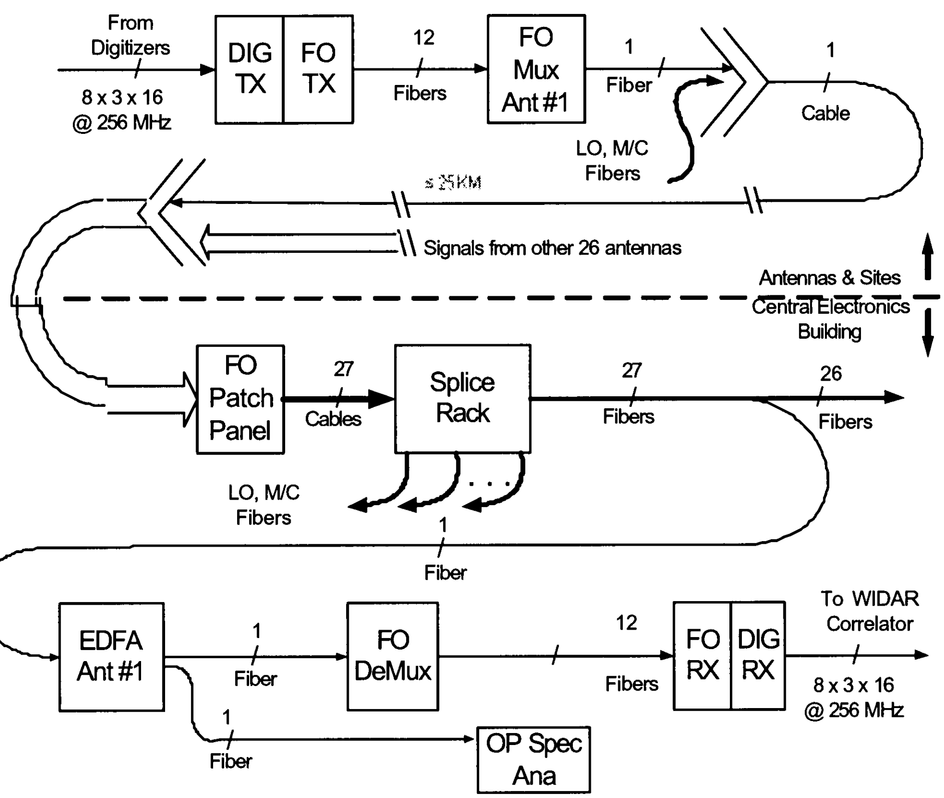


Figure 1. EVLA Data Transmission System Block Diagram

2.1 Transmitter (Antenna) Hardware Design

The transmitter/formatter hardware, located at the antenna, uses a Xilinx Virtex-2 series Field Programmable Gate Array (FPGA) to format the data and configure it into 16 serial data streams at 640 MHz. These data are then transferred to a 16:1 multiplexer made by AMCC for SONET OC192 communications. The device, which contains a phase locked voltage controlled oscillator and a 16-bit shift register, produces a 10.24 Gbits/s serial data stream. An integrated optical transmitter module, containing a laser, a modulator driver amplifier and an electro absorptive (EA) optical modulator, is used to launch the 10.24 Gbits/s signal onto each of the twelve fibers at twelve discrete wavelengths. The twelve fibers from the transmitters in each antenna are combined onto a single fiber using a passive 12:1 WDM fiber multiplexer.

2.2 Receiver Hardware Design

In the central electronics building, the twelve optical signals from each antenna are split apart using a passive WDM fiber de-multiplexer. Each optical carrier is fed to an OC192 optical receiver module, which contains a PIN diode, a trans-impedance amplifier and a limiting amplifier. The recovered 10.24 Gbits/s electrical data stream is fed to an AMCC OC-192 1:16 de-multiplexer IC. This device performs all clock and data recovery functions and de-multiplexe the data back into 16 serial data streams at 640MHz. These data are then transferred using Low Voltage Differential Signaling (LVDS) to a Xilinx Virtex-2 Field Programmable Gate Array (FPGA). The Xilinx FPGA performs all synchronization, error checking, re-clocking and de-multiplexing functions. Data output to the WIDAR Correlator is a 48 Bit wide LVDS word at 256 MHz.

2.3 Design Details

All of the designs for the Xilinx FPGAs are implemented using the VHSIC Hardware Description Language (VHDL – IEEE std 1076.3) utilizing Xilinx's Foundation ISE series software. The 10.24 Gbits/s data streams in and out of the AMCC chip set are CML logic levels. All other high-speed data signals utilize Low-Voltage-Differential-Signals or Positive-Emitter-Coupled-Logic standards. All monitor and control functions in each of the prototype modules are performed by a combination of a PIC 16F877 Microcontroller and a state machine implemented in a Xilinx FPGA. Each module is supplied 48VDC from which high efficiency DC/DC converters produce all other voltages locally.

2.4 Protocol

The Data Transmission System is based on a digital protocol utilizing a 160-bit frame structure and scrambling techniques. The protocol is described in detail in the EVLA Memorandum #33 - "Digital Transmission System Signaling Protocol" Version 2, November 2001. The frame is shown in Figure 2.

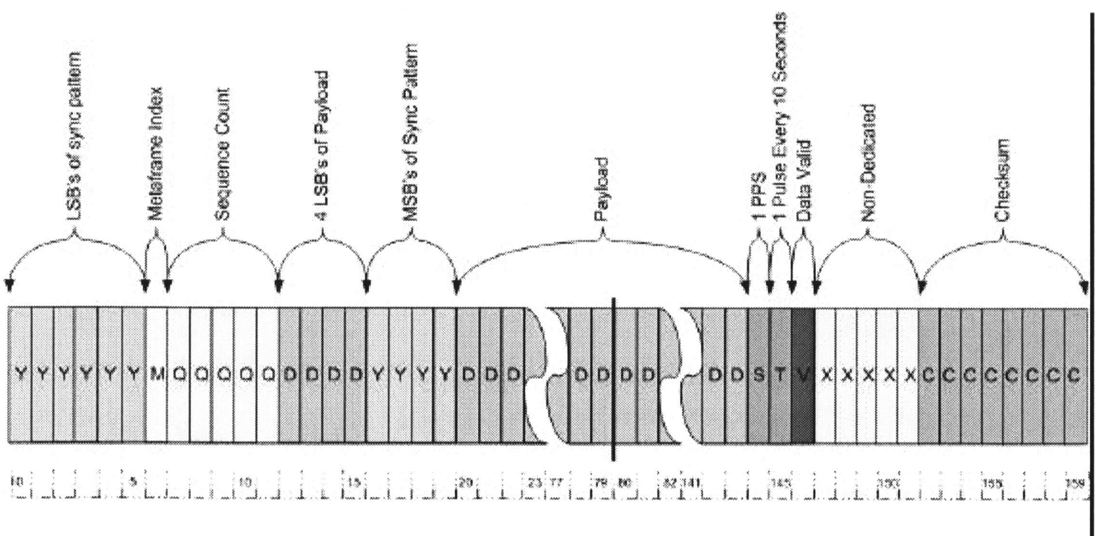


Figure 2: The Data Frame

The frame is composed of a divided 10-bit sync word, 1-bit meta-frame index, a 5-bit sequence count, a 1 pulse per second bit, a 1 pulse per 10 second bit, a data valid bit, 5 non-dedicated bits, and an 8-bit checksum. The first 4 payload bits are carried in locations 12 through 19 with the remaining 124 contiguous bits beginning with the bit location 20.

2.5 Formatter/De-formatter Configuration

The 256 MHz to 10.24 GHz rate conversion produces a natural 80 bit wide word. This word consists of 16 format bits and 64 data bits. Two consecutive 80-bit words are combined to produce a 160-bit frame. The 160-bit frame is produced at an effective 64 MHz clock rate and time division multiplexed by 160. To maintain the order of the frame, a 16-bit partitioning and re-ordering circuit is used. The circuit is placed between the input selector and the two 5:1 output multiplexers inside the formatter chip. This re-ordering is necessary to correct for the shuffling of the output selector.

A simplified formatter block diagram, Figure 3, shows the functional blocks including: a 64-bit input bus, input selector, partition and re-ordering circuit, the times 5 multiplexers, the output selector and the final times 16 multiplexer. Sixteen format bits are associated with each 64 data bit group. The format bits are used for the frame and Meta-frame synchronization, timing and transmission of the checksum word.

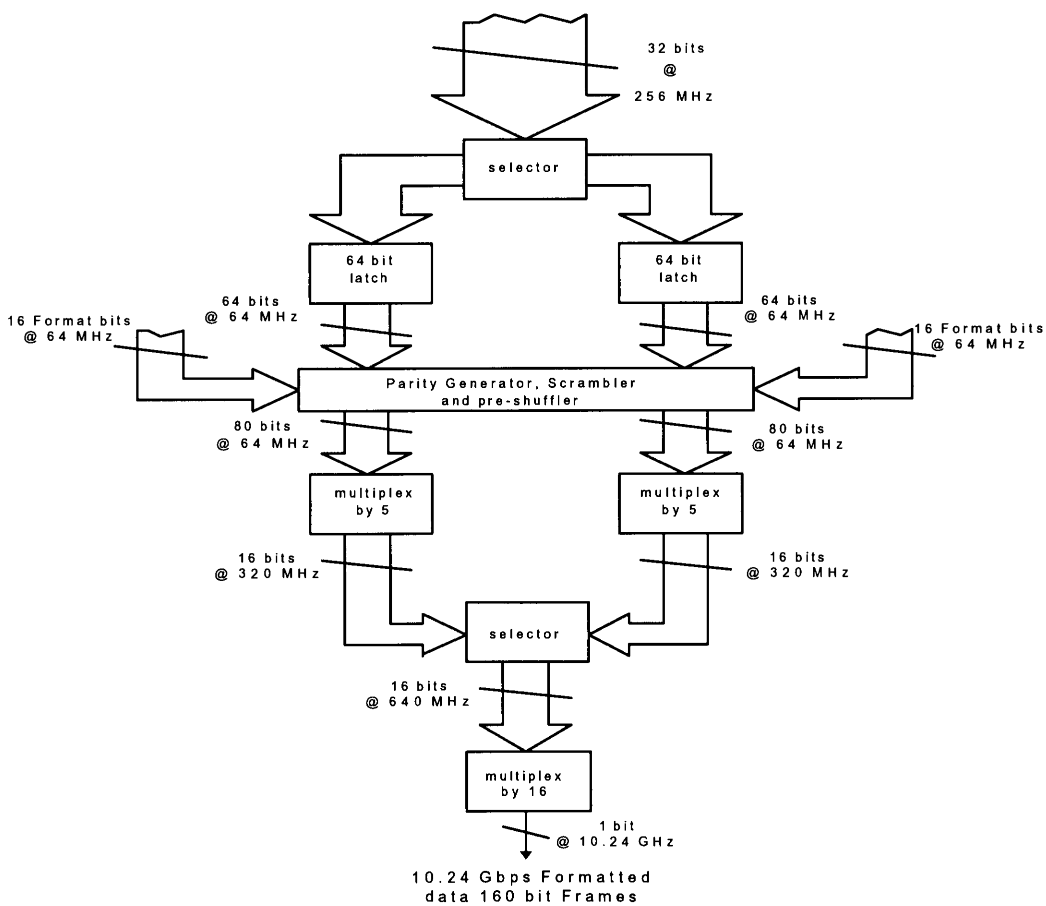


Figure 3. Simplified Formatter Block Diagram

A simplified de-formatter block diagram, showing the 16-bit input bus, the times 5 de-multiplexers, the de-shuffler and transfer switch, the pipelined barrel shifter, the descrambler, the 32 frame FIFO and the output times 4 multiplexer, is shown in Figure 4. Sixteen format bits are associated with each 64 data bit group. All signals on the input side of the 32-bit frame FIFO are aligned with the recovered data clock. Signals on the output side of the FIFO are aligned with the WIDAR correlator data clock.

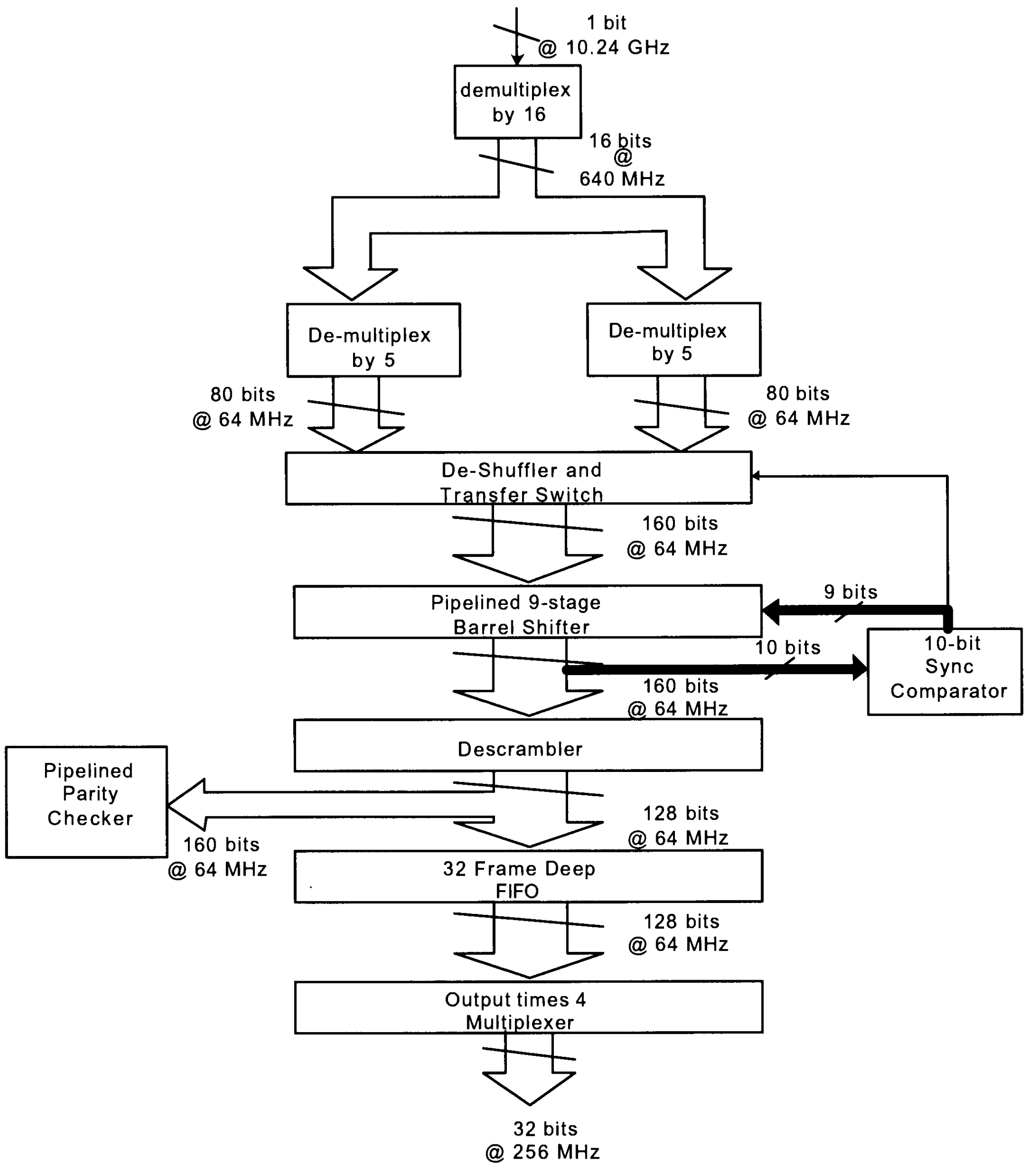


Figure 4. Simplified De-formatter Block Diagram

2.6 Channel Alignment

To maintain frame concurrence across the three optical channels used to transmit each IF polarization, the formatter inserts an identical incrementing count into each frame. This count is extracted by the three receivers, compared, and delays applied to the early arriving channels. The result is three simultaneously clocked 160-bit frames with the identical incrementing count.

2.7 Bit Error Rate Monitoring

The initial Bit Error Rate (BER) of the electro-optical fiber transmission system is expected to be 10^{-9}. However, the completed EVLA system will consist of 324 optical transmitters and receivers, several thousand miles of fiber and thousands of splices and reconfigurable connections. The capability to monitor the performance and integrity of such a complex system is essential. With this in mind, a mechanism for monitoring the Bit Error Rate of each 10.24 Gbits/sec optical channel is provided. Eight bits of each 160-bit frame are used as a checksum of the previous 152 bits. Each of these eight bits detects all odd numbers of errors introduced in 19-bit groups of data. While not an exhaustive error checking mechanism, this easily implemented approach should provide a reasonable indication of the health of each optical channel, in most cases allowing a degraded channel to be repaired before seriously affecting the astronomical data.

2.8 Scrambling

Frame Synchronous Scrambling (FSS) is used in the EVLA to provide adequate timing and to minimize low frequency content. The entire frame, except for the ten sync bits, will be scrambled by a static random pattern. A selected scrambling pattern is added modulo 2 to the remaining bits of the frame with the first generated scrambling bit added to the eighth frame bit. A Shift Register Generator (SRG) produces the scrambling pattern and the pattern "runs" continuously throughout the 153 bits of the pattern. A seven stage SRG producing a 127-bit length sequence is used. The 153-bit pattern produced with a generator polynomial of 1 + X^6 + X^7 and a seed or initial value of hexadecimal 46 has the random properties required. The scrambling pattern has 77 ones and 76 zeros achieving almost perfect DC balance. This scrambling technique reduces systematic jitter and ensures proper operation of the AC coupled optical receiver and the phase-locked loop in the clock recovery circuit.

3. FIBER PERFORMANCE

Standard Single Mode Fiber (SMF) was selected for the IF fiber optic Data Transmission System. The predicted attenuation for the SMF fiber is approximately 0.30 dB/km, or 6.6 dB over 22 km of fiber. The predicted pulse spread @ 10Gbits/s assuming ¼ wavelength is about 38ps [2]. The predicted performance of the fiber is summarized in Table 2. The table assumes a data rate of 10Gbits/s and a distance of 22 km to the farthest antenna.

Table 2. Predicted Fiber Performance for the EVLA IF System

Parameter	SMF
Attenuation Penalty (22 km)	6.6 dB
Dispersion Penalty (22 km)	2.0 dB
Pulse spread @ 10Gbits/s	38 ps
Non-Linear Effects [3]	Negligible
Max. Launch Power	2.5 dBm
Max. Laser Spectral Width [4]	0.1 nm

3.1 Loss Budget

The optical attenuation loss budget is shown in Table 3. A total attenuation of about -25.4 dBm is predicted. An EDF with an optical gain of 12 dB is included in the loss budget. When the optical gain of the EDA is included the total attenuation is only –13.4 dBm. The required receiver input level is about –20 dBm to maintain the required BER. Th difference between the total attenuation and the required receiver input is the margin and is about 6 dBm.

Table 3. Optical Attenuation Power Budget Using SMF

Elements	No. Units	Loss/Unit (dB)	Loss (dBm)
IF Rack to Vertex Room Bulkhead			
Launch Power			0.00
16ch WDM MUX	1	-6.00	-6.00
Connector	3	-0.30	-0.90
Fiber (km)	0.004	-0.30	0.00
Vertex Room Bulkhead to Antenna Pad		$P_{vtx\ bulkhead}$ = -6.90	
Connector	1	-0.30	-0.30
Fiber (km)	0.02	-0.30	-0.01
Farthest Antenna Pad to CB Termination Panel		$P_{last\ antenna\ pad}$ = -7.21	
MIL Connector	2	-0.50	-1.00
Connector	1	-0.30	-0.30
Fiber (km)	22	-0.30	-6.60
Splice	2	-0.10	-0.20
Bends	18	-0.10	-1.80
CB Termination Panel to Patch Panel		$P_{termination\ panel}$ = -17.11	
Connector	3	-0.30	-0.90
Fiber (km)	0.02	-0.30	-0.01
EDFA Gain	1		12.00
Correlator Patch Panel to Correlator Receiver		$P_{IF\ patch\ panel}$ = -6.01	
Fiber (km)	0.004	-0.30	0.00
Connector	3	-0.30	-0.90
16ch WDM DMUX	1	-6.50	-6.50
Received Power			-13.41
Receiver Sensitivity			-20.00
Margin			6.59

3.2 Optical Q Budget

The EVLA system will use COTS receivers that can provide data with an error rate of less than 10^{-9} with a minimum received power of –20 dBm if the signal quality is greater than a Q of 15.5 dB. In order to calculate the required launch Q of the system, all known factors that effect signal quality are added to the receiver requirements. The noise sources are presented as power penalties in dB and represent the impact the noise sources will have on the system digital signal-to-noise ratio (Q). Table 4 lists the calculated power penalties that effect Q. In this table each power penalty is added to the specified receiver Q to obtain a predicted minimum transmitter Q in dB.

Table 4. Required Transmitter Q in dB

EVLA SYSTEM PARAMETER	SMF (dB)
Required Received Q	15.56
Extinction Ratio	1.86
Multiplexer Crosstalk	2.00
Chromatic Dispersion	2.00
Polarization Mode Dispersion	0.04
Non-linearity	0.00
Polarization Dependent Loss	2.12
Optical Amplifier Noise	2.50
Component Aging	1.00
Margin	3.00
Required Transmitter Q (dB)	30.08

To maintain the EVLA start-of-life Bit Error Rate of 10^{-9}, using a receiver with a required digital SNR (Q) equal to 15.5dB or 6 linear, the minimum transmitter Q must be greater than 30 dB for SMF fiber. To compare the measured values to the predicted values given in Table 4, a few of the parameters need to be adjusted. First, the aging and the margin parameters are adjusted to zero and Table 4 will then be rearranged as Table 5. The values are also translated from dB to linear for comparison to the test equipment output. Since there was only a single laser used in the test the Multiplexer Crosstalk parameter is also set to zero. The analysis predicts that the measured Q through 22 km of SMF should be about 13 (linear). The next section compares the measured results to these predictions.

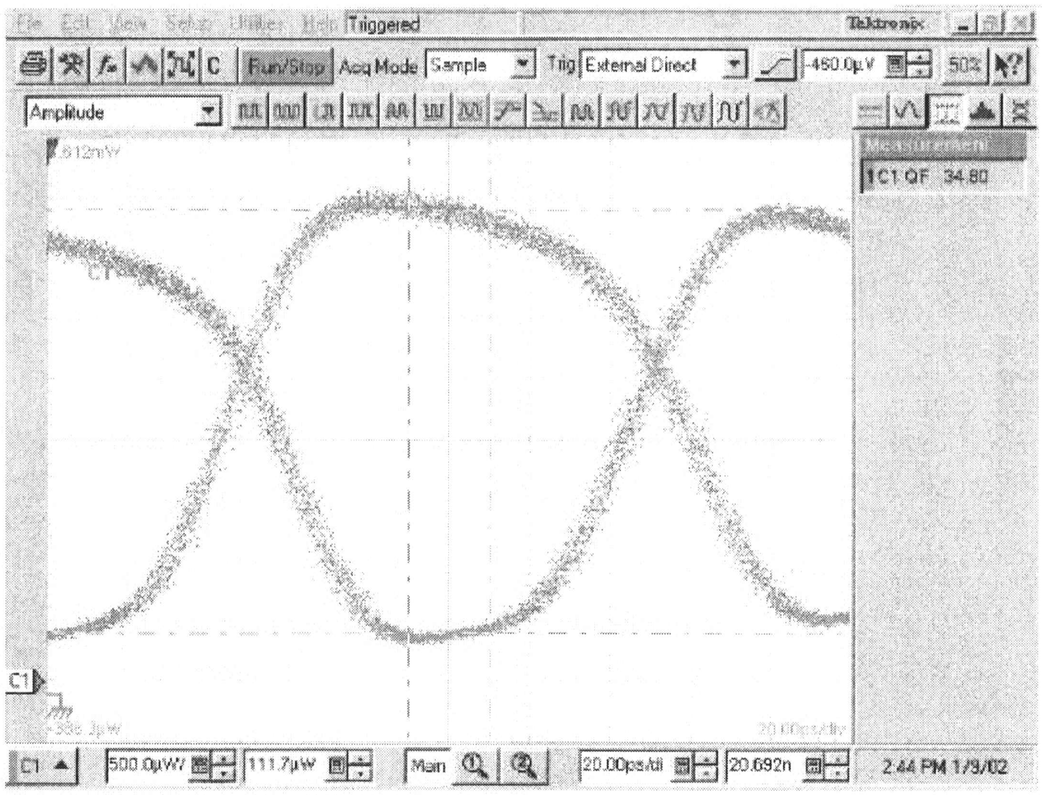
Table 5. Predicted Quality Factor—Using Worst Case Parameters

EVLA SYSTEM PARAMETER	SMF (dB)	SMF (Linear)
Measured Transmitter Q (dB)	30.83	34.8
Extinction Ratio	-1.86	0.807
Multiplexer Crosstalk	0.00	1
Chromatic Dispersion	-2.00	0.794
Polarization Mode Dispersion	-0.04	0.995
Non-linearity	0.00	1
Polarization Dependent Loss	-2.12	0.783
Optical Amplifier Noise	-2.50	0.750
Component Aging	0.00	1
Margin	0.00	1
Predicted Measured Q (dB)	22.31	13.03

4. MEASURED RESULTS

A bench prototype of a single 10 Gbits/s link was tested in January 2002 at the AOC in Socorro NM. The system consisted of a prototype formatter, a CW laser, a passive 12:1 WDM fiber multiplexer and a passive 12:1 WDM fibe de-multiplexer, an EDFA, and SMF.

The output of the laser through 1 meter of fiber was measured to determine the launch Q factor using an Optical Communication Signal analyzer, Tektronix CSA 8000. Figure 5 shows a typical screen output. The signal strength about 5.5 dBm out of the laser. Note that the Quality Factor of the eye pattern is 34.8 linear. This is similar to the predicted launch Q (table 4) required to obtain a Q of 13(linear) at the receiver.



Laser only

Figure 5. Optical EYE Pattern with 1 Meter of Fiber

The complete IF link was then measured. This included: a passive 12:1 WDM fiber multiplexer and a passive 12:1 WDM fiber de-multiplexer, an EDFA, 22 km of SMF fiber, and fourteen FC/APC connectors. The resulting Q was about 13.27 linear, Figure 6. From table 6 the predicted Q was 13.3. In addition, the shape of the eye is starting to show the affects of dispersion [5]. This was predicted by the chromatic dispersion calculation.

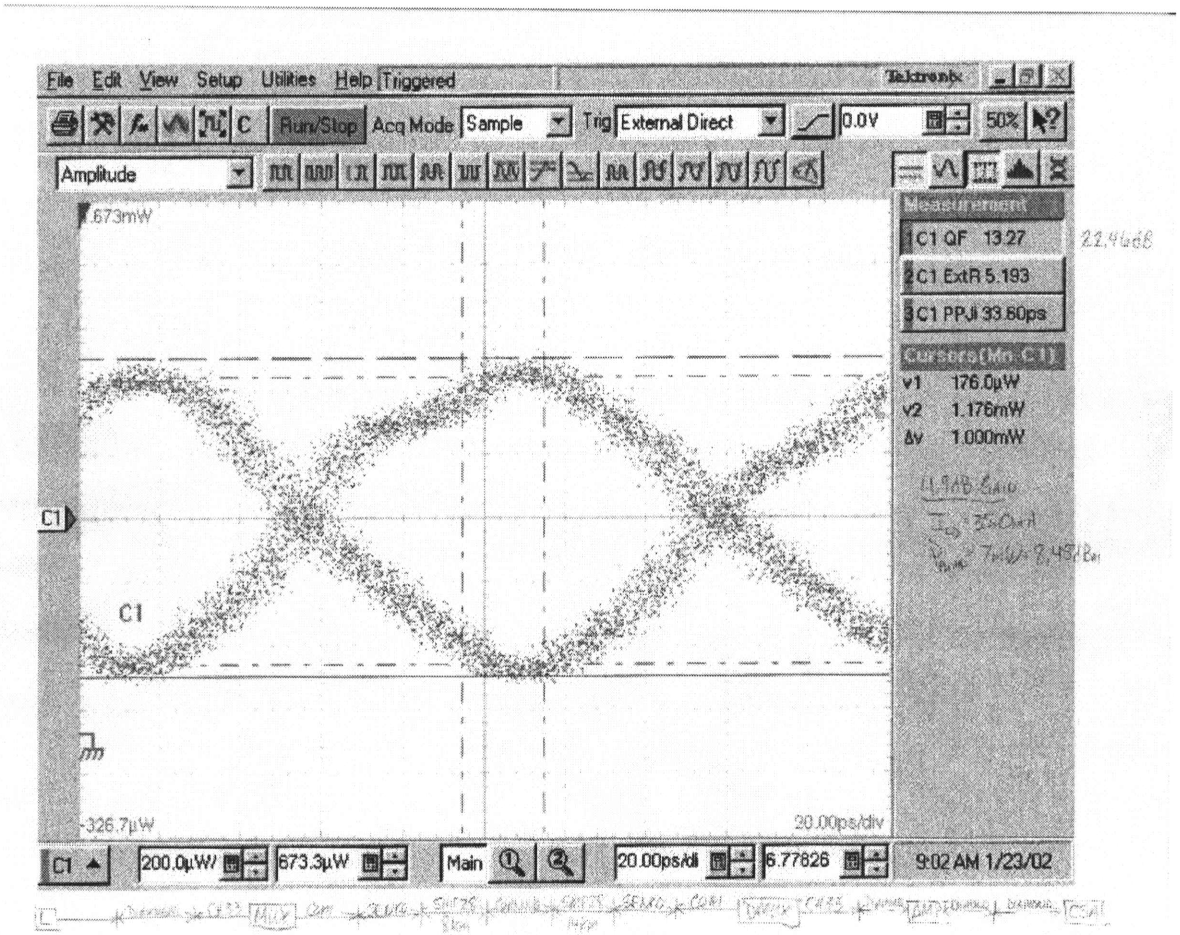


Figure 6. Complete IF link Performance

5. LESSONS LEARNED

Five lessons will be presented.

5.1 The use of COTS components developed for the telecommunications and computer industries allowed NRAO to design a high performance digital IF Data Transmission System for use in large Radio Interferometers without incurring large up-front engineering costs.

5.2 The use of standard SONET protocols was not practical in this system due to the requirement of realigning the multiple 10.24 Gbits/s data streams from each antenna at the receiving end. In the end we decided to use the SONET OC-192 hardware but not the protocols.

5.3 The new Xilinx Virtex families of Field Programmable Gate Arrays greatly simplified the design process by allowing NRAO to:

A. Update and test designs without major redesign or modifications of printed circuit boards and circuit components.
B. Use high performance logic interfaces, such as LVDS and PECL, without the use of the numerous line drivers, receivers and complex printed circuit boards usually associated with these technologies.

5.4 The AMCC and Xilinx devices also introduced NRAO to the positive and negative aspects of the Ball Grid Array (BGA) packaging concept.

A. On the plus side, due to greater pin count and better routing flexibility, BGAs allow for substantially higher density and higher performance Printed Circuit Board designs.
B. On the minus side, BGAs are difficult to install and remove in a laboratory environment. Also troubleshooting is challenging because many of the pins are impossible to probe. Based on our experiences with these devices, a Pace soldering and X-ray system designed specifically for BGA IC's has been purchased and installed in our laboratory. We believe that a Pace or similar system is required for prototyping and is also required for rework and repair throughout the operational life of the EVLA.
C. At-the-end-of-the-day, we find that the advantages of the BGA packaging concept outweigh the disadvantages. A properly equipped laboratory can work with these devices efficiently and successfully.

5.5 NRAO has also discovered that the signal quality and phase relationship of the master clock signals, especially to the 10.24 Gbits/s Mux/Demux ICs, is very critical. We tested the prototype hardware using different clock and reference sources with varying phase noise characteristics. Close in phase noise and spurious signals present on the master clocks affect the performance of the phase locked VCOs in the Mux/Demux ICs, which in turn affects on the jitter and BER of the 10.24 Gbits/s signal. In addition, varying the phase relationship of the VCO and reference clocks to the Multiplexer IC's had a visible impact on the jitter of the eye patterns. Examining the same signals on a spectrum analyzer revealed varying levels of spurious signals and close in phase noise.

6. Summary

The Very Large Array (VLA) is the most productive astronomical instrument on Earth despite its 22 year age, yet the fiber optic based IF transmission system described in this paper promises to make the Expanded VLA 10 times as sensitive. To achieve this substantially improved performance, the received signals are digitized at the antenna and transmitted through fiber using a high performance dig ital transmission system. To minimize risk and expense, the transmission system uses COTS technology available from the telecommunications industry to perform the demanding task of transporting 3.24 Terabits/second of astronomical data to a central location. The sophisticated design also represents an important shift in the astronomical community to Field-Programmable -Gate-Arrays, Ball-Grid-Arrays, Erbium Doped Fiber Amplifiers, and various test and fabrication equipment to support the new high data rate technologies.

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