GBT MEMO 99

NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank WV

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DESIGN GOALS FOR A DIGITAL CONTINUUM RECEIVER

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Introduction

After thinking about a new DCR for some time, I would like to propose the following system. We would build the system on the VME platform. Two custom boards would be built in house. One board would be a timing generator and the other an integrating counter board. A block diagram of this system can be found at the top of figure 1.

Basic Specifications

V/F CONVERTER

Voltage to frequency converters would be located in the receiver room and at the prime focus. The pulse train from the V/F converters would run over fiber to the alidade room.

The present DCR uses V/F converters with a maximum pulse frequency of 5 MHZ with a 10 volt input. Another V/F converter is available with 10 MHZ output with 10 volt input. The 5 MHZ V/F converters linearity is around 5 times better than the 10 MHZ V/F converter.

NUMBER OF CHANNELS

At present the number of channels would be 16. The integrating counter board would be designed so that this number can be increased.

NUMBER OF PHASES

To understand what is meant by a phase, please look at the bottom of figure 1. All of the lines out of the timing generator can have its state selected for one phase period. The number of phases will probably be unlimited. If we have to set a limit, it would be in some binary increment (512, 1024 etc.). We will use the 10 MHZ standard for the time base. The number of lines that can be programmed will be set at eight.

ADVANCED PHASES

As in our present DCR we will have an advanced version of the signal/reference line. This line could be used to move the sub-reflector before we are done taking data for that phase. (Because of the inertia of the sub-reflector good data is available after the sub-reflector is told to move)

MINIMUM & MAXIMUM PHASE PERIOD

The minimum phase period will be determined by the time it takes to transfer data to the computer and do something with it. I would guess a few hundred micro seconds. The maximum is

dependent on the V/F converter frequency. For a V/F converter frequency of 5 MHZ it would be 859 seconds.

START OF SCAN

The timing generator will be designed so that it can go to phase 0 some selected period of time after the 1 second tick. The resolution of this period will be 100 nano seconds.

BAD DATA FLAG

When the computer reads the data from the integrating counters it will also read a bad data flag. If this flag is set then the computer will treat the data accordingly. Some things that could possibly set the bad data flag would be, antenna of source, LO out of lock and RFI detected.

SLAVE OPERATION

The integrating counters will always be controlled by external signals, even if they are being generated by the local timing generator.

DATA HANDLING

Data can be integrated in the DCR computer. It will be time tagged and passed on to the data analysis computer.

DIAGNOSTIC CAPABILITIES

I would like to have the capability to have the computer in the receiver room, switch a reference voltage into the V/F converters. In addition we will have the ability to switch in a reference frequency at the integrating counter inputs.

Some of the specifications will not be able to be set until we get into the actual design of the DCR. It would be good to have some continuum observers involved when design decisions have to be made. Anyone interested in being involved in these design decisions should contact me.

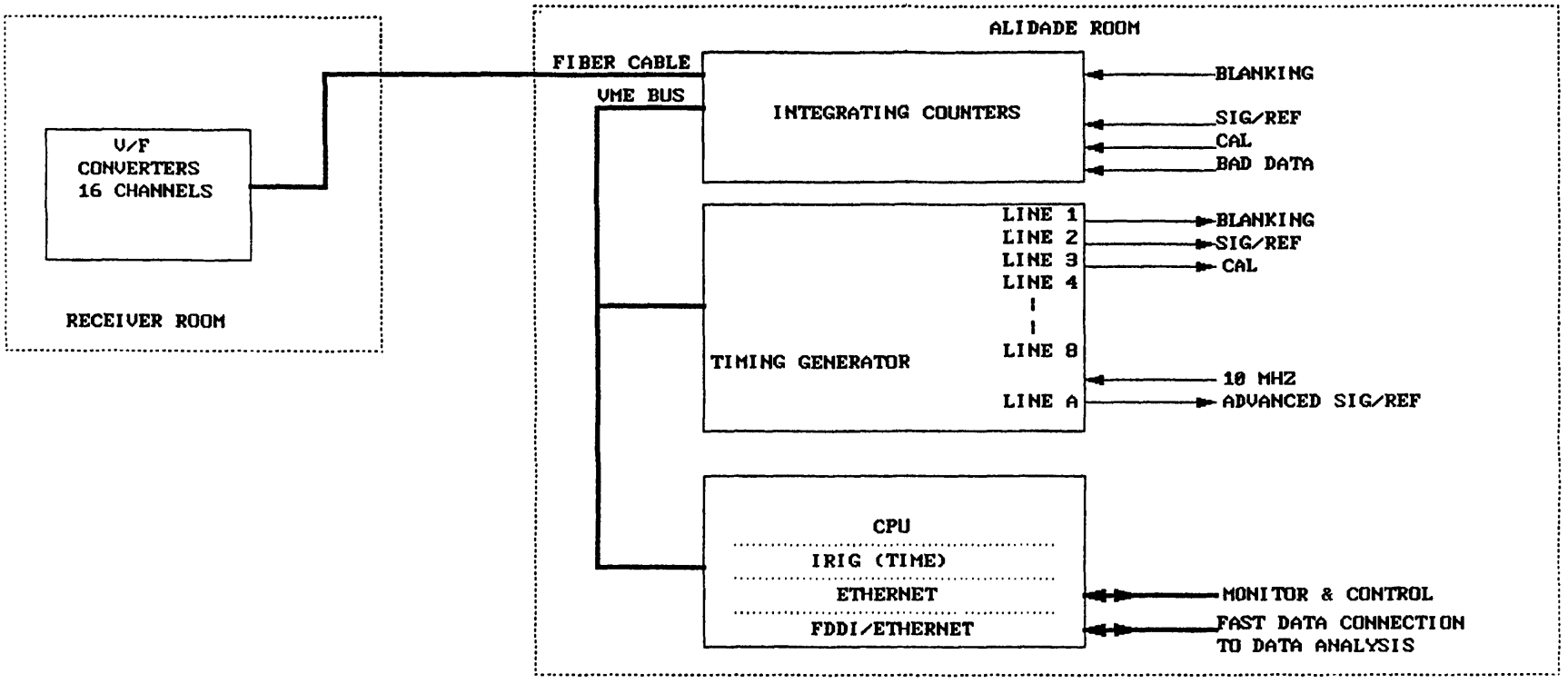

DIAGRAM OF PHASE PERIODS

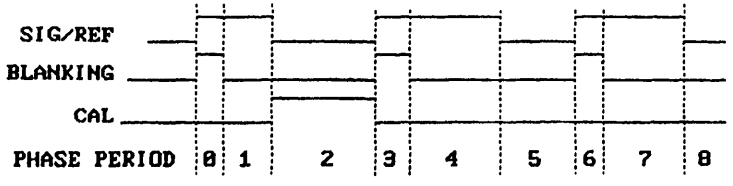

FIGURE 1

NRAO GREEN BANK			
TITLE PROPOSED DCR FOR GBT USING VME PLATFORM			
SIZE B		NUMBER BXXXXXXXXX	REV A
DATE JAN 27,1993		SHEET 1 OF 1	