GBT MEMO 101

THE HOLOGRAPHY SYSTEM: IF AND CORRELATOR DESIGN

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I. System Design

The design parameters for the holography backend are determined by the resolution and accuracy of the holography map. As noted in GBT Memo No. 68, a 200 x 250 pixel map with an accuracy of at least 100 um rms is needed to measure the surface; therefore, the system is designed for an accuracy of 10 um rms. Using the holographic antenna measurement analysis of the 12 Meter Millimeter Wave Telescope Memo 202[2], an estimate of the signal-to-noise ratios along with the minimum integration time for each point can be calculated. The correlation bandwidth is determined by the type of source used, whether it be a satellite beacon or an continuum astronomical source, such as a water maser. The initial conception of the holography measurement system was to use a satellite beacon for a high resolution high accuracy map and a astronomical source for a lower resolution lower accuracy map at different elevations to determine gravitational deformations. Therefore, the correlator is designed to operate at either a 100 KHz bandwidth or a 10 KHz bandwidth. A list of all drawings associated with this project are given in Table 1.

The analysis for SNR ratio and the associated integration time along with the dynamic range of the backend is taken from memo 202. The integration time requirements along with the associated SNR is calculated using a Mathematica simulation for an ideal circular aperture with a typical satellite EIRP of 40 dBw taken from the 1992 International Satellite Directory and a reference receiver temperature of 100° K. The results are shown in Table 2 for a 0.13m horn reference and a 100 meter test antenna. Since the detection of phase variations of $2\pi\,\Delta z / \lambda$ is necessary for a surface accuracy of $\Delta z / 2$, the dynamic range must be greater than 52 dB for $\Delta z = 10\ \mu m$ and $\lambda = 2.5$ cm. In order to achieve an accurate measurement of each panel, a very large map is needed; therefore, the map must consist of measurements from sidelobes which are as much as 125 beamwidths away with no oversampling. This predicates a backend with a estimated dynamic range of 70 dB. The estimate is taken from GBT Memo No. 47 which predicts the antenna pattern for 10 beamwidths away.[3] As noted in memo 202, the dynamic range requirements can be relaxed if the central point is not measured or an attenuator is included in the backend.

The correlator backend is intended to operate in conjunction with two separate receivers, one for the test antenna (GBT) and one for the reference antenna. The receivers should consist of a tunable IF section with an output frequency band of 50.001 MHz to 50.100 MHz.

II. IF

The IF portion of the backend accepts inputs from 50.0001 MHz to 50.1000 MHz and downconverts the band to a baseband range 100 Hz to 100 KHz or 100 Hz to 10 KHz. A block diagram is shown in Figure 1. The IF consist of two channels, one for the reference and one for the test signal. Each channel consists of a 51/2 MHz bandpass filter, a programmable attenuator, a SSB downconverter with greater than 27 dB rejection, a 100 KHz and a 10 KHz antialiasing filter and a 16 bit ADC where the lower two bits are discarded. The system gain from the input of the 51 MHz bandpass filter to the input of the AD converter is 33 dB with an equivalent input noise of -98 dBm/Hz and one dB compression point of -14 dBm. The dynamic range is 72 dB for the 10 KHz bandwidth and and 62 dB for the 100 KHz bandwidth. Each channel has a front panel meter displaying the input level in dBm, a front panel monitor of the input, and a front panel monitor of the output. The test channel has a 90 degree phase shifter accurate within +/- 1 degree over 10 KHz bandwidth and +/- 2 degrees over a 100 KHz bandwidth. The IF drawer also contains a 50 MHz PLL which generates the LO signals from a 5 MHz input.

A. SSB Downconverter

The single sideband mixer rejects the band from 49.9999 MHz to 49.9000 MHz by splitting the signal and introducing a 180 degree phase difference in the unwanted sideband and then recombining the signal at baseband to cancel the undesired sideband. Since the Hilbert transform circuit at baseband requires the tightest tolerances, an op-amp circuit was used in the implementation to eliminate inductors. In order to achieve greater than 30 dB of rejection, the accuracy of the transform must be +/- 1 degree over a 100 Hz to 100 KHz bandwidth. The parameters for the circuit, which has a ratio of upper to lower frequency greater than 1146 with a phase error of 0.66°, was not available in the paper by S.D. Bedrosian[4]; therefore, a Mathematica program was generated which calculated the values need by evaluating ratios of elliptical functions to solve for the pole-zero locations. The gain of the SSB downconverter is measured to be 24 dB with an equivalent input noise of -95 dBm/ Hz and a 1 dB compression point of -4 dBm. The schematic is given in drawing D35205S0 and the Mathematica program is given in drawing A35205D003. The rejection at various frequencies is given in Table 3.

B. Anti-aliasing Filter

The anti-aliasing filter consists of a 100 Hz five section highpass elliptical filter, cascaded with a 100 KHz seven section lowpass elliptical filter and a 10 KHz seven section lowpass elliptical filter. Both the 10 KHz bandwidth and the 100 KHz bandwidth outputs are available. The circuit is implemented using OP27 operational amplifiers with an RC topology that contains a voltage control voltage source network. The paramerters chosen for the 100 Hz highpass filter are: modular angle equal to 26°, reflection coefficient of 0.05, and a minimum attenuation of 40.81 dB at 43.84 Hz. The parameters chosen for the 10 KHz and 100 KHz highpass filter are: modular angle equal to 26°, reflection coefficient of 0.20, and a minimum attenuation of 48.81 dB at 20.5 KHz and 205 KHz , respectively. The schematic is given in drawing D35205S012. The gain of the 100 KHz and the 10 KHz filter is measured to be 42 dB. The highpass section of the filter has a 3 dB point at 100 Hz and 34 dB of attenuation at 60 Hz. The 10 KHz filter 3 dB point is measured to be 8.80 KHz, with a one dB compression point of -32 dBv and 30 dB of attenuation at 10 KHz. The input noise density is measured to be -3.16 $\mu V/\sqrt{Hz}$. The 100 KHz filter 3 dB point is measured to be 87.75 KHz with a one dB compression point of +31 dBv and 30 dB of attenuation at 100 KHz. The input noise density is measured to be -3.16 $\mu V/\sqrt{Hz}$.

C. Hilbert Transform

As described in the SSB downconverter section, a Mathematica program generated the parameters for the 100 KHz bandwidth and a 10 KHz bandwidth Hilbert transform circuit. The schematics for the circuit is given in drawings D35205S013 and D35205S014, respectively. The design tolerances were necessitated by the accuracy in the holographic map. The errors caused by the Hilbert transform circuit can be reduced in the analysis software, but in order to achieve the performance needed tight design criteria were necessary. The goal was to achieve +/- 0.66° degree deviation peak-to-peak from 90 degrees over a 10 KHz bandwidth and +/-1.0 degree deviation peak-to-peak from 90 degrees over a 100 KHz bandwidth. The 10 KHz bandwidth circuit phase deviation is measured to be less than +/-1.0 degree and the 100 KHz bandwidth circuit phase deviation is measured to be +/-1.8 degrees. The gain of each circuit is 0 dB with a 1 dB compression point of +10 dBv, and the equivalent input noise floor is -7.93 $\mu V/\sqrt{Hz}$.

D. Analog to Digital Converters

The most critical part of the entire backend is the AD converters, since they can restrict the dynamic range and noise performance of the correlator. For a 72 dB dynamic range, greater than 12 bits were needed. An economical ADC with a bandwidth greater than 100 KHz is the 16 bit Burr Brown PCM 78P combined with the Burr Brown SHC 5320 sample and hold. The maximum input range is +/- 3V with a resolution of 91.55 uV. The ADC's were tested by taking numerous readings to obtain adequate statistics of the noise. The variance of the readings indicated an rms noise value of 550 uV or just over 2 bits. The ADC's were located in the IF drawer in order to isolate them from the digital electronics. The ADC's also have separate power supplies to further isolate them. Since only 12 bits were needed and the lower bits are masked noise, the lower 2 bits are discarded. The circuits were tested and found to be linear within 1%. The ADC's require an external sample pulse and a external clock which are synchronized with the digital electronics. The output is a serial two's complement 16 bit number and a seventeen pulse clock. The input and output signals are buffered by a 8820 and 8830 line drivers, respectively. The schematic is shown in drawing B35205S009.

E. 50 MHz PLL

The phase lock loop consists of a 50 MHz Vectron crystal oscillator which is locked to a 5 MHz input via a digital PLL. A monitor circuit detects lock and is indicated by a green LED located on the front panel. Two outputs are available, one for each SSB downconverter. The output power is + 9 dBm with the harmonics being less than - 40 dBc. The schematic is shown in drawing B35205S011.

F. Logarithmic Amplifier

The input signal is split and detected by a BD-4 diode. The detected signal is input to a logarithmic amplifier and the level scaled to produce a 100 mV/ dBm output signal. The output signal is then input to a digital voltmeter on the front panel. The range of the detection circuit is -20 dBm to +5 dBm. The schematic is shown in drawing B35205S016.

III. Digital Correlator

The digital correlator calculates six products which are 48 bits after integration from the three 14 bit inputs. The integration time is set externally by a 16 bit input. The block diagram is shown in Figure 2. The correlator consists of 9 cards: ADC interface card, a timing card which generates all the clocks and timing signals, a multiplier card, an accumulator and 8x1 multiplex output buffer card, a display driver card, an IF input attenuation control card, and a MCB bus interface card. Fast CMOS technology with TTL logic was used to implement all digital circuits. The block diagram for the correlator is given in drawing D35205K001. Two different timing cards allow selection of either a 195,312 KHz or a 24,414 KHz sampling rate. The maximum integration time for the 195,312 KHz sampling rate is 524,288 x 5.12 us = 2.68435456 s and 524,288 x 40.96 us = 21.47483648 s for the 24,414 KHz sampling rate. The six products are the reference channel squared R^2, the test channel squared T^2, the phase shifted test channel squared Q^2, along with the cross products RT, RQ, and TQ. The timing diagrams for the 5.12 us and the 40.96 us sampling intervals are given in drawings B35205L001 and B35205L002, respectively.

A. ADC Interface

The ADC interface card accepts serial data and a clock from the AD converters and converts the data stream to a parallel output. This is accomplished using a serial to parallel shift register. The input to the card is a 17 pulse clock with a corresponding 16 bit serial input; therefore, gates for delay are needed to align the clock edges with the data edges. At the beginning of each integration, the serial to parallel shift registers are zeroed by an inhibit signal from the timing card. Therefore, the first sample from the AD converters are ignored so that any charge buildup on the sample and hold circuits occurring between integrations will not influence the products. The schematic for the card is given in drawing B35205S001.

B. Timing Card

The timing card consists of a 25 MHz crystal oscillator, which serves as the master clock, along with five 4 bit counters which set the integration time. The card also provides the AD converters with an external clock. The AD converters require the rising edge of the clock to fall within 50 ns of the falling edge of the sample pulse, so some delay was needed to ensure this condition. The 2 bytes for the integration time are input one byte at a time and are stored in registers. The 2 byte number is calculated by dividing the desired integration time by the resolution rounding off to the nearest integer and taking the two's complement. Since only four of the five counters can be preset, the resolution for the 24 KHz and the 195 KHz sampling rate is 16 X 40.96 us = 655.36 us and 16 x 5.12 us = 81.92 us, respectively. An external pulse starts the integration. The 2 byte integration time does not have to be input again unless a change of integration time is desired. The integration stops when the MSB of the counters changes from a high state to a low state.

The logic of the timing card generates all enables and all addresses for the multiplexers, the multipliers, and the storage registers, so that all the multiplying and accumulation is synchronous. Between each sample, the timing card enables the input multiplexers such that all the combinations of input are applied to the multiplier chips for the six different products. The pipeline registers are addressed in conjunction with the enables so the products will be added to the total and stored in the proper address.

The timing card has a remote enable and a remote 3 bit address input. Once the remote enable is activated, the data stored in the pipeline register at the input address will be output to the muliplexers. Products T^2, Q^2, R^2, TQ, TR, QR are stored at locations 0,1,2,3,4,5, respectively. The schematic for the 100 KHz card is given in drawing B35205L002, and the schematic for the 10 KHz card is given in drawing B35205L003.

C. Multiplier Card

The multiplier card consists of 12 four bit data selectors, and two 32 bit two's complement multipliers. The data selectors are arranged so that each of the three 14 bit inputs are either output to the 16 bit X bus, the 16 bit Y bu,s or the output is left in a high impedance state. The two superfluous input least significant bits of each mulitplicand are held low, and the four least significant bits of the product are unused. The X bus is connected to the X multiplicand and the Y bus is input to the Y multiplicand of the multiplier. The multipliers operate in parallel where one multiplier outputs the 16 most significant bits and the other multiplier outputs the 16 least significant bit to the adders. The schematic for the card is given in drawing B35205S004.

D. Accumulator Card

The accumulator card consists of three 16 bit pipeline storage registers, 12 four bit adders, and eight 8 x1 multiplexers. At the start of integration, the output of the pipeline registers are held in a tristate for one sample period. This inputs a minus one to the adders where a carry is input for one cycle. The output of the adders is necessarily zero, which is stored in the pipeline registers for all six products. After the multiplier card has output one of the six products, the product is added to the previous accumulated sum. Because the sum is 48 bits, the MSB of the product is extended to maintain two's complement arithmetic. The new sum is then stored in the pipeline registers. The stored data in the pipeline registers at a given address is output at the next rising edge of the system clock when the three bit address is applied to the select inputs and the external read mode is activated. In order to output all six bytes to the 8 bit output bus, a three bit address must be applied to the multiplexers. The addresses 0, 1, 2, 3, 4, 5 correspond to the bits 0-7, 8-15, 16-23, 24-31, 32-39, 40-47, respectively, where 47 is the MSB. The schematic for the card is given in drawing B35205S005.

E. Display Driver

The display driver card functions as the input/output interface for the AD converters and the front panel displays. A ribbon cable connects the card to the front panel by a connector which plugs into one of the IC slots on the Shallow card. Another ribbon cable connects the two read addresses and the output byte to a different front panel display. The sample pulse, the external clock, the data clock, and the serial data for each sampler is routed through the display card by twisted pairs of wires which are soldered to a connector and inserted into the card. The other end of the twisted pairs are inserted into an Elco connector mounted on the rear of the chassis. The schematic for the card is given in drawing B35205S006.

F. Attenuator Control

The attenuator control card contains two registers, one for the five bit reference channel attenuator and the other for the five bit test channel attenuator. The registers require seven bits of external input, five bits to set the attenuator and one bit to enable each of the two registers. Because the attenuator require +24 volts, the outputs of the registers are buffered by a high voltage open collector hex inverter and are routed through the Elco connector. The schematic for the card is given in drawing B35205S007.

G. Standard Interface Card

The correlator was equipped with a standard interface so it may be operated from a serial bus. The standard interface card provides the necessary handshake between the standard interface and the correlator. Since the correlator outputs the data to the C/M bus faster than the standard interface can read the data, no delay is needed and the device acknowledge is connected directly to the device request. The interface is active only when the device request output from the standard interface is high. The card is designed so that the lower eight C/M bits are always used for reading data and the upper eight for writing data. When the correlator is integrating, the lower eight bits will be FF hex. The schematic for the card is given in drawing B35205S008.

IV. Software

Routines in C++ were written which: calculate the integration and set the correlator, set the attenuators, begin integration, and read the data from the correlator. These exist for operating the correlator via a 386 PC or through the MCB serial data bus. The routines written for the standard interface use borrowed code in the object oriented style of programming from routines for the standard interface.

V. Test Results

The IF drawer and the correlator were used for a holography map on the 45' OVLBI antenna. The 12 GHz front end from previous holographic experiments on the 140' antenna was used as a reference. The map size was 64 x 64. No specific tests on the backend were conducted; however, the holography system produced a map which contained recognizable surface features of the 45' antenna. A memo in the OVLBI series is forthcoming.

VI. Acknowledgements

I would like to acknowledge all technicians at GB, since each contributed something to the construction of the backend, especially Jerry Turner for the correlator chasis, and Brian Crouse for the IF chassis and system tests.

I would also like to acknowledge Larry D'Addario for performing tests on the 45-ft antenna with the holography system, Ron Maddalena for analyzing the results with his newly developed software, and Roger Norrod for providing helpful information on the integration of the holography system with the GBT.

References

1. R.J. Maddalena, R. Norrod, S.D. White, 1991, "Planned Holographic Measurements with the Green Bank Telescope," GBT Memo No. 68.

2. L.R. D'Addario, 1982, "Holographic Antenna Measurements: Further Technical Considerations" NRAO 12-Meter Telescope No. 202, 11/92.

3. S. Srikanth, 1990, "Electromagnetic Analysis of the GBT," GBT Memo No. 47.

4. S.D. Bedrosiani; "Normalized Design of 90° Phase-Difference Networks," IRE Transactions on Circuit Theory, Vol. LT-7, June 1960.

Drawing Title	Drawing No.	Date	Program Format	No. Pages
Holography Correlator Block Diagram	D35205K001	02/02/93	ACAD12	1
Holography Block Diagram	D35205K002	03/17/92	ACAD12	1
Digital/IF Interconnect	A35205W001	02/04/93	ACAD12	1
Serial to Parallel	A35205W002	11/05/91	QPRO	1
Int Time/Enables	A35205W003	11/05/91	QPRO	1
Select Multiply	A35205W004	11/05/91	QPRO	1
Multiply/Accumulate	A35205W005	11/05/91	QPRO	1
Display Driver	A35205W006	11/05/91	QPRO	1
Attenuator Driver	A35205W007	05/19/92	QPRO	1
VLBA Interface	A35205W008	06/30/92	QPRO	1
Power Supply/Downconvertor Interconnect	A35205W009	02/05/93	ACAD12	1
100KHz A/D Convertor Timing Diagram	B35205L001	02/02/93	ACAD12	1
10KHz A/D Convertor Timing Diagram	B35205L002	02/02/93	ACAD12	1
A/D Timing Diagram	B35205L003	02/02/93	ACAD12	1
Timing Diagram	B35205L004	02/02/93	ACAD12	1
Coarse Timing	B35205L005	02/03/93	ACAD12	1
A: Serial to Parallel Shalloway Card Assembly	D35205A001	02/01/93	ACAD12	1
B: 100K Samples Shalloway Card Assembly	D35205A002	02/01/93	ACAD12	1
B: 10K Samples Shalloway Card Assembly	D35205A003	02/01/93	ACAD12	1
C: Select Multiply Shalloway Card Assembly	D35205A004	02/01/93	ACAD12	1
D: Multiply/Accumulate Shalloway Card Assembly	D35205A005	02/01/93	ACAD12	1
E: Display Driver Shalloway Card Assembly	D35205A006	02/02/93	ACAD12	1
F: Attenuator Control Shalloway Card Assembly	D35205A007	02/02/93	ACAD12	1
G: VLBA Interface Shalloway Card Assembly	D35205A008	02/02/93	ACAD12	1
A: Serial to Parallel	B35205S001	06/10/92	FUTURENET	1
B: 100K Samples	B35205S002	11/01/91	FUTURENET	3
B: 10K Samples	B35205S003	11/01/91	FUTURENET	2
C: Select Multiply	B35205S004	10/17/91	FUTURENET	1
D: Multiply/Accumulate	B35205S005	10/17/91	FUTURENET	2
E: Display Driver	B35205S006	01/09/92	FUTURENET	1
F: Attenuator Control	B35205S007	05/19/92	FUTURENET	1
G: VLBA Interface	B35205S008	07/17/92	FUTURENET	2
Test A/D Convertor	B35205S009	01/10/92	FUTURENET	1
Front Panel Display	B35205S010	11/18/91	FUTURENET	1
50MHz Phase Locked Loop	D35205S011	02/03/93	ACAD12	1
Elliptical Filter	D35205S012	03/18/92	ACAD12	1
100 KHz Hilbert Transform	D35205S013	03/18/92	ACAD12	1
10 KHz Hilbert Transform	D35205S014	03/18/92	ACAD12	1
Single Sideband Convertor	D35205S015	03/18/92	ACAD12	1
Log Amp	B35205S016	02/03/93	ACAD12	1
QTest A/D Convertor	B35205S017	01/10/92	FUTURENET	1
Reference A/D Convertor	B35205S018	01/10/92	FUTURENET	1
Drawing Index - Holography	A35205D001	02/05/93	QPRO	1
Integration Time & Noise Simulation	A35205D002	02/09/93	MATHMATICA	1
Hilbert Transform Calculations	A35205D003	02/09/93	MATHMATICA	1
Address Display	A35205Q001	02/09/93	ACAD12	1
50 MHz Phase Locked Loop PC Board	A35205Q002	02/09/93	ACAD12	1
Display Driver PC Board	A35205Q003	02/09/93	ACAD12	1
100 KHz Hilbert Transform PC Board	A35205Q004	02/09/93	ACAD12	1
Log Amp PC Board	A35205Q005	02/09/93	ACAD12	1
Single Sideband Convertor PC Board	B35205Q006	02/09/93	ACAD12	1
100/10 KHz Filter PC Board	A35205Q007	02/09/93	ACAD12	1
50 MHz Phase Locked Loop Box	B35205M001	03/09/92	ACAD12	1
Correlator Front Panel	D35205M002	02/03/93	ACAD12	1
Hilbert Transform Box	B35205M003	02/03/93	ACAD12	1
Single Sideband Box	C35205M004	02/03/93	ACAD12	1
Downconvertor Power Supply Front Panel	D35205M005	01/21/93	ACAD12	1
Downconvertor Power Supply Rear Panel	D35205M006	01/21/93	ACAD12	1
Chassis Panel - Left Side	D35205M007	01/21/93	ACAD12	1
Chassis Panel - Right Side	D32505M008	01/21/93	ACAD12	1
Chassis Panel - Bottom	D35205M009	01/21/93	ACAD12	1
Downconvertor Power Supply...Top Panel	D35205M010	01/21/93	ACAD12	1
Holography Downconvertor...Top Panel	D35205M011	01/21/93	ACAD12	1
Holography Downconvertor - Front Panel	D35205M012		ACAD12	1
Holography Downconvertor - Rear Panel	D35205M013		ACAD12	1
DRAWING NUMBER: A35205D001	TITLE: DRAWING INDEX - HOLOGRAPHY			02/05/93

TABLE 1. LIST OF DRAWING NUMBERS

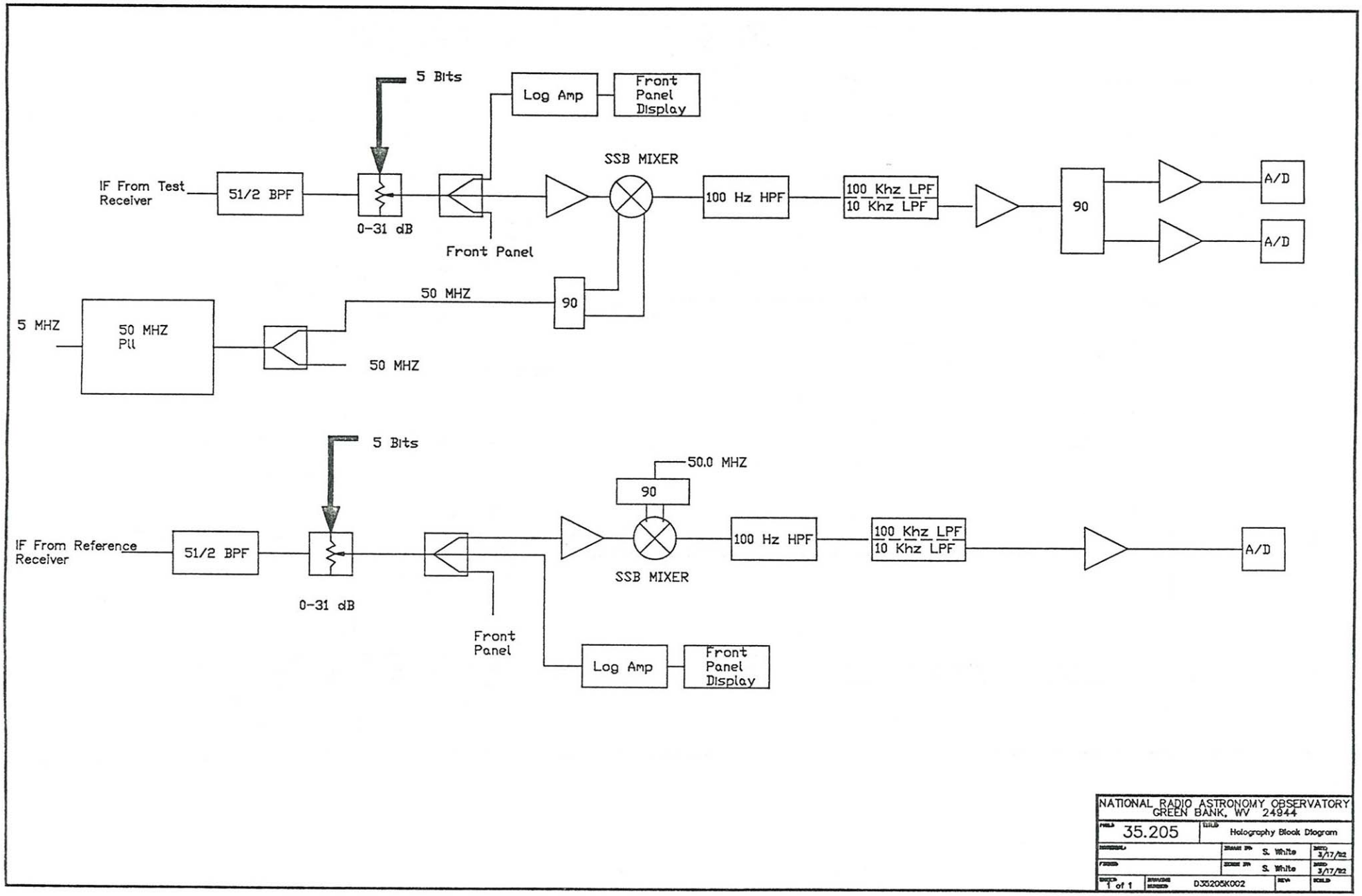
Sampling Interval	Resolution	Number of Samples	Mathmatica Results			$\Delta Z = 10$ [μM]
$\Delta 1$ D/λ	D/Δ	K = (Δ1/λ)	σ_{AVG}/σ_o	M_o/σ_{AVG}	M_o/σ_o	τ [ms]
0.50	200	40,000	0.01406	11050	155	6.4927
	300	90,000	0.00985	16575	163	7.1179
	400	160,000	0.00774	22100	164	7.2386
0.75	200	40,000	0.01048	16575	174	8.1188
	300	90,000	0.00744	24862	185	9.2146
	400	160,000	0.00592	33150	196	10.3390
1.0	200	40,000	0.00867	22100	191	9.8731
	300	90,000	0.00623	33150	206	11.4745
	400	160,000	0.00500	44200	221	13.1447

Table 2. Noise and Integration Time Requirements for GBT with D = 100 m $\lambda = 2.5$ cm where σ_{AVG} is the rms of the measurement errors, M_o is the on axis measurement, and σ_o is the rms on axis error, and Δ 1 is the sampling interval as defined by the direction cosine.

Frequency [Khz]	0.09	1.0	2.0	10.0	20.0	30.0	40.0	50.0	80.0	88.0	98.0
Test Channel Rejection [dB]	20	32	27	40	38	37	35	33	31	28	25
Ref. Channel Rejection [dB]	26	35	28	36	33	36	38	38	34	28	27

Table 3. Single-Side Band Rejection Measurements.

FIGURE 1. IF BLOCK DIAGRAM



NATIONAL RADIO ASTRONOMY OBSERVATORY GREEN BANK, WV 24944			
PROJ 35.205	TITLE Holography Block Diagram		
DRAWN BY	S. White	DATE 3/17/92	
CHKD	CHKD BY S. White	DATE 3/17/92	
SHEET 1 of 1	DRAWING NUMBER D35205K002	REV	SCALE

FIGURE 2. CORRELATOR BLOCK DIAGRAM