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# Doubling the Bandwidth of the 64-Antenna ALMA Correlator

NAASC Memo #115

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Date: May 21, 2015

## ABSTRACT

A method of doubling the bandwidth of the baseline ALMA correlator is presented. The approach taken is to use the present correlator infrastructure as much as possible but replace most of the circuit cards. Economy of hardware cost, software development, and ALMA operation disruption will thus be achieved.

## Overview

The ALMA correlator upgrade being suggested here would be the second of a two-step process to increase the performance of the system. The first step is described in NAASC MEMO #114 which proposes increasing the frequency resolution of the ALMA correlator by a factor of 8. This first step is currently being considered for a 2015 NA ALMA development study proposal award.

If the resolution upgrade is funded and implemented, implementation will be done in such a way as to facilitate this second step. Because the resolution upgrade requires the development of an expensive custom integrated circuit, the resolution increase will have the higher cost of the two modifications. Bandwidth doubling would be a relatively inexpensive process (of course, bandwidth doubling has serious cost implications for the rest of the ALMA data path, whereas the resolution increase has mostly implications for the correlator and software and hardware downstream from the correlator).

If so desired, it would be an easy task to make the twice bandwidth modification compatible with the current bandwidth. That is, with the addition of some temporary very simple interface cards to replace the old TFB cards, the upgraded correlator system would be able to work with the current data transmission system at the current data rate. In this way, the remaining ALMA sub-system could be brought up to double bandwidth operation on an optimum time schedule.

As indicated above, other sub-systems of ALMA, receivers, digitizers, data transmission, etc., need to be upgraded for full twice bandwidth operation.

These two correlator upgrades represent a relatively inexpensive way to get a high performance interim system pending the possible availability of a software correlator in the 2020's.

## Clock

As currently implemented, the ALMA correlator runs with a clock rate of 125 MHz. This rate will have to be changed to 250 MHz. Two ways of doing this would be to either replace all of the clock oscillators in the system with 250 MHz units or to continue distribution at 125 MHz but develop 250 MHz on each card. The implementation presented here proposes using the latter approach, since all modern FPGAs have frequency doublers and, with an upward conversion, there will be no phase ambiguity and synchronous operation will be possible throughout the system.

Modern FPGAs also have the advantage of clock and output phase adjustment to assist in providing error free data transmission throughout a system designed for 125 MHz but now requiring 250 MHz operation.

## Station Electronics

The current DRX card will be replaced with a plug-in replacement card that implements the current DRX fiber optic data recovery but with twice the bandwidth. While the DRX card is housed within the racks of the correlator, it has never been considered as part of the ALMA 64-antenna correlator. Redesign of the DTX/DRX cards that bring data from the outlying antennas to the correlator is not included in the cost estimate below.

The current Tunable Filter Bank Cards and Station Cards will be removed and replaced with newly designed TFB/Station Cards to handle twice the clock rate. Each new TFB/Station card would duplicate the present function of two TFB Cards plus the current Station Card, all at twice the data rate. Using a 250 MHz clock

rate will fit the double bandwidth into the same number of sub-bands (32) thus enabling major parts of the correlator infrastructure to be used without modification.

The interface between the DRX card and the TFB/Station Card would be card-to-card cables using high data rate LVDS or optical with a total data capacity of 32 G-b/s (250-MHz x 32-ch x 2-bits x 2-IFs).

The interface between the new TFB/Station Card and a new double data rate Station Interface card will be made using the current station mother board circuit traces carrying 250MHz data instead of the current 125 MHz rate. Engineering tests have been run that proves this approach is technically possible; error free transmission over the existing circuits has been demonstrated at the increased data rate.

As mentioned above, to make the system “backward compatible”, simple interface cards to replace the old TFB cards could be designed and placed into the current TFB card slots so as to interface the present DRX card to the new TFB/Station Card. This would allow operation at the current ALMA bandwidth while the rest of the ALMA system is brought up to full twice bandwidth capability. A rough cost estimate to implement this option is about \$150,000 (not included in the cost estimate at the end of this document).

### **Station Racks to Correlator Racks Cable Interface**

It is proposed to use the current data cabling for data transmission between the station racks and the correlator racks. These cables will have to operate at 500 MHz instead of the current 250 MHz data rate. The EVLA correlator uses the same cables at a 1 GHz data rate (with frequency compensation in the cables) and this gives us some confidence they will be able to operate error free in the upgraded ALMA correlator. Still, extensive engineering tests will be required to fully qualify this approach.

It is highly desirable to keep the current cables between the SI (Station Interface) cards and CI (Correlator Interface) cards since replacing them would take a week or more per quadrant. It may be possible to build cable compensation into the SI card.

### **Correlator Electronics**

A new double data rate Correlator Interface card will be required to replace the current CI cards.

A new Correlator card, currently being proposed for the 8-times resolution project, will replace 4 current Correlator cards. The Correlator card custom chip, now requiring a 250 MHz clock rate, would probably necessitate a 45-nm or finer process (and will possibly require an extra pre-scaler bit in the correlator circuit).

The interface between the CI card and the upgraded correlator card will use the current correlator mother board traces working at 250 MHz. Again, engineering tests have been run that proves this approach is technically possible; error free data transmission has been demonstrated using the present correlator infrastructure at the increased data rate.

### **Post-Correlator Electronics**

Post-correlator electronics will be much like that being considered for the resolution upgrade project. Since the number of sub-channels will stay at 32, the data rate in the post-correlator electronics will not change.

### **Power Considerations**

The upgraded correlator will probably require less electrical power than the current system. Voltage requirements on the replacement logic cards are another matter, however. Most of the new logic families that would be used will require DC voltages lower than any distributed currently. DC-to-DC converters working with the current system voltages should remedy this situation.

## Software Considerations

One very significant advantage that this proposed bandwidth increase has over a complete system redesign is that much of the current correlator oriented ALMA software, developed over the last many years, can remain mostly intact. Much of the current logic would be re-packaged with little conceptual change in larger, faster, FPGAs. Software that would require little change includes:

- Support for observation modes (all modes currently defined will be supported in the upgrade)
- TFB sub-band programming
- Multi-resolution modes
- Delay models
- Sub-band processing and calibration
- Sub-array support

The twice bandwidth modification will require major changes in the firmware embedded in the correlator microprocessors. However, to first order, the interface between the Correlator Control Computer (CCC) and the Station Electronics C167 microprocessor will not change. A minimal amount of work should be required for modifications and re-validation of the CCC to Station Electronics interface.

The resolution upgrade does, of course, have software implications for the Correlator Data Processor (CDP) computer due to the output rate increase.

## Cost Estimate

A summary of new logic cards will be:

TFB/Station	256
SI	128
CI	512
Correlator*	128
Final Adder*	16

Where \* indicates cards developed for the 8 times resolution upgrade. Preliminary (correlator system only) cost estimates for both upgrade projects would be:

Resolution upgrade	\$5 million hardware	5 FTE labor
Bandwidth upgrade	\$2 million hardware	5 FTE labor