SYNCHRONIZATION OF SLOW AND FAST REFERENCE SIGNALS AFTER LONG TRANSMISSION

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INTRODUCTION

In many applications, it is necessary to transmit a timing reference from one place to another with picosecond precision. This can be done, for example, by sending a 1.0 GHz tone, provided that its phase can resolved on the receiving end to about .001 cycle; this is within the present state of the art for transmissions over hundreds of km via various media. However, if only a single tone is sent then the time information conveyed is ambiguous to one cycle of the tone, or 1 nsec in this example. This means that if the reference tone is used to synthesize any frequency that is not a multiple of the reference, then the phase of the synthesized signal cannot be specified. If unambiguous synthesis is required, then a reference frequency that is a sub-multiple of each synthesized frequency must be sent; typically, this requires a reference less than or equal to the smallest step between synthesized frequencies.

In principle, then, all multiples of 1 Hz could be synthesized from a single 1 Hz reference. But it is difficult to do this to psec precision, and if microwave frequencies must be synthesized then the large frequency multiplication would be difficult to implement in a phase stable way. The solution is to transmit two or more references, including a high frequency (HF) for precise timing and a low frequency (LF) for ambiguity resolution, and possibly some intermediate frequencies. The LF reference need only be transmitted with sufficient precision to resolve one cycle of the next-higher frequency reference.

If the timing at the receiving end must maintain a known relation to that at the transmitting end, then the delay through the medium must be accounted for. If the HF and LF references are many decades apart, then they are likely to be subject to different delays. Nevertheless, in many practical cases it is possible to account accurately only for the delay on the HF reference; the others can be ignored because the precision needed is much less.

An example may clarify the preceding points. At the Green Bank OLVBI Earth Station, synthesizers on the antenna must generate microwave frequencies with sub-Hz resolution, while keeping them unambiguously synchronized to a remote hydrogen maser. We plan to accomplish this by sending a hierarchy of reference signals as follows:

500 MHz, high precision, through length-monitored cable;
5 MHz, through unmonitored cable;
1 Hz, through unmonitored cable;
<1 Hz, by computer commands over a separate link.

The precision reference will be drive harmonic phase locked loops with psec-precision phase detectors. The cable length monitoring will have an accuracy of about 3 psec. The 5 MHz and 1 Hz signals (including the effects of their cables) must have timing accuracies of +-1 nsec and +-100 nsec, respectively, relative to the precision reference, but

this can be achieved with ordinary coax over moderate distances in spite of temperature- and flexure-induced stress. The computer commands need only arrive with 0.5 sec accuracy.

Circuitry to accomplish the ambiguity resolution might be complicated, possibly involving multiple phase locked loops. In this memo, I report on tests of a very simple method of re-timing the received low frequency reference signals so that they have the same precision as the high frequency reference. The low frequency references can then be used in synthesis with the same precision as if the high frequency reference had been divided down in an ideal divider, but without the corresponding phase ambiguity.

CIRCUIT DESCRIPTION

The idea is to use a very fast D-type flip-flop clocked by the HF reference (500 MHz) to capture the next-slower reference (5 MHz); then to use the captured signal to clock another such flip-flop, capturing the next-slower reference (1 Hz); and then to continue in this way if necessary until the timing of all references is determined by the HF reference and the delays through the flip-flops. The circuit is shown conceptually in Figure 1. The stability of the flip-flop delays could determine the overall accuracy, so this was checked experimentally.

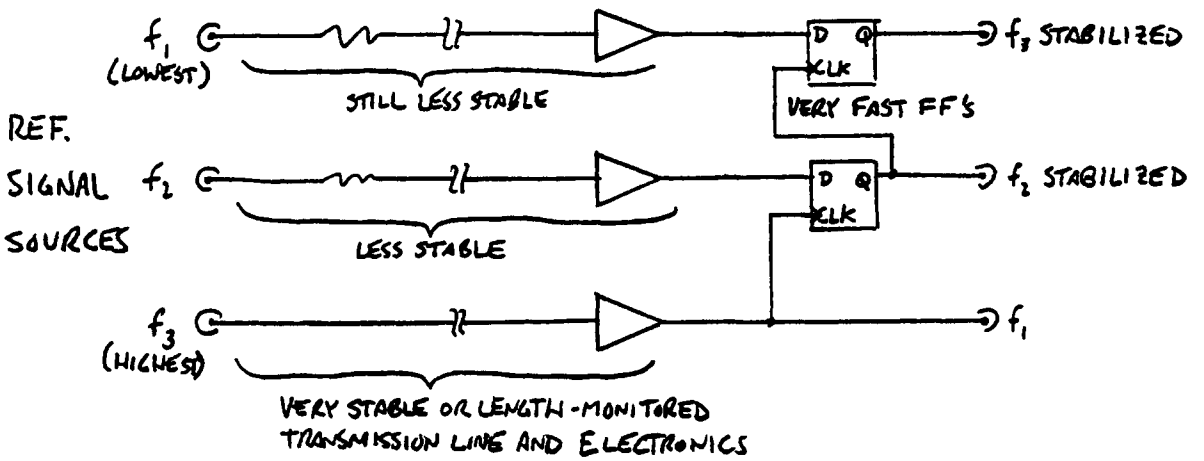


FIGURE 1: CONCEPTUAL CIRCUIT DIAGRAM

IMPLEMENTATION DETAILS

I chose the Gigabit Logic 10G021A Dual Precision Flip Flop as the basis of a test design. This is a GaAs chip of a proprietary type featuring maximum clock rates up to 2.3 GHz. A less expensive version (10G021A-3L) with maximum clock of 1.5 GHz was used for these tests. The detailed circuit is given in Figure 2, and portions of the chip's data sheet are reproduced in Appendix A.

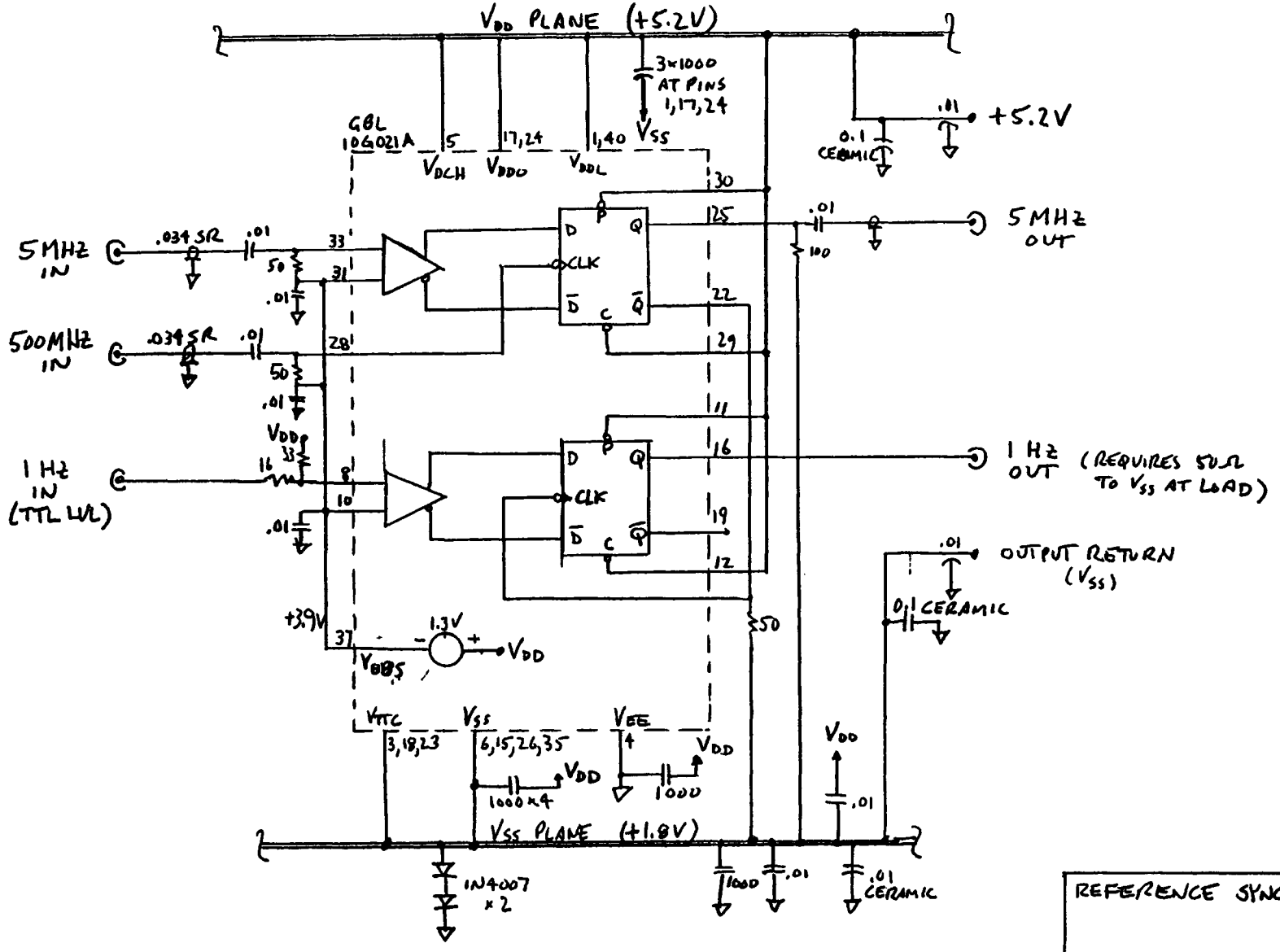
The chip is in a 40-pin PLCC that fits a special socket designed to support the fast signals (Gigabit Logic PN 90GSKT-40L). A small PC board was constructed on .010-inch thick glass-epoxy to allow narrow-width 50 ohm microstrip. This was mounted in a small aluminum box with SMA connectors for the signals. The 500 MHz and 5 MHz signals were brought to the chip through .034-inch semi-rigid coax. The chip requires several bias voltages between 0 and 5.2 V, and this complicates the layout. In a more complex circuit, the supplies should be on separate planes of a multi-layer board, but here I was able to get away with a two-layer design. Only one power supply was needed because I used a diode string to develop one of the bias voltages and an internal source in the chip for another. Nevertheless, careful attention to layout and bypassing was required, as indicated in Figure 2.

TEST RESULTS

The setup of Figure 3 was used to verify proper operation of the circuit. A 500 MHz sinusoid was applied to the clock input, and a 100 MHz sinusoid was applied to the "5 MHz" input. These frequencies were readily available and allowed easy viewing on the oscilloscope. An HP 54503A digitizing oscilloscope (500 MHz bandwidth) was used. Cable lengths were carefully equalized so that the relative timing of the waveforms seen on the oscilloscope was correct. A trombone line in the 500 MHz path allowed the triggering phase of the flip-flop to be adjusted. A typical result is shown in Figure 4. Note that the output transitions occur very near the positive-going zero crossing of the clock, even though the flip-flop is triggered on the negative-going clock edge. This indicates that the propogation delay is nearly 1000 psec, in rough agreement with the data sheet. The 100 MHz input waveform is somewhat distorted by mismatch and nonlinearity of the flip-flop input.

The temperature sensitivity of the flip-flop delay was evaluated using the setup of Figure 5. The Al box containing the flip-flop circuit was coupled to a peltier-controlled plate, which was enclosed in a cardboard box lined with 2 inches of plastic foam. The temperature on the side of the Al box was monitored with a thermister gauge. It was possible to change the temperature by 25 C and reach thermal equilibrium in about 15 minutes. All other circuitry was kept at lab ambient temperature. As before, 100 MHz was applied to the "5 MHz" input. The captured 100 MHz was compared in phase with the input 100 MHz using an HP 8405A Vector Voltmeter. Calibration was checked by moving the trombone line by a measured amount. Several temperature cycles from 13.5 C to 38.0 C were run; the results were quite repeatable, as follows:

phase change	0.25 deg at 100 MHz over 24.5 C
corresponding delay change	6.94 psec
temperature coefficient	0.28 psec/C.



ALL C's AND R's CHIP TYPE UNLESS NOTED

FIGURE 2

REFERENCE SYNCHRONIZER

LRD 920914

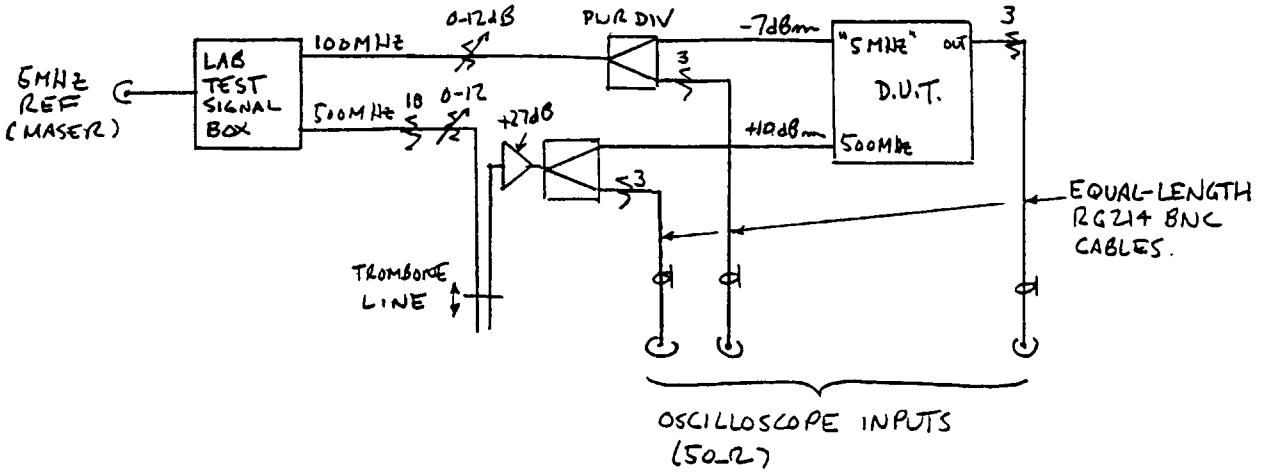


FIGURE 3: FUNCTIONAL AND TIMING TEST SETUP.

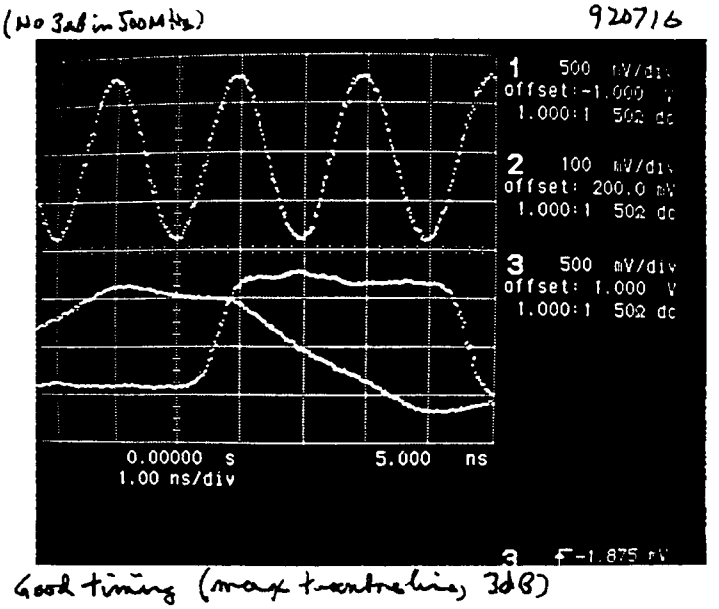


FIGURE 4: TYPICAL RESULT USING SETUP OF FIG. 3.

DISCUSSION

The temperature coefficient of delay seems remarkably small, especially considering that the typical total delay through the flip-flop is 850 ps. However, the result is consistent with the speed vs. temperature curves on the data sheet (see Appendix A). These show that the maximum clock rate peaks near room temperature, so that its temperature coefficient is near zero there. The delay should behave similarly. The typical maximum clock rate for the 10G021A-3 is shown as about 1.95 GHz at 0 C and about 1.80 GHz at 85 C; the difference between the reciprocal speeds is 42 psec over 85 C, or 0.50 psec/C.

DEVICE AVAILABILITY

The Gigabit Logic Corporation was purchased by TriQuint Semiconductor, Inc. in 1991. Unfortunately, TriQuint has decided to discontinue the entire GaAs IC product line to which the 10G021A belongs. They will continue to sell existing stock until it is depleted. As of August 1992, they had the following available:

68 ea.	10G021A-3L	(1.5 GHz)	$82.90 1-9
9 ea.	10G021A-L	(2.0 GHz)	$130.00
3 ea.	10G021A-2L	(2.3 GHz)	$156.00
?	10G021A-C	dice	

The dice will be put into packages if necessary to fill orders; there is no minimum quantity or extra charge for this. No more wafers can be made because the Gigabit fabrication process has been shut down. But some of the chips in this line might be re-designed to allow production using an existing TriQuint process.

Meanwhile, other suppliers of fast GaAs chips that might be suitable are scarce. One possibility is NEL Division of NTT Electronics Technology, in Japan (U.S. agent is KBK Inc., New York, 212/687-8564). They have a GaAs line that includes a single D flip-flop that claims 4 GHz maximum clock speed and 615 psec max delay, but the price each is $417.

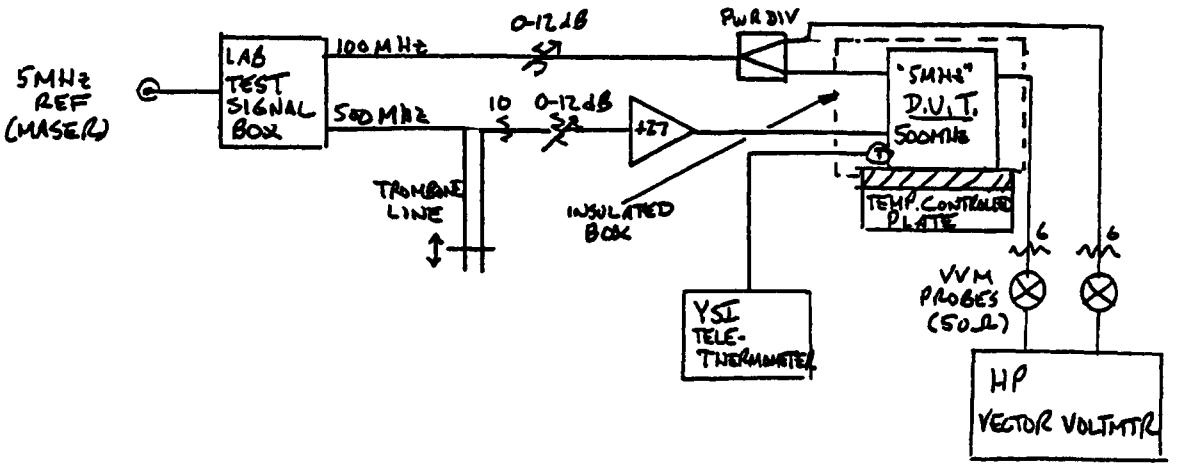


FIGURE 5: SETUP FOR TEMPERATURE COEFFICIENT MEASUREMENTS.

APPENDIX A: DATA SHEET, Selected pages.

GBL GigaBit Logic

10G021A
10G021AM

Dual Precision D Flip Flop
2.7 GHz Clock Rate
10G PicoLogic™ Family

FEATURES

- DC to 2.7 GHz operation
- 0°C to +85°C operating temperature range
- -55°C to +125°C military temperature range
- Ultra-low input sampling skew
- Individual clock, preset, and clear inputs on each flip flop
- Negative edge triggered flip-flop design
- ECL & PicoLogic™ compatible complementary outputs
- High gain ECL compatible differential inputs
- Output stage supports a wide range of load resistor and termination voltage combinations
- Available in 40 pin leaded or leadless chip carrier and dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

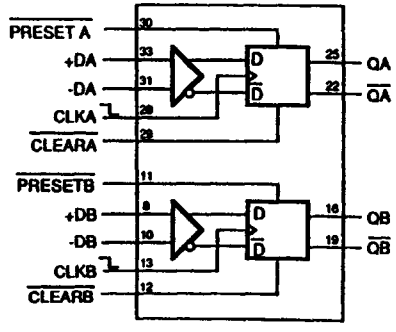
- Data repeaters/regenerators
- Decision circuits
- Synchronizers
- Data samplers

FUNCTIONAL DESCRIPTION

The 10G021A consists of two negative edge triggered precision D flip-flops capable of operating at clock frequencies of over 2 GHz. Each flip-flop features individual clock, preset, and clear inputs. Each half of the 10G021A contains a high speed differential data input to which the input signal is applied. When the input stage is used as a line receiver or amplifier the data inputs can be driven differentially for maximum noise immunity. The - D input may also be used as a reference input to allow selection of the switching threshold. When the - D input is connected to an ECL generated VBB the + D input can be driven from an ECL compatible source. The complementary outputs are ECL and PicoLogic compatible, and support a wide range of load resistor and termination voltage combinations. The output driver has been designed for maximum symmetry between Q and $\overline{Q}$ output waveforms. The design of the 10G021A is such that high and low input data are sampled at the same point in time relative to the falling clock edge. This eliminates pulse lengthening or shrinking encountered with traditional D flip-flops which sample high and low data a gate delay apart in time. The 10G021A's precise data sampling translates to ultra low data sampling skew. Thus the 10G021A's output data eye pattern is highly symmetrical minimizing distortion of regenerated data.

The 10G021A is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM



10G021A ORDERING INFORMATION

Pkg. Type	Min. Speed (0°C to 85°C) 2.3 GHz	2.0 GHz	1.5 GHz
C	10G021A-2C 10G021A-2L	10G021A-C 10G021A-L	10G021A-3C 10G021A-3L 10G021A-3X
Dice			

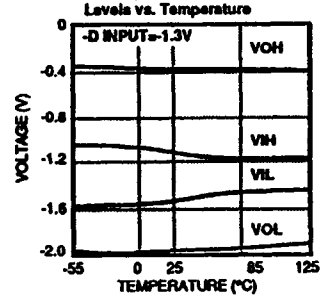
Pkg. Type	Min. Speed (-55°C°C to +125°C) 2.0 GHz	1.7 GHz	1.2 GHz
C	10G021AM-2C 10G021AM-2L	10G021AM-C 10G021AM-L	10G021AM-3C 10G021AM-3L 10G021AM-3X
L Dice			

GBL GigaBit Logic

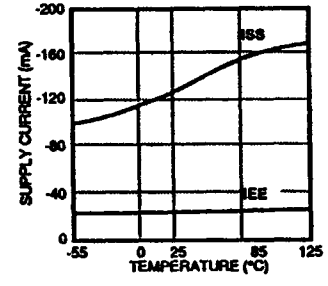
10G021A
10G021AM

TYPICAL PERFORMANCE CHARACTERISTICS

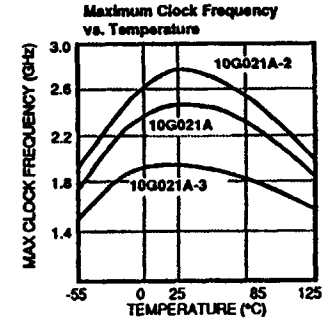
Data Input and Q Output Levels vs. Temperature



ISS & IEE vs. Temperature



Maximum Clock Frequency vs. Temperature



DC CHARACTERISTICS

Tc = 0°C to 85°C (10G021A); -55°C to 125°C (10G021AM), VSS = -3.5 V to -3.3 V, VEE = -5.5 V to -5.1 V, VDDL = VDDO = 0 V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input Voltage High; Clock, Preset, Clear Inputs	-0.8		VDDL	V	
VIL	Input Voltage Low; Clock, Preset, Clear Inputs	VTT		-1.7	V	
I IN	Input Current Clock, Preset, Clear Inputs	-250	225	600	µA	VIN: -0.8 V to -1.7 V
ISS	Power Supply Current		150	250	mA	
IEE	Power Suppy Current		35	100	mA	No Load
PD	Power Dissipation		700	1400	mW	

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	10G021A-2						10G021AM-2						Units	Notes
		0°C		Tc = +25°C			+85°C	-55°C		Tc = +25°C			+125°C		
		Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max		
1/T1	Max Clock Frequency	2.3		2.7			2.3		2.0		2.7			2.0		GHz	2, 6
T2	(+D)-(-D) Hold Time	0		0	-60		0		0		0	-80		0		ps	
T3	(+D)-(-D) Setup Time	250		250	165		250		265		250	165		265		ps	
T4	Preset Pulse Width	750		750	500		750		1000		750	500		1000		ps	
T5	Preset Low to Q High		700		575	700		700		850		575	700		850	ps	
T6	Preset Low to $\overline{Q}$ Low		700		575	700		700		850		575	700		850	ps	
T7	Clear Pulse Width	750		750	500		750		1000		750	500		1000		ps	
T8	Clear Low to Q Low		750		625	750		750		900		625	750		900	ps	
T9	Clear Low to $\overline{Q}$ High		750		625	750		750		900		625	750		900	ps	
T10	Clock Low to Q High		625		525	625		625		750		525	625		750	ps	
T11	Clock Low to $\overline{Q}$ Low		625		525	625		625		750		525	625		750	ps	
T12	Clock Low to Q Low		625		525	625		625		750		525	625		750	ps	
T13	Clock Low to $\overline{Q}$ High		625		525	625		625		750		525	625		750	ps	
Tr	Output Rise Time		220		180	220		220		240		180	220		240	ps	3
Tf	Output Fall Time		140		125	140		140		160		125	140		160	ps	3
	Clock to Output Skew		100		60	75		100		100		60	75		100	ps	4
	Input Sample Skew				25							25				ps	5
Tw	Clock Pulsewidth	200		180			200		200		180			200		ps	

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	10G021A						10G021AM						Units	Notes
		0°C		Tc = +25°C			+85°C	-55°C		Tc = +25°C			+125°C		
		Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max		
1/T1	Max Clock Frequency	2.0		2.3			2.0		1.7		2.3			1.7		GHz	2, 6
T2	(+D)-(-D) Hold Time	0		0	-50		0		0		0	-50		0		ps	
T3	(+D)-(-D) Setup Time	265		265	175		265		300		265	175		300		ps	
T4	Preset Pulse Width	1000		1000	670		1000		1300		1000	670		1300		ps	
T5	Preset Low to Q High		850		650	850		850		1050		650	850		1050	ps	
T6	Preset Low to $\overline{Q}$ Low		850		650	850		850		1050		650	850		1050	ps	
T7	Clear Pulse Width	1000		1000	670		1000		1300		1000	670		1300		ps	
T8	Clear Low to Q Low		900		700	900		900		1200		700	900		1200	ps	
T9	Clear Low to $\overline{Q}$ High		900		700	900		900		1200		700	900		1200	ps	
T10	Clock Low to Q High		750		600	750		750		950		600	750		950	ps	
T11	Clock Low to Q Low		750		600	750		750		950		600	750		950	ps	
T12	Clock Low to $\overline{Q}$ Low		750		600	750		750		950		600	750		950	ps	
T13	Clock Low to $\overline{Q}$ High		750		600	750		750		950		600	750		950	ps	
Tr	Output Rise Time		240		200	240		240		275		200	240		275	ps	3
Tf	Output Fall Time		160		150	160		160		220		150	160		220	ps	3
	Clock to Output Skew				75	100						75	100			ps	4
	Input Sample Skew				30							30				ps	5

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	10G021A-3						10G021AM-3						Units	Notes
		0°C		Tc = +25°C			+85°C	-55°C		Tc = +25°C			+125°C		
		Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max		
1/T1	Max Clock Frequency	1.5		1.8			1.5		1.2		1.8			1.2		GHz	2, 6
T2	(+D)-(-D) Hold Time	0		0	-40		0		0		0	-40		0		ps	
T3	(+D)-(-D) Setup Time	300		300	190		300		350		300	190		350		ps	
T4	Preset Pulse Width	1300		1300	870		1300		1500		1300	870		1500		ps	
T5	Preset Low to Q High		1150		900	1150		1150		1350		900	1150		1350	ps	
T6	Preset Low to $\overline{Q}$ Low		1150		900	1150		1150		1350		900	1150		1350	ps	
T7	Clear Pulse Width	1300		1300	870		1300		1500		1300	870		1500		ps	
T8	Clear Low to Q Low		1200		950	1200		1200		1400		950	1200		1400	ps	
T9	Clear Low to $\overline{Q}$ High		1200		950	1200		1200		1400		950	1200		1400	ps	
T10	Clock Low to Q High		1050		850	1050		1050		1250		850	1050		1250	ps	
T11	Clock Low to $\overline{Q}$ Low		1050		850	1050		1050		1250		850	1050		1250	ps	
T12	Clock Low to Q Low		1050		850	1050		1050		1250		850	1050		1250	ps	
T13	Clock Low to $\overline{Q}$ High		1050		850	1050		1050		1250		850	1050		1250	ps	
Tr	Output Rise Time		275		250	275		275		320		250	275		320	ps	3
Tf	Output Fall Time		220		200	220		220		275		200	220		275	ps	3
	Clock to Output Skew				125	175						125	175			ps	4
	Input Sample Skew				40							40				ps	5