THE OVLBI DECODER TEST FIXTURE

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1.0 GENERAL DESCRIPTION

This report describes a portable test fixture that generates a fairly complete simulation of the Radioastron and VSOP downlink data formats. It produces outputs containing the I channel bit stream, Q channel bit stream, and clock for any of four modes: Radioastron at 72 MHz, 36 MHz, and 18 MHz clock rates; and VSOP at 64 MHz clock rate. The astronomical signal portion of each frame consists of pseudo random noise that repeats every frame, but is different in the I and Q channels. The header portion of each frame is realistic, including variations from frame to frame as required to correctly represent frame counters and similar fields.

In addition, the test fixture accepts as inputs the signals that would appear at a VLBA Recorder's Formatter inputs and checks them for bit errors. That is, if the test fixture is used to generate data that is processed through an OVLBI earth station's Decoder for recording on the VLBA recording system, then the Decoder's output can be connected back to the test fixture (instead of to the Formatter) for error checking. Each erroneous bit in the signal portion of the frame can be counted. (However, one limitation is that only the signals corresponding to half of the downlink -- either the I or Q channel -- can be checked at one time.)

Further, the test fixture includes various features useful in testing, including the ability to turn differential encoding on or off, the ability to make frames slightly longer or shorter than normal, and the ability to introduce intentional errors in either the header or signal portion of some or all frames.

Although the design is especially well matched to the NRAO OVLBI Earth Station at Green Bank, it should be useful for testing other stations as well.

2.0 SETUP AND BASIC USER INSTRUCTIONS

The device is in a small box, about 25x20x13 cm. See the wiring diagram in Figure 1 for details of the external connections. It requires only d.c. power and a dumb ASCII terminal for control and readouts.

2.1 Power requirements

Rear panel connector, 5 pin Amphenol (mating connector and cable supplied):
+5.0 V at approximately 2.0 amperes.
-5.2 V at approximately 1.0 ampere.

2.2 Terminal interface

RS232, 3 wire connection, rear panel DB9 male connector.
Baud rate 9600, 8 data bits, no parity.
80-column lines assumed by software; a few ANSI escape sequences (like screen clearing) are used by the software, but generally a very

simple terminal is adequate.

2.3 Outputs

Two forms of output are provided:

2.3.1 Differential ECL on a 20-pin male IDC connector (compatible with ribbon cable connectors), with internal d.c. pulldowns provided. Each signal should be differentially terminated in a 100 ohm load.

2.3.2 Single-ended ECL on three SMA connectors, with no internal pulldowns. Each signal should be terminated with 50 ohms to -2.0 volts.

2.4 Inputs

Input signals are accepted on 40-pin IDC connectors identical in form and pinout to those used at the inputs of the VLBA Formatter. The cable to the Formatter contains 16 data signals (8 derived from the I channel and 8 from the Q channel), a 32 MHz clock, and a 1 Hz clock. The test fixture includes two such input connectors on the rear panel, one connected to the I channel signals and the clocks, and the other connected to the Q channel signals and the clocks. Only one should be used at a time.

2.5 Operation

After applying power, ensure that both front panel pilot lights are on. Then press the front panel "RESET" button to initialize the internal microprocessor. The prompt "OVLBI TESTFIX>" should appear on the terminal's screen. After that, various commands are accepted as explained under "Software" below. Typing H<CR> will produce a sequence of help screens that together describe all commands and give some other operating information. The first command needed is usually the one that loads the operating mode; it is one of L1<CR>, L2<CR>, L3<CR>, or LV<CR> for loading Radioastron 18 MHz, Radioastron 36 MHz, Radioastron 72 MHz, or VSOP 64 MHz, respectively. After entering one of these commands, data for that mode is being produced at the outputs.

3.0 HARDWARE DESCRIPTION

Details of the test fixture are seen in logic diagram 34227L003 (computer file L003D01.SCH), reproduced in Figure 2. This shows the internal wirewrap card that contains all of the circuitry not shown on Figure 1. The major divisions of this drawing include:

1) microprocessor
2) test frame generator
3) differential decoder
4) error detector
5) error rate measurement

The usual system hook-up when using the test card to test the OVLBI decoder is to drive the decoder satellite input from the IDATA-QDATA-CLOCK test fixture output (all are differential ECL signals).

The decoder output, which normally will drive a VLBA formatter, can then be connected to the formatter interface input of the test fixture. Only one half of the decoder output can be tested at a time. Thus, with either the I data output or the Q data output of the decoder connected to the test fixture, the integrity of data through the decoder can be tested. The test fixture will monitor the decoder output and detect all deviations of this output from its own frame data contents.

The test fixture will ignore the decoder output during times when satellite headers are being output (actually, the headers are replaced at the decoder output with pseudo random data). Counters on the test fixture can count bit deviations of the decoder output from the frame contents so that a bit error rate can be determined.

3.1 Microprocessor

The microprocessor used on the test fixture is an 87C51. It has 32K of external UVROM (IC 9B) and 32K of external RAM (IC 9A) and supports communication with a terminal via an RS232 serial port. The microprocessor is connected to the rest of the test fixture logic through ICs 9D, 8E, 8B, 8C, and 8D. Error counters ICs 7D and 7E are also ports from the hardware into the micro. The microprocessor functions include;

1) communication with a terminal
2) establishing the test fixture mode (VSOP, Radioastron 72-MHz, Radioastron 36-MHz or, Radioastron 18-MHz)
3) filling the 6A/5A, 6C/5C, 6D RAM frame buffer with data for one satellite frame
4) servicing the 6B, 5B, 5D FIFO memories when an active header is required
5) reading the 7D and 7E error counters and tabulate the error counts

The microprocessor can both write to and read the frame buffer made up of RAMs 6A/5A, 6C/5C and 6D. Tranceivers 8B, 8C, and 8D provide the path for data between the frame buffer and the micro. Upon microprocessor reset, or when a mode change is requested vis the terminal, the micro will fill the frame buffer with bytes for one satellite frame (in Radioastron mode the buffer could actually hold as many as three frames but the extra capacity is not used).

The I-channel and Q-channel RAMs (6A/5A and 6C/5C respectively) are both filled with a 15-bit pseudo-random pattern throughout the data portion of the frame. The seed pattern for the two channels are different resulting in the same pattern in both but offset in time by a large fraction of the pattern length. The microprocessor will shift the random pattern 8 times between each RAM location insuring that there is no short term correlation between the 8 bits within a frame byte.

Starting at RAM location 4E02 for Radioastron or at RAM location 9C3A for VSOP, the microprocessor will write a frame header. A terminal flag is written into the 6D RAM to establish the frame length (at RAM address 4E1F for Radioastron or at 9C3F for VSOP).

Once the frame buffer has been filled, it will free run and output data for satellite frames into registers 2B and 3C. The frame buffer needs no microprocessor intervention except where an active header is desired. Except where an active header is being supported, the contents of every frame will be the same.

In order to support an active header, the microprocessor will read the frame buffer starting at RAM location 4DF0 for Radioastron or at 9C10 for VSOP through 48 bytes of all RAMs. The micro does this RAM read just after the "0" command is issued. It will put the contents of the RAMs into a file within its own external RAM (starting at memory location 0100). This data file will be used to fill the FIFO memories every frame. This action insures that there is no data change within a frame when the active header is turned on. (The act of the microprocessor reading the frame buffer RAMs will, of course, disrupt the satellite frame completely since the micro must take over the RAM address counters in order to read them).

3.3 Frame Buffer

The frame buffer consists of binary counter ICs 7A and 7B which generates the RAM address, RAMs 6A/5A for the I-channel data, RAMs 6C/5C for the Q-channel data, RAM 6D for parity and control, FIFOs 6B (I-channel), 5B (Q-channel), and 5D (parity/control) and control PAL 7C.

RAMs 6A/5A are tri-stated with the 6B FIFO, RAMs 6C/5C are tri-stated with FIFO 5B, and RAM 5D is tri-stated with FIFO 5D. PAL 7C switches between the RAMs and the FIFOs when the active mode is enabled providing data for the satellite frames. In operation, the switch between RAM and FIFO is controlled by bits TS0 and TS1 from RAM 6D or FIFO 5D. The intention is that when an active header is selected, control will switch from the RAMs to the FIFOs 48 bytes before the end of a satellite frame (RAM address 4DF0 for Radioastron or 9C10 for VSOP). Thus, 48 bytes of every satellite frame (the very last part of which is the header) will come from the FIFOs. The FIFO contents must be supplied by the microprocessor writing at least 48 bytes into them prior to the end of every frame. This data can then be made to change from frame to frame with appropriate software in the micro.

MODE6 (from P1.4) is the microprocessor term that controls if the active header is selected. If MODE6 is high, the FIFO will be selected every frame to provide a portion of the satellite frame data. The FIFOs are 64 deep but normally only 48 bytes of the FIFO depth is used. The remaining FIFO storage is available to force long frames by using the microprocessor I and J commands (to be described later). When a TS0 = 1 AND TS1 = 0 state is detected by the 7C PAL, control is switched to the FIFOs. Control reverts to the RAMs when the 7C PAL detects that TS1 = 1.

The terminal flag left in the 6D RAM (or the 5D FIFO) is recognized by PAL 7C and results in the signal TS2 becoming active for one clock. The TS2 signal resets the 7A, 7B frame counter and starts another frame. RAM 6D also has the byte parity bits in Radioastron mode.

The FIFO map seen on the test fixture schematic (bottom-center) give useful memory locations for both the frame buffer and microprocessor. For example, at the Radioastron map location marked "1st BYTE OF HEADER", the frame buffer memory location is given as 4E02 (in all RAMs, 6A/5A, 6C/5C, and 6D). When this part of the frame buffer is read and stored in the micro external RAM as describe above, the contents wind up in micro RAM locations 0136 (I data), 0137 (Q data), and 0138 (parity). There is also an error mask in the micro RAM to be described later that is in memory location 0036, 0037, and 0038.

3.4 Differential Encoder

Both the parallel to serial convertors and the differential encoder are described in this section. Parallel to serial conversion of the RAM/FIFO 8 (for VSOP) or 9 (for Radioastron) bit wide outputs is done in ICs 2B and 3C. PAL 3B select the appropriate crystal oscillator (72-MHz for Radioastron or 64-MHz for VSOP) and divides it by 1, 2, or 4 (2 or 4 for Radioastron only) depending on the mode. This PAL also develops the STB signal needed by 2B and 3C. Signal STB is a 1-in-8 strobe for VSOP and a 1-in-9 strobe in Radioastron mode.

PAL 2C does the differential encoding to simulate the actual operation on the spacecraft. The MODE2 signal, controlled by the micro, can enable or disable the encoding function. When the differential encoder is disabled I and Q data flows unmodified through the 2C PAL. IC 1C converts the test fixture to ECL logic levels.

3.5 Error Detector

Either the I data or the Q data output of the decoder can be connected to the test fixture for verification. ECL to TTL translators 1D, 1E, and 1F convert the decoder output (which normally drives a VLBA formatter) into TTL logic levels. The 1B PAL takes the 32-MHz formatter clock and divides it down to 8-, 4-, or 2-MHz synchronizing the final output to the decoder data by using the formatter 1 second tick.

ICs 4D and 4C perform a dual function. Output pins 14, 15, and 16 of PAL 4D form a 4-state state machine used to detect the start of the data portion of a satellite frame as it comes out of the decoder. The first three data bytes of every frame is set by the microprocessor as being 1D, F8, 4C for I data or 34, 9A, BB for the Q data path (this is set by the pseudo-random data generator seed discussed earlier).

PAL 4D will look for one of these sequences (which one it looks for is set by the microprocessor MODE7 signal). If the rest state of PAL 4D is considered to be STATE0, it will advance to STATE1 (4D pin 15 high) when is detects a HEX 1D (in I data mode) at the I/Q data inputs. If the PAL is in STATE1 it advances to STATE2 (4D pin 16 high) if the byte following the HEX 1D is F8 (for I data), otherwise it returns to STATE0. If the PAL is in STATE2 and the very next byte is a 4C, PAL 4D pin 14 (SYNC) goes high for one clock cycle indication sync detection.

One problem with the sync detector exists. In VSOP mode, a frame is 40,000 bytes long but the 15-bit data generator will start to repeat itself after 32,767 bytes (clocks). Thus, the sync sequence can be expected to occur twice every VSOP frame. A term, Q15, from the frame predict counter (PALs 4A and 4B) allows the sync detector to ignore the second occurrence of the sync code in a frame.

The second function provided by PALs 4D, 4C is to generate a 15-bit pseudo-random data pattern that should predict the decoder output once frame sync has been detected. The 15 flip/flops, FB0 through FB14, are distributed between the two PALs. The only unusual thing about the data generator is that it must advance by 8 states every clock to reproduce the test frame generator output.

Normally, a 15-bit feedback shift register would have 15 flip/flops and one EX-OR feedback gate. For a 15-bit data generator, stages 15 and 14 would be EX-ORed to provide input for shift register stage 1. In order to shift 8-states per clock, however, the EX-OR of stages 15 and 14 drives the input of shift register 8 instead of stage 1. The input to shift stage register 7 is driven by the EX-OR of stages 14 and 13 and so on until shift register stage 1 is driven by the EX-OR of stages 7 and 8. Thus by having 8 EX-OR gates instead of one, every shift register stage can look ahead 8 clocks and effect the 8 shifts per clock desired.

The COMPARE signal generated by PALs 4A and 4B causes the 15-bits of the data generator to be parallel loaded during the frame header to the appropriate state for the start of the data portion of a frame. This will allow them to predict the decoder data output for the rest of the frame.

PALs 4A and 4B form a receive data frame counter. The decoder substitutes an unpredictable random data pattern at its output for the header portion of every satellite frame and the test fixture must have a mechanism to ignore this part of the decoder output. Every time frame sync is detected by PAL 4D, the frame counter implemented by PALs 4A and 4B is initialized. The counter will then free run, predicting the frame header positions until re-initialized by subsequent sync detections. The free run ability of this counted means that a missed sync detection,

due to a bit error, will not cause a failure in the error detection process.

The output of the 4A, 4B receive frame counter is the signal COMPARE which should exactly spans the header part of the decoder output.

PALs 3E and 2E compare the decoder output clock by clock with the predict data generator of PALs 4D and 4C (4-bits in each PAL). The error detectors can function in two modes as specified by the micro processor MODE4 term. If MODE4 is low, PALs 3E or 2E will latch in the error state whenever a deviation between the decoder output and the predict generator is detected. If MODE4 is high, the error detection is not-latching or momentary, i.e., every time an error is detected, a pulse will occur at the PAL 3E, 2E output. When latched in the error state, the PALs can be reset with the RST-A or RST-B signals.

The COMPARE signal causes the error detector PALs to ignore the decoder output for the duration of the frame header.

3.6 Error Rate Measurement

The error rate measurement is done in ICs 3D, 7D, and 7E. One of the eight error outputs of the 3E, 2E PALs, ERR[7..0], is selected by mux 3D and every error is counted by 7D and 7E. The error detect PALs must be in the momentary detection mode for this measurement to be made.

The microprocessor has software in it that will automatically rotate through all 8 error output of the 3E, 2E PALs. Every frame, the micro will read the error count for one frame and then advance to the next ERR[7..0] term. Tabulations of the error counts for errors made on the 8 error lines are kept in the microprocessor and a formatted bit error rate display is available on the test fixture terminal.

4.0 SOFTWARE

The modules that make up the software for the test fixture are contained in these source files:

TF-MAS.ASM
TF-TEST.ASM
TF-HEAD.ASM
TF-OBS.ASM
TF-MON.ASM
TF-HELP.ASM
TF-MASK.ASM

Each is described in one of the following subsections. Copies of the files are available from the author upon request.

4.1 TF-MAS.ASM

TF-MAS.ASM contains the interrupt vectors and the routine executed upon hardware reset. After a reset, the card is initialized and the frame buffer filled with data to support VSOP mode.

Subroutine FILLTFR is called to fill the frame generator. As described earlier, a 15-bit pseudo-random data pattern is written into the data portion of the frame. Different data generator seeds are used for the I and Q channels insuring that the I data and Q data streams are different.

4.2 TF-TEST.ASM

TF-TEST.ASM has various test routines in it that can be used to test the test fixture itself. The most important of these tests

are TEST2, TEST3, and TEST4. When invoked, these tests will write data patterns to the I-data RAMs, the Q-data RAMs or the parity/control RAM and then read the patterns back to verify proper operation of the RAMs. The test will loop performing the selected test until the space bar is pressed.

4.3 TF-HEAD.ASM

TF-HEAD.ASM has the active header subroutine in it (HEADER) and canned satellite frame headers FILLTFR uses when it writes into the frame buffer.

4.4 TF-OBS.ASM

TF-OBS.ASM has operational software in it. Entry into this module is made via the monitor "O" command. Entry is at label OBS. Upon entry, the card is prepared for more dynamic operations than just outputing static frames. The routine labeled GETINFO will read through the frame buffer starting 48 bytes before the end of frame and copy the contents of that portion of the frame buffer into the microprocessor external memory starting at memory location 0100. When an active header is selected, this information will be written into the frame FIFOs once a frame. This is done to insure that, initially, the FIFO data will exactly duplicate the frame buffer RAM contents.

A parallel buffer starting at location 0000 in the micro external RAM is then cleared. This part of memory can be used in an error creating mechanism programmed by the monitor I, and J commands (to be explained later).

A file starting at memory location 0300 is also cleared. This file will be used in the VSOP active header routine.

Finally, the IT0 microprocessor interrupt is enabled. After entering OBS, the following conditions prevail;

1) Mode selection is VSOP or Radioastron depending upon what was selected before the "O" command was given.
2) The file starting at loc 0100 has the current frame buffer data, unchanged, in it.
3) The file starting at loc 0000 has been cleared.
4) Active header mode has been selected.
5) Latched error LED mode has been selected.
6) The error storage area starting at loc 0200 has been cleared.
7) The VSOP data file starting at loc 0300 has been cleared.
8) Error print-out has been disabled.
9) The microprocessor frame interrupt has been enabled.

After the frame interrupt has been enabled, the microprocessor will enter an idle loop waiting for frame interrupts. Every time such an interrupt has been detected, the INT0V routine is executed. This routine does the following:

1) Clock the result of the last frame's error detection count into secondary storage (in the 7D, 7E chips), set-up the error counter to the next error line (ERR0 through ERR7), and reset the active error counter (also in the 7D, 7E chips).
2) Read the error counts just strobed into secondary and store them to be added later to the microprocessor running error counts.
3) Write 64 bytes into each of the three FIFOs. The data thus stored will be used in next test fixture satellite frame if active headers are enabled.
4) Support the monitor I, J error commands.

5) Tabulate the error just stored into the microprocessor running error counts.
6) Reset the interrupt.
7) Call the active header routine.
8) Set a flag for the idle loop.
9) Return from interrupt.

Upon return from interrupt, the idle loop will detect the occurrence of the interrupt and go support the screen error print-out routine if it is selected.

4.5 TF-MON.ASM

The TF-MON.ASM module has the software to support the monitor routine. The options available in the monitor are given in the help screen which uses the TF-HELP.ASM module. Below is a brief description of the monitor options by help screen;

4.5.1 HELP screen 1

LV, L1, L2, L3 will initialize the test card and load its frame generator RAMs to support VSOP, Radioastron 18 MHz, Radioastron 36 MHz, or Radioastron 72 MHz respectively. This command should be used after a card reset only.

IXXXX, JYY, and KZZ are commands that can be used to set up recurrent error conditions in the test fixture frame output. The IXXXX is the period of the error loop in satellite frames, JYY is the error pattern duration within the loop defined by I, and KZZ sets up the type of error. The IXXXX command will set up a loop of XXXX frames over which the J and K options will repeat. Thus, if XXXX = 5DC0 (24,000 in base 10), the condition set up by J and K will re-occur every 60 seconds in Radioastron 72-MHz mode. For J04 (YY = 04), the error will occur 4 satellite frames in a row. The KZZ command will cause the microprocessor to load one of the canned FIFO masks in TF-MASK.ASM into the file starting at location 0000. This file is EX-ORed with the FIFO file starting at loc 0100 as set by the IXXXX and JYY instructions. For K00 (ZZ = 00), canned error mask 00 is selected (CAN0 in TF-MASK.ASM). It will make one error in all 8 bits of one byte in both the I channels and in the Q channel once per frame. The K option need not be used, an operator can use the monitor modify command to write into the file starting at loc 0000 and get any error condition desired. Parity errors, data errors, sync errors, long frames, or short frames can all be make by inverting the proper bit or bits in the file downloaded to the FIFO.

The O* (the * indicated that this is a single key stroke command, no terminal c/r is needed) will start the test fixture into its active mode. A number of monitor options are effective only after the "O" command has been issued. The E* command will return the test fixture microprocessor to a passive state.

The B* command will control the terminal bit error readout. This function cycles between three states, not printing , printing one line of errors for every 1,000,000 bits tested (per ERR7 through ERR0 line), and printing one line of errors for every 256,000,000 bits tested. When the "O" command is first used, the non-printing mode is selected. The first time the B command is issued, the 1,000,000 bit printout option is entered. The next time the B command is used, the 256,000,000 bit printout option occurs. The 3rd B command returns to the non printing mode, and so on. In both printout modes, each entry in the an error line is calibrated in bit errors per 1,000,000 bits. Errors are cleared between every printout line except when the monitor "Q" command is used. The Q command toggles between clearing and non

clearing.

The U* command will toggle the differential encoder on and off.

The V* command will reset the error LEDs in latched LED mode.

The W* command will toggle between latched and non-latched (momentary) error LED operation.

The X* command toggles between the test fixture expecting to test the I decoder output and the Q data decoder output. The test fixture defaults to the I data.

The Y* command toggles between an active and a non-active header. When an active header is selected, the FIFO memories provide the information for a portion of every frame.

The Z* command will cause the use of the error mask (at microprocessor location 0000) to be used once (bypassing the need for the IXXXX and JYY commands).

The 0*, 1*, 2*, and 3* commands affect the operation of the display, page, and modify monitor commands. After the 0* (zero, not letter O) command these functions act on the microprocessor external RAM memory (and is the default condition). After the 1*, 2*, or 3* key strokes, the three monitor commands act on the I data, the Q data or the parity/control RAMs, respectively.

The 8* and 9* commands cause the microprocessor to skip or repeat VSOP data commands when active header mode is selected.

4.5.2 HELP screen 2

This HELP screen defines the internal tests of the test fixture card itself. The most important tests are TEST2, TEST3, and TEST4 which test the test fixture frame generator RAMs.

4.5.3 HELP screen 3

This HELP screen gives the utility monitor options.

The DXXXX, PXXXX, and MXXXX YY .. ZZ monitor commands will display 16 bytes, display 256 bytes or modify bytes starting at RAM location XXXX. Which RAM that is affected is a function of the S*, 0*, 1*, 2*, and 3* commands. After the D of P commands, additional carriage returns will display subsequent bytes from memory. Special DH or MHX YY .. ZZ exist to display or modify VSOP data storage. DH will display all 16 VSOP data type and MHX YY .. ZZ will write YY .. ZZ (for up to six bytes) into data type X (x = 0 through F).

The R and RXX YY .. ZZ will display or modify the microprocessor internal RAM memory. R will display all 256 bytes and RXX YY .. ZZ will start modifying the RAM at loc XX.

The GXXXX will goto memory loc XXXX.

The TX command will execute TESTX. To exit a test, hit the space bar. A special test is TM which will test the microprocessor external RAM memory.

The H or ? command will type the help screens.

The A* command will repeat the last monitor command. This option allows a single key stroke entry for repetitive commands. Not all monitor commands are supported by the A command.

The S* command will switch the D and P commands from the external microprocessor RAM to the external ROM memory.

The .* command will clear the terminal screen.

4.5.4 HELP screen 4

Help screen 4 given the canned error mask files available.

4.6 TF-HELP.ASM

HELP.ASM contains ASCII files for the terminal help screens.

4.7 TF-MASK.ASM

TF-MASK.ASM has several canned error masks that can be whisked into the file storage starting at memory location 0000 with the monitor "K" instruction. These masks can be EX-ORed with the file starting at location 0100 to cause known deviations from the fixed frame content. The monitor I and J commands control the application of the loc 0000 file.

By using these files, controlled data errors, parity errors, long or short framers can be transmitted to test the decoder error handling capability.

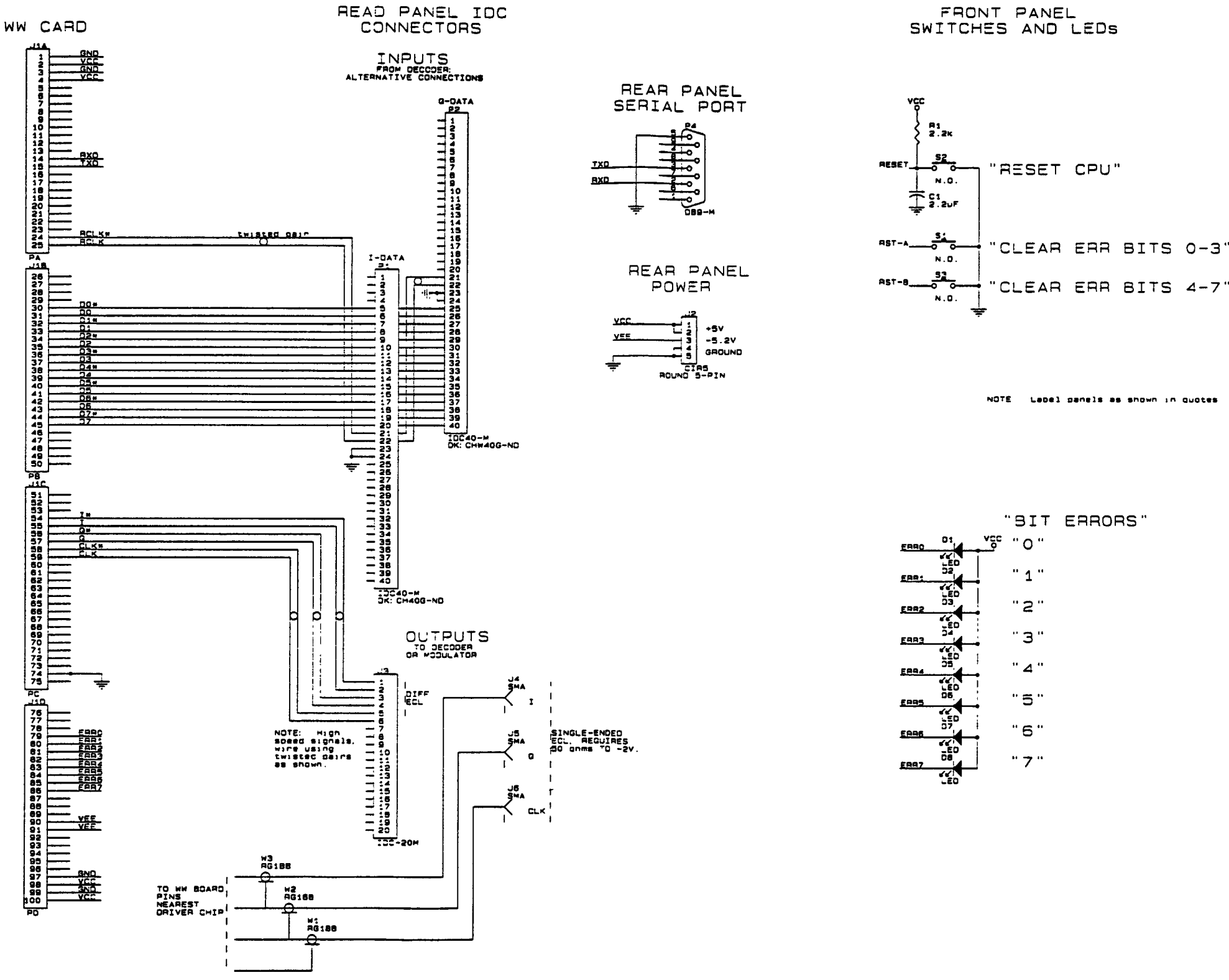
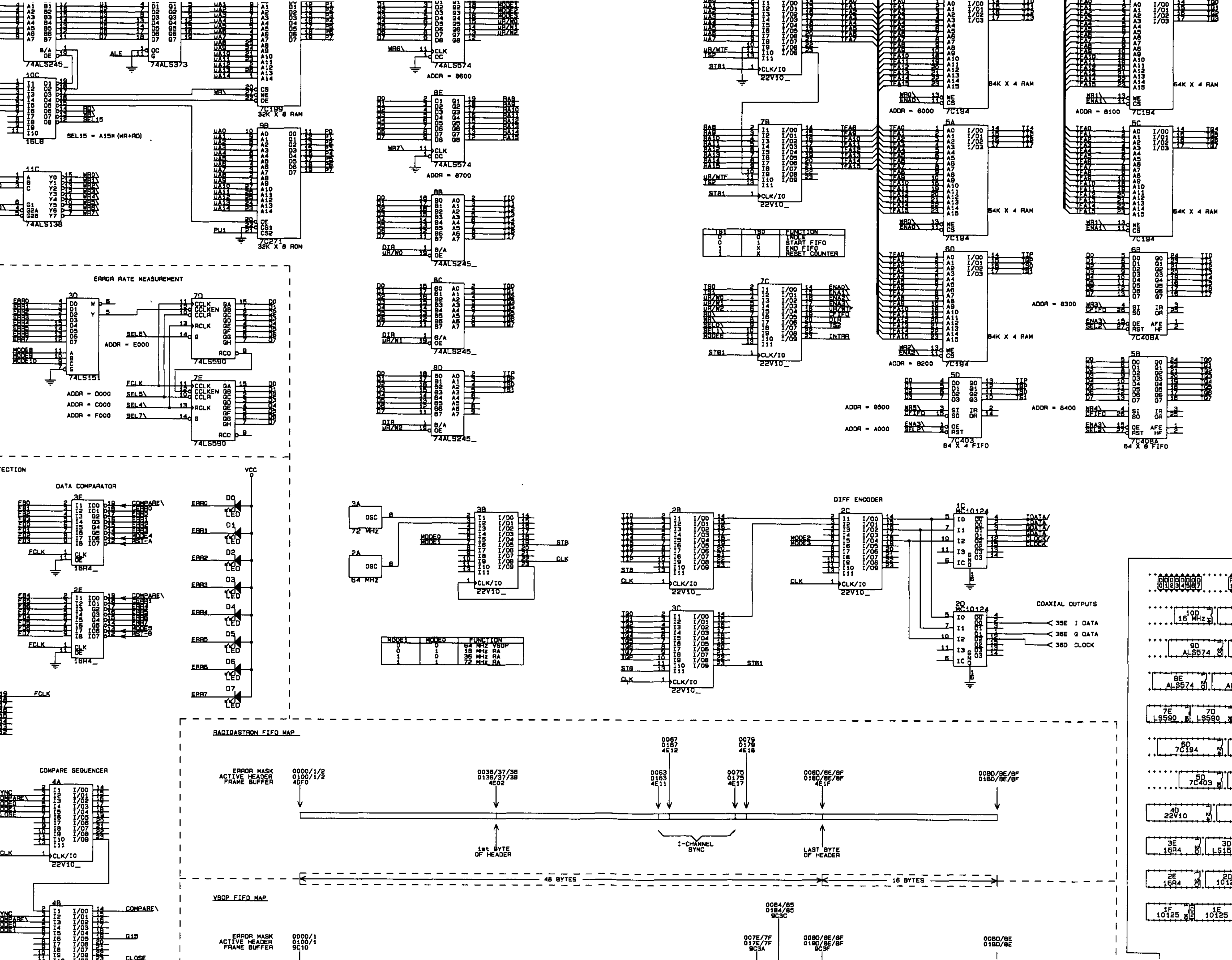

WW CARD
READ PANEL IDC CONNECTORS
INPUTS
FROM DECODER:
ALTERNATIVE CONNECTIONS
Q-DATA
I-DATA
IDC40-M
DK: CHW40G-ND
IDC40-M
DK: CH40G-ND
OUTPUTS
TO DECODER
OR MODULATOR
DIFF ECL
SINGLE-ENDED ECL. REQUIRES -2V.
NOTE: High speed signals, wire using twisted pairs as shown.
TO WW BOARD PINS NEAREST DRIVER CHIP
IDC-20M
REAR PANEL SERIAL PORT
TXD
RXD
DB9-M
REAR PANEL POWER
+5V
-5.2V
GROUND
CIRS
ROUND 5-PIN
FRONT PANEL SWITCHES AND LEDs
VCC
R1 2.2k
RESET
"RESET CPU"
C1 2.2uF
RST-A
"CLEAR ERR BITS 0-3"
RST-B
"CLEAR ERR BITS 4-7"
N.O.
NOTE Label panels as shown in quotes
"BIT ERRORS"
"0"
"1"
"2"
"3"
"4"
"5"
"6"
"7"

FIGURE 1



TS1	TS0	FUNCTION
0	0	IDLE
0	1	START FIFO
1	X	END FIFO
1	X	RESET COUNTER

MODE1	MODE0	FUNCTION
0	0	64 MHz VSOP
0	1	18 MHz RA
1	0	36 MHz RA
1	1	72 MHz RA