VSOP COMPATIBILITY TESTS AT GREEN BANK, SEPTEMBER 1994

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Abstract: Tests were conducted for four days using the NEC Satellite Simulator and the Green Bank Earth Station. Signals were coupled radiatively between the 14-m antenna and a small horn connected to the simulator about 30 m away. The downlink signal was successfully demodulated, with reliable locking of the Costas loop and clock recovery loop over a wide dynamic range. Reliable frame synchronization was achieved in the Decoder, the header processing software was verified, and the bit error rate was measured. More than one hour of header data, originating in the simulator's ROM, was recorded on the station computer's disk. The simulator was then locked to the station's uplink transmitter and it was verified that two-way lock was maintained while the transmitter frequency was varied over +-500 kHz (more than the maximum Doppler range). These significant successes were offset by the following difficulties: the downlink bit error rate was unacceptably high, and the two-way timing transfer could not be tested because of a failure of the station's downlink phase detector. These problems will be corrected in the near future.

1. INTRODUCTION

From September 24 through 28, 1994, Kesato Takahashi of NEC and Zen-Ichi Yamamoto of ISAS visited Green Bank and brought with them the Satellite Simulator that NEC has constructed for testing of tracking stations in both the U.S. and Japan. Their instrument is described in [1] and its block diagram is reproduced in Figure 1. All of the critical subassemblies are electrically identical to those used on the spacecraft.

The purpose of the visit was to establish compatibility of the Green Bank Earth Station with the satellite by coupling the Simulator to the Station radiatively and operating both uplink and downlink as if the satellite were in orbit. Although Doppler effects could not be simulated (there being no relative motion), it was hoped to verify the stability of the two-way timing link as well as to check the demodulation, decoding, and higher-level processing of the wideband data.

2. SETUP

2.1 The Satellite Simulator

The Simulator includes a 15.3 GHz receiver that locks a 50 MHz VCXO to the received carrier; an LO generator that produces the 14.2 GHz downlink carrier and the 128 MHz data clock using the VCXO as reference; a QPSK modulator at 14.2 GHz; and a data formatter that will digitize one or two baseband signals (in any of the VSOP modes) and insert header data to form the I and Q data streams to the modulator. There is also a diplexing filter that puts the uplink input and downlink output signals on the same coaxial port; the downlink portion of this filter limits the bandwidth to about 250 MHz. These subassemblies are equivalent to their counterparts on the satellite. In addition, the Simulator includes a controller (not part of the flight hardware) that can generate simulated header data, with the information bytes supplied by user-set switches or by a ROM that contains about 1 hour of varying header data. The main flight component not included in the simulator is the downlink power amplifier.

There are two other features specifically for the ground tests. The formatter allows external downlink data signals (I, Q, and clock) to be substituted for those generated in the simulator. The external data are recaptured and differentially encoded before being supplied to the modulator, but otherwise are unprocessed. Also, the modulator output is available before the diplexer, allowing use of separate connections for the uplink and downlink signals. Internal mode controls determine whether the external or internal data source is used, and in the latter case, which of several digitization modes is used. It is also possible to turn the modulation off so that only the carrier is transmitted.

2.2 Arrangement of Equipment

A 10x20 cm rectangular horn was mounted about 6 m above ground level on a tower about 30 m from the 14m earth station antenna. The horn was connected by flexible waveguide to a small shed at the base of the tower where the NEC simulator and other instruments were installed. With the 14m antenna pointed toward the tower at 3.5 deg elevation and the horn pointed to -3.5 deg elevation, the horn illuminates the lower quadrant of the main reflector. (An earlier setup had the horn 2.5 m above ground level and aimed upward so as to couple to the earth station's vertex optics by looking past the edge of the subreflector. While adequate signal strengths could be obtained, this arrangement proved to have excessive multipath, leading to large gain variations across the signal bandwidth. Swept measurements of the final setup showed a waveguide-in-to-IF-out flatness of better than 2 dB over 400 MHz.) The horn was set for horizontal polarization, and was found to couple about equally into the RCP and LCP receiving channels.

For most of the tests, the "satellite" equipment was arranged as shown in Figure 2a. The simulator was locked to a 15.3 GHz signal from an HP8672A synthesizer, and its output was taken from the modulator directly to the waveguide. Note that this omits the diplexer from the downlink path. The downlink data source could be either from the simulator or from the NRAO Decoder Test Fixture [2]. In the first case, the data portion of each frame is obtained by digitizing externally supplied signals. We arranged a chain of amplifiers and attenuators so that, in lab tests, identical broad-band noise with a PSD of -8 dBm / 32 MHz was supplied to each input (the nominal level is -5/32 dBm/MHz [1]). Note that with no inputs the data portion of the frame is expected to be all zeros or all ones, although this was not confirmed.

In order to check the downlink with the diplexing filter in the path, the arrangements of Figure 2b was used. The HP synthesizer was still used for the uplink. To allow two-way communication to the Earth Station, the setup was modified slightly to that of Figure 2c. The simulator's receiving level is only -73 to -113 dBm, whereas its output is -15 dBm; this causes more attenuation to be needed in the uplink path than in the downlink path.

Figure 3 is a simplified block diagram of the earth station modules that were involved in the tests.

3. TESTS AND RESULTS

3.1 Laboratory measurements of Simulator

We began by making some simple measurements of the simulator in the laboratory. We connected an HP8672A synthesizer, set to 15.3 GHz, to the diplexer and verified that the simulator locks over the specified range of power (-73 to -113 dBm); in fact, it exceeded the spec by 5 to 10 dB on each end. We also checked that it locks over the specified frequency range (+-460 kHz from nominal).

Then we connected the modulator output to a spectrum analyzer and recorded spectra under a variety of conditions. Figure 4 shows the unmodulated downlink spectrum at three different scales. There is measurable phase noise within 100 kHz of about -96 dBc/Hz at 10 kHz offset, falling to -108 dBc/Hz at 100 kHz. There are also -56 dBc spurs at +-1 kHz. We do not know the origin of these and did not investigate; it is possible that the spurs were on the synthesizer signal used as the reference. In any case, the performance is satisfactory.

Figure 5 shows the modulated spectrum under four different conditions. Unless otherwise noted, the digitization mode was 2 channels, 2 bits/sample, 32 MHz sampling rate (VLBA compatible mode); other available modes included (2,1,64 MHz), and (1,2,64 MHz). In Figure 5a, no baseband signals were intentionally applied to the Simulator, but the channel A input was open circuited and channel B was terminated. In Figure 5b, a sinusoidal signal was applied to both inputs. In Figures 5c and 5d, broadband noise (about 1 MHz to 300 MHz) was applied (same signal to both inputs) at approximately the nominal spectral density; Figure 5c used the 2-channel, 1-bit mode. Note that the dynamic range of these plots is limited by the spectrum analyzer's noise, which is -62 dBm at this resolution.

3.2 Downlink data transmission tests

Using the setup of Figure 2a, we transmitted the downlink signal from the Simulator to the Station and attempted to demodulate and decode it. However, reliable locking of the Demodulator's Costas loop was not obtained, and consequently the data could not be properly decoded. Nevertheless, the Decoder was occasionally able to obtain frame sync when data from the NRAO Test Fixture was being sent, but not with header data from the NEC Simulator. To accomplish this much, it was necessary for us to reverse the "I" and "Q" channel outputs of the Demodulator, but otherwise the differential decoding was found to be correct (since, even when we supply the data, the differential encoding is done in the Simulator).

We decided to set up most of our receiving chain in the laboratory in order to troubleshoot the Costas loop problem. The lab setup included the HP8672A uplink source, our Decoder Test Fixture as one data source, our noise generator, the NEC Simulator, our Downconverter (with an HP83620A for its LO), our Demodulator, and our (spare) Decoder. (This was a large and complex setup!) The main Station components not included were the cryogenic front end, the Ku LO, and the station computer. Under these conditions, with very high SNR into the Demodulator, some adjustments were made to the Costas loop's lock detector that allowed successful operation for most types of signal. We did discover, however, that transmitting digitized noise in (2,2,32) mode resulted in marginal performance of the Costas loop; other modes were satisfactory. It is possible that the noise level we were providing to the Simulator was too low, resulting in long runs of zeros or ones. However, use of pseudo-random noise from the NRAO Test Fixture produced reliable lock over a dynamic range of more than 20 dB.

[Note that our Costas loop is a.c. coupled, and therefore it cannot lock on an unmodulated signal, nor to one where most of the modulation energy is below a few MHz. Also, note that our IF chain contains no AGC (but we do have computer-controlled gain adjustment with 2 dB resolution), so the Costas loop is required to operate over a significant range of signal levels.]

Since we had the Decoder available in the lab setup, we decided to investigate the frame sync. Again, reliable sync occurred with the NRAO headers but not with the NEC headers. Analysis showed that the Decoder was assuming that each byte of the header was sent

LSB first, whereas it is really sent MSB first. (In my opinion, the VSOP documentation [3] is ambiguous on this point.) The sync code was quickly corrected by changing its binary definition in the Decoder, allowing perfect frame sync to be obtained. The remaining bytes of the header were corrected by a firmware change in the Decoder. The NRAO Test Fixture was then made consistent with this new format by revising its firmware.

Downlink spectra measured at IF following our Downconverter are shown in Figures 6a (with PRN from the NRAO Test Fixture) and 6b (with 2-bit digitized noise from the Simulator). The former spectrum is conforms closely to theory.

Everything was then re-installed at the antenna and the radiatively-coupled test was repeated, this time with good success. We obtained reasonable spectra at our 600 MHz IF (Figure 6c) and verified that we had good signal-to-noise ratio and no saturation of the receiving chain. The 1 to 2 dB ripple that is observable in the spectrum is probably due to multipath in the very compact, near-field arrangement. We briefly rearranged the Simulator's RF connections to those of Figure 2b, so that the modulated downlink would pass through the diplexing filter, resulting in the spectrum of Figure 6d; note that the outer lobes are truncated. We did a quick check to see that the link performance was essentially unchanged, but all the detailed tests were done with the (less realistic) setup of Figure 2a.

The Demodulator locked very reliably and the Decoder achieved essentially perfect frame sync, with no resyncs observed over periods the order of one hour, in spite of a rather high rate of random bit errors. The measured signal level range over which the Demodulator would acquire both carrier and clock lock is shown below.

Signal source c,b,r	Dncvtr IF Attn Set Min	Max	Dynamic Range
Simulator (2,2,32)	-26dB	-22dB	4 dB
Simulator (2,1,64)	-26	0	>26
NRAO Test Fixture	-26	0	>26

With the Simulator as data source, our external broadband noise was being digitized in the selected mode. It is possible that the noise level was not correct. Clearly the Demodulator had difficulty with the 2-bit digitization mode; this would be explained if the data consisted of mostly zeros or mostly ones, but we did not attempt to check this directly.

3.3 Header processing software tests

The Decoder collects all header bits from each frame, and its firmware then processes them to eliminate redundant data and to filter out random errors before passing the results to the station computer for higher-level interpretation. Basically, the pattern of 25 repeats of 16 header types is decoded and each information byte is considered good if there are at least 10 exact agreements among the 25 repeats. The station computer can then convert the data to convenient units, average the total power measurements, display the results, and write selected data to the log at intervals appropriate to each datum. For details of this processing, see [4].

The low-level processing was checked first. Although not every detail could be conveniently checked, it all appeared to be performing correctly. Using the Simulator's ROM data, the format sequence was correctly filtered. This required that the error correction code in W4 be properly decoded, else the repeat sequence could not have been recognized. The Decoder firmware detects and reports groups of headers with more or fewer than 16 repeat blocks, as is expected occasionally because the data generation clock and the

downlink clock are not coherent (see [3], page 5, Note 2). Indeed, it was observed that a "short group" occurred every 10-20 minutes.

Higher level software was checked with reference to the listings of the ROM data given in [1]. There are 23 different sets of header data, each repeated either 32 times (taking 64 sec) or 64 times before going to the next one. With some secondary repeat cycles, the whole ROM lasts 4096 sec (1h08m20s). We did two kinds of checks: we used operator display software to give decoded and labeled displays of the data that could be manually checked on-the-fly against the listings; and we recorded all the data in the log every 15 sec for later study. The displays included such things as temperatures in K or C, LO frequencies in MHz, noise diode state, subsystem power states, etc. With few exceptions, everything that we checked was correct. In fact, during this test Takahashi-san discovered (from more detailed hexidecimal listings that he had in his laptop PC) that the ROM contains some data glitches at certain points; we actually observed some of these. Study of the recorded data is not complete as of this writing; a brief examination showed that most of the data makes sense, but there may be a few discrepancies that are not yet explained.

3.4 Bit error rate test

The NRAO Test Fixture includes the ability to check the data bits of each frame by connecting it to the Decoder outputs (which normally go to the Formatter of the VLBA recording system). For our internal tests, the Test Fixture is normally located adjacent to the Decoder and Formatter, but in the present setup they were about 30 m apart (see Figure 1a). This required a long cable carrying the eight 8 Mb/s data signals and the 32 MHz and 1 Hz clocks on differential lines. Integrity of the cable was separately verified before these tests. A limitation of this feature of the Test Fixture is that it can be connected to only half of the data at a time (signals from either I or Q), and the error rate counter can observe only one of the eight signals at a time (although it is multiplexed among all eight in firmware). Nevertheless, meaningful bit error rate measurements can be made.

Tests were made using the I channel signals at three SNRs, obtained by inserting attenuators at the Simulator's RF output (KMOD-2 port). In each case, signal and noise powers were measured at IF using a power meter preceded by a 600MHz/50MHz bandpass filter. Since the filter bandwidth is less than the modulation bandwidth, the signal was measured with modulation off (carrier only), assuming that the modulation does not significantly change the total power. The raw data and computed results are shown in Table 1. These results are

Table 1: BIT ERROR RATE TEST RESULTS

RF Attn	IF Attn	Signal	Noise	Eb/N0	Time	Bits	Errors	BER
0 dB	20dB	-22.1dBm	-61.9dBm	+35.7dB	64s	5.12e8	271	6e-8
10	10	-20.6	-50.5	25.8	10	8.00e7	6608	8e-5
20	0	-20.7	-40.4	15.6	10	8.00e7	10800	1.3e-4

relatively poor, considering that the theoretical BER at Eb/N0=15.6dB is less than 1e-7. The difference is believed to be due to details of Demodulator optimization, and this is now under investigation.

3.5 Two-way phase lock test

Near the end of the available testing period, the RF connections to the Simulator were altered to those of Figure 2c,

allowing two-way communication with the Earth Station at appropriate signal levels. The Simulator locked without difficulty to the radiated uplink signal, and the Costas loop, clock loop, and frame synchronization on the downlink side continued to perform as before. The uplink fine tuning synthesizer (DDS) was then varied in frequency from -700 kHz to +700 kHz relative to the nominal 15.3 GHz to check the lock acquisition range. (The Simulator's specification is +-460-kHz, which is the maximum Doppler range.) Results are shown in Table 2. The Costas loop tuning (range 1 to 4 volts) followed the frequency as expected, and the Simulator maintained lock from -700 kHz to at least +420 kHz. At the frequency extremes, the uplink was turned off and back on to verify lock acquisition.

Table 2: TWO-WAY LOCK TEST

DDS1 Freq MHz	Offset kHz	Costas Loop Integrator	Monitors LockDet	Notes
28.5714286	0			15.30... GHz
28.5704286	-7	2.085v	2.578v	
28.4714286	-700	1.040		All still locked
28.5814286	+70	2.197		
28.6014286	+210	2.407	2.64	
28.6214286	+350	2.617		
28.6314286	+420	2.720		
28.6714286	+700			Simulator out of lock

With two-way lock established, the next logical test would have been to measure the residual phase error on the recovered downlink carrier. Unfortunately, a last-minute failure of the phase detector in the Two Way Timing Control Module precluded this test. (It had been working a week earlier. Two weeks later, the failure was traced to one bad chip, an operational amplifier; upon replacing it, proper operation was restored.)

4. DISCUSSION

From the NRAO's viewpoint, the tests were largely successful and were certainly extremely valuable. I believe that ISAS and NEC also consider the exercise mostly successful and worthwhile.

Correction of the BER problem will require a substantial effort, but we do not believe that there is any fundamental problem that will cause a major re-design. Instead, precise adjustments of the Demodulator circuitry (including bit capture timing, matched filter parameters, quadrature accuracy, and perhaps other parameters) are expected to result in the required improvement. We have been somewhat hampered by not having a high-quality test modulator that is known to provide signals that would achieve near-theoretical performance with an ideal demodulator; we will work on this too.

Detailed tests of the two-way timing stability are still needed internally, using our own Satellite Simulator, although we would like to have tried it with the Japanese Simulator.

We would like to try these compatibility tests again after improving our equipment, but well before launch. We understand that scheduling use of the Simulator for another test is difficult for ISAS and NEC because of requirements in Japan, but we hope that an appropriate time can be found.

5. ACKNOWLEDGMENTS

No positive results at all would have been possible from these tests without the dedicated work of the Green Bank project team over the preceding few months, and indeed throughout the project. Special thanks are due to Dave Burgess, Ray Escoffier, Glen Langston, Bill Shillue, and Dick Thompson for long hours of hard work immediately before and during the tests. Bill and Dick came to Green Bank to help on very short notice. Also, Richard Bradley of the Central Development Lab spent a day helping to resolve some receiver problems a few days before the tests.

Of course, the tests could not have been done without Takahashi-san and Yamamoto-san, who supplied not only their simulator (which proved to be of very high quality) but expertise in its operation and much useful advise.

We received a lot of help from the Green Bank shops in preparing for these tests. The support and encouragement of Mike Balister and Bob Brown are also appreciated.

REFERENCES

[1] NEC, "Muses-B Observation Subsystem Simulator: Guide Book" (undated).

[2] R. Escoffier, "The OVLBI Decoder Test Fixture." OVLBI-ES Memo, October 1994, to be published.

[3] ISAS, "Muses-B Ku-band Telemetry Format." Document VSOP-5130, Revision 5, 9/12/94.

[4] L. D'Addario, "VSOP Header Processing Design Document," 94/08/14. Available by anonymous ftp from ftp.gb.nrao.edu in directory ./ovlbi/doc.

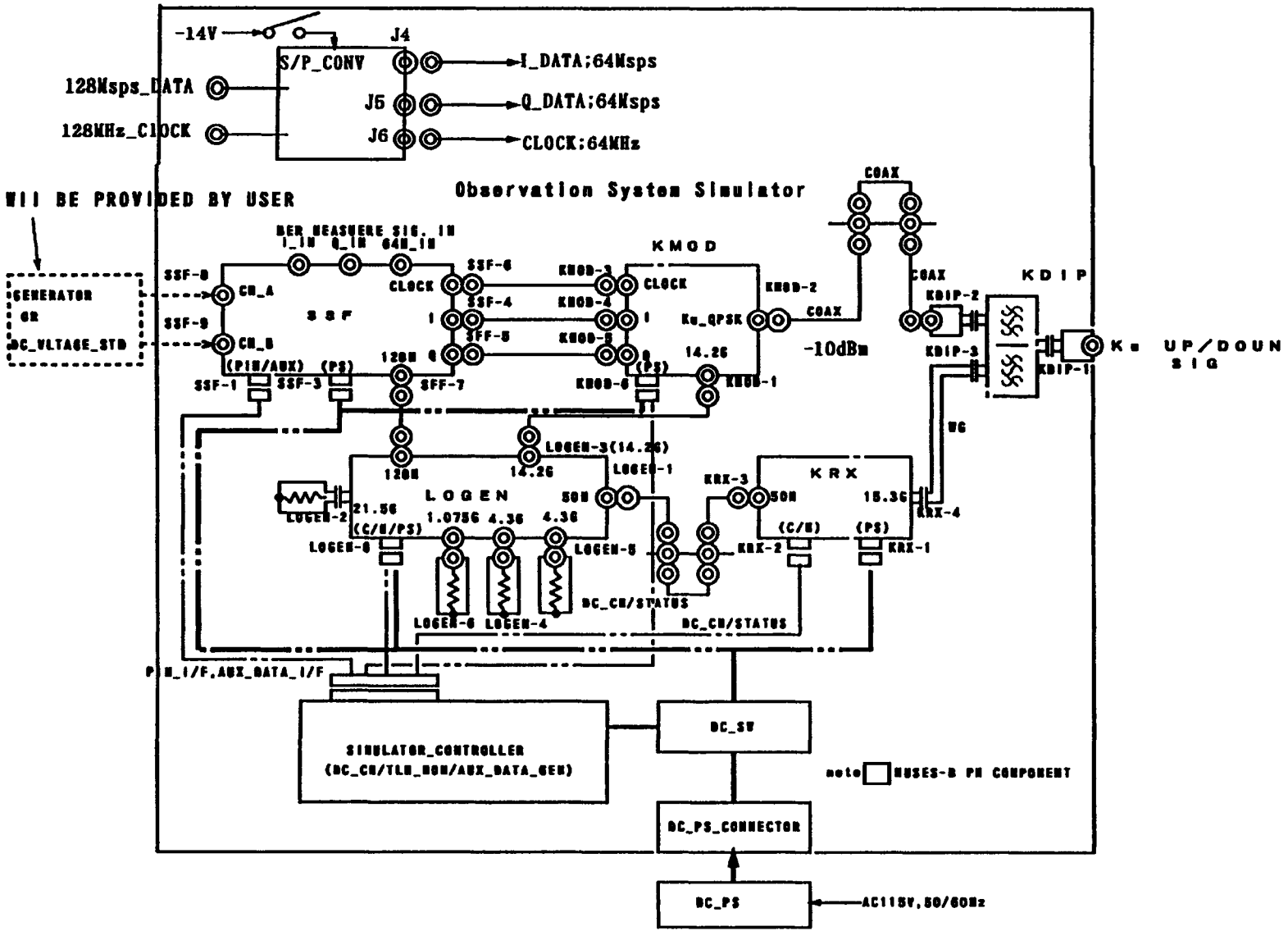
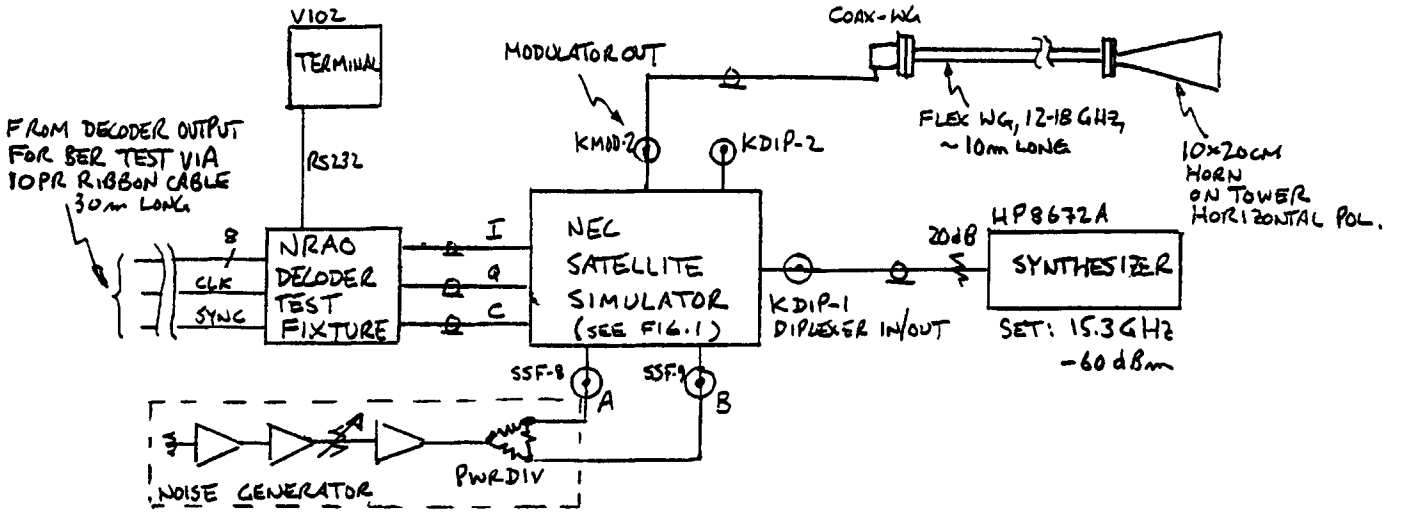
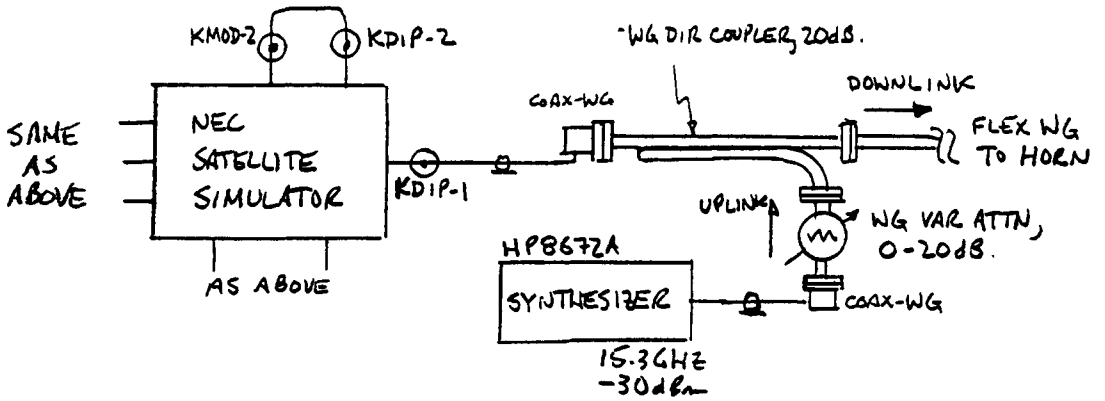


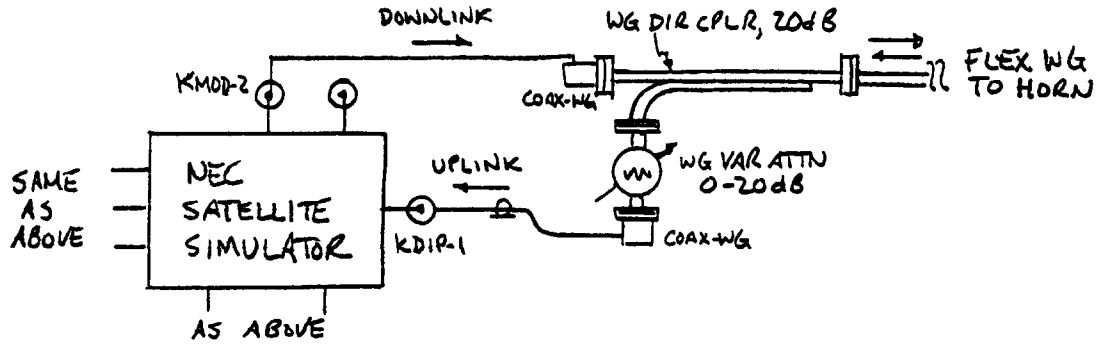
Figure 1 OBSERVATION SYSTEM SIMULATOR BLOCKDIAGRAM



a. Setup used for most of the tests. Uplink from synthesizer, downlink from 14.2 GHz modulator, bypassing the diplexer.

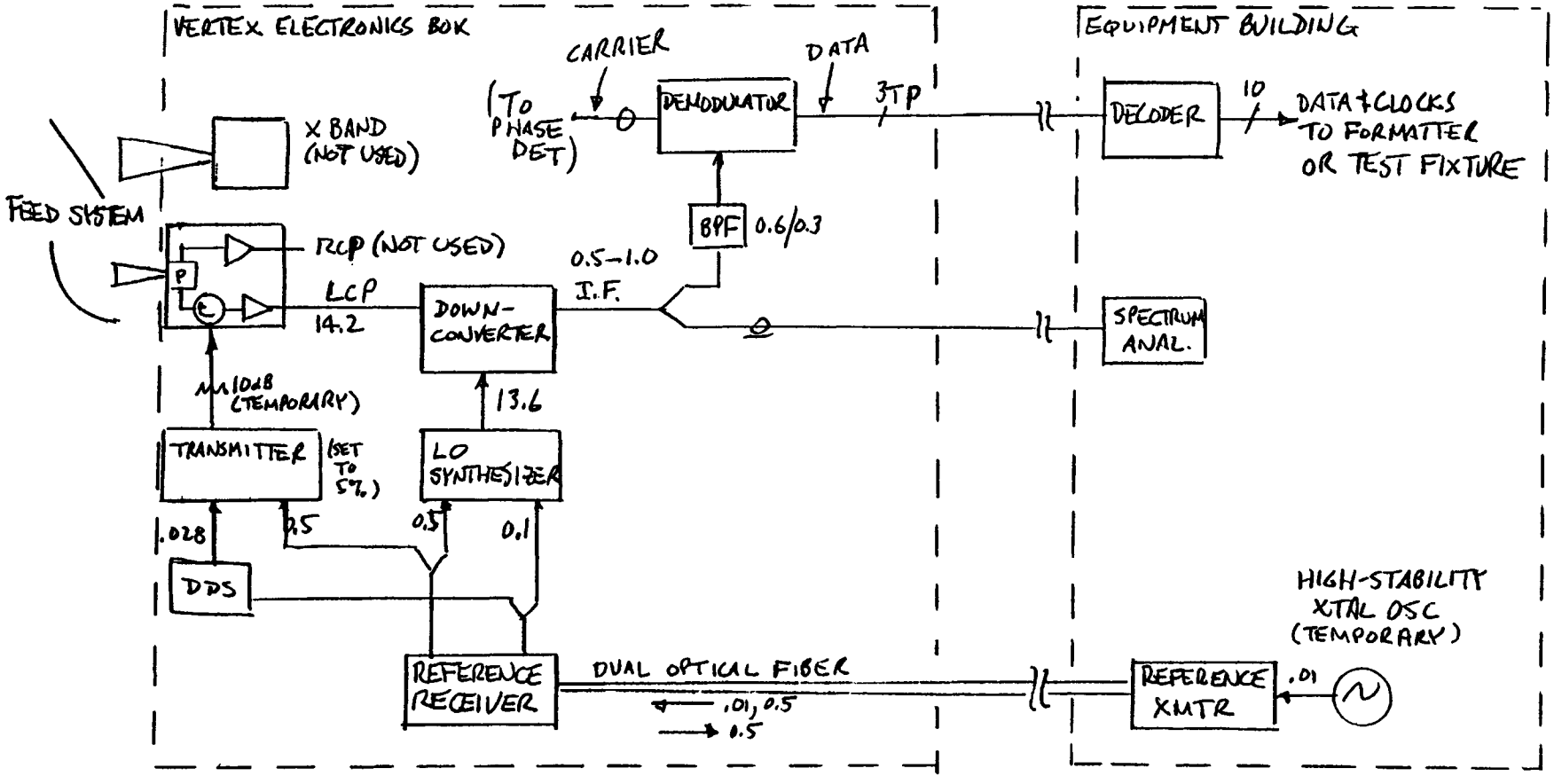


b. Setup used to check performance when the downlink is filtered by the diplexer.



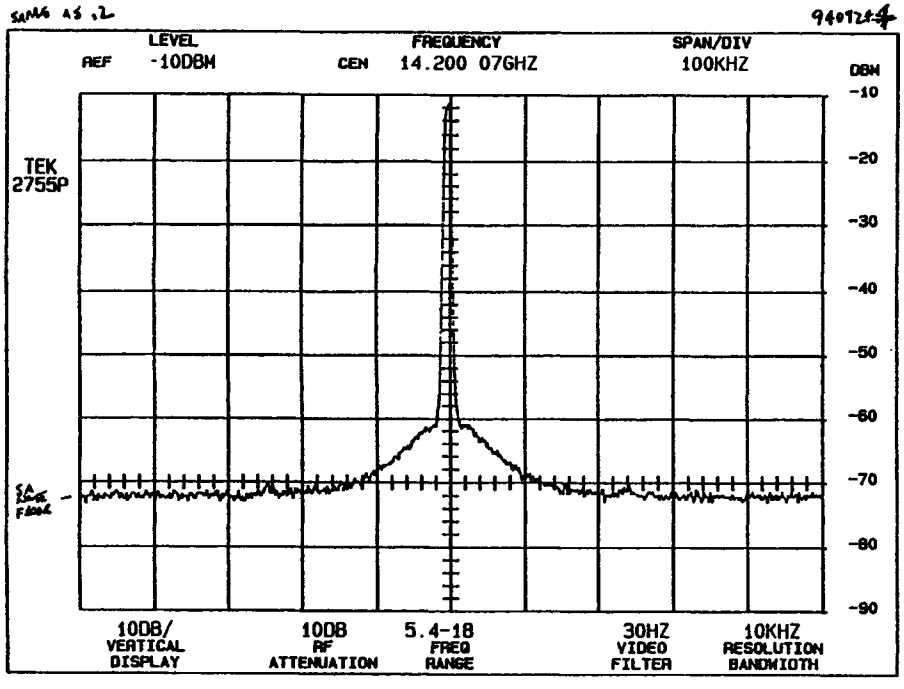
c. Setup used for two-way phase lock tests; uplink from Earth Station transmitter.

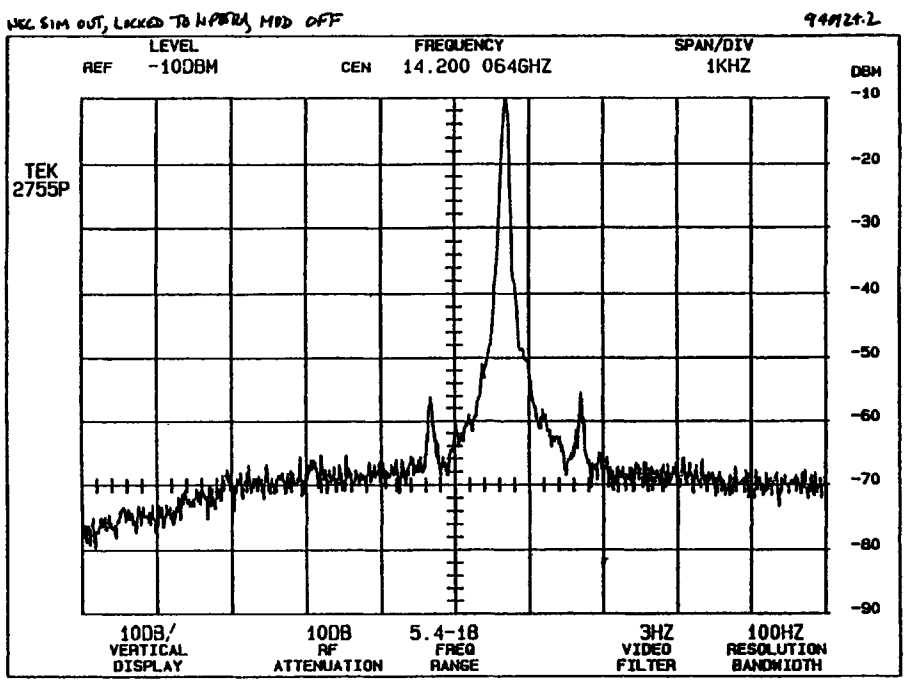
Fig. 2: Setups of satellite simulation equipment for tests conducted at the Earth Station. All of this hardware, along with various test instruments, was located in a temporary shed 30m from the center of the 14m antenna. The horn was mounted 6m above ground on a tower.



NUMBERS ARE FREQ IN GHz USED IN THESE TESTS.

Fig. 3: Simplified block diagram of the portion of the Earth Station electronics that was involved in these tests.





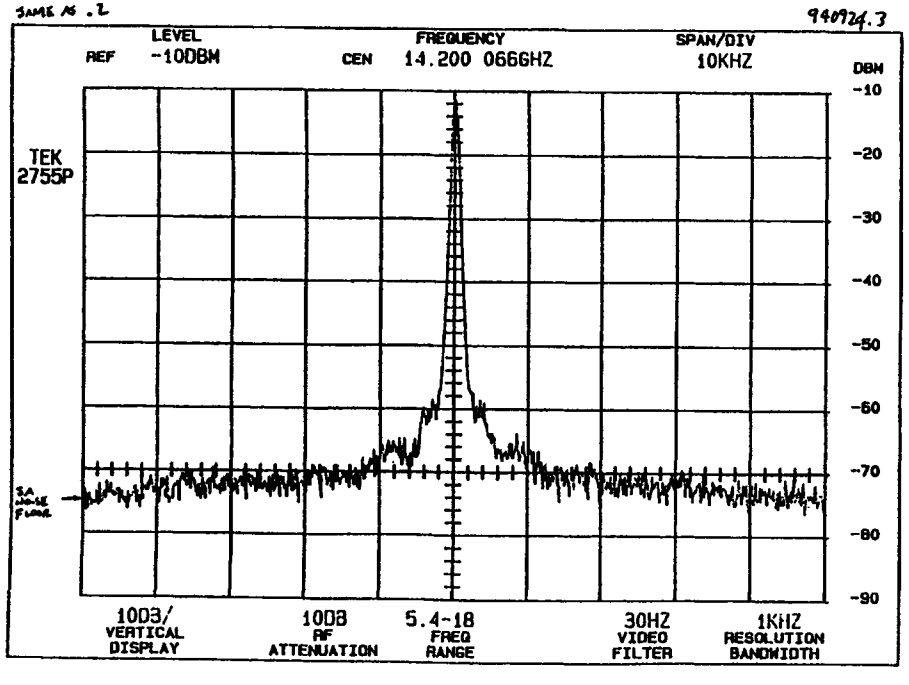
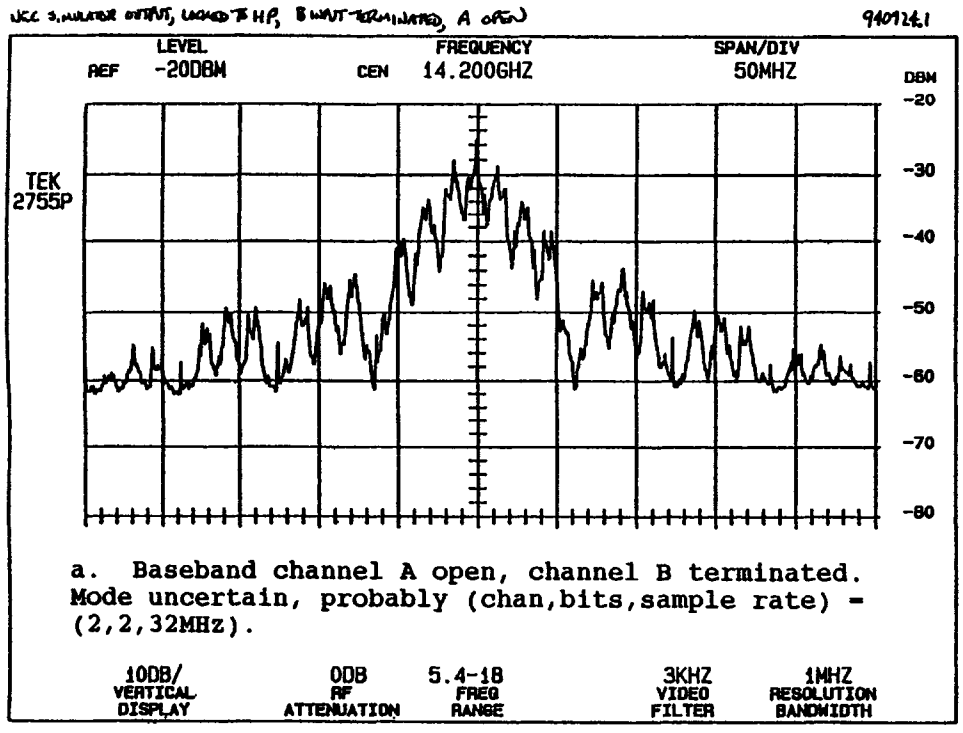
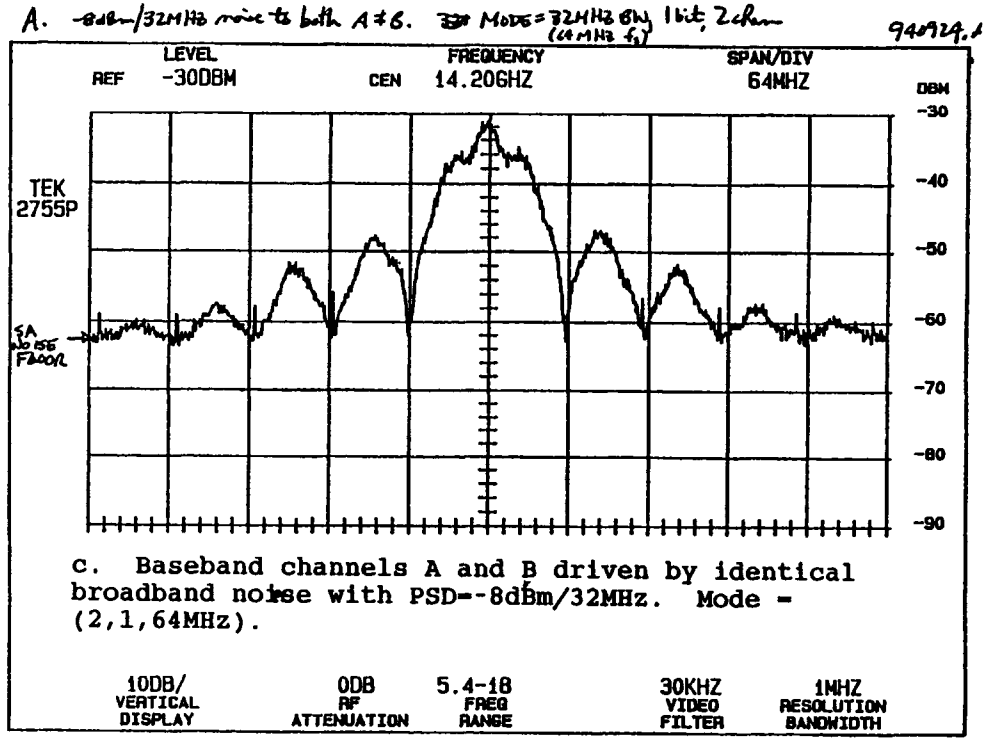


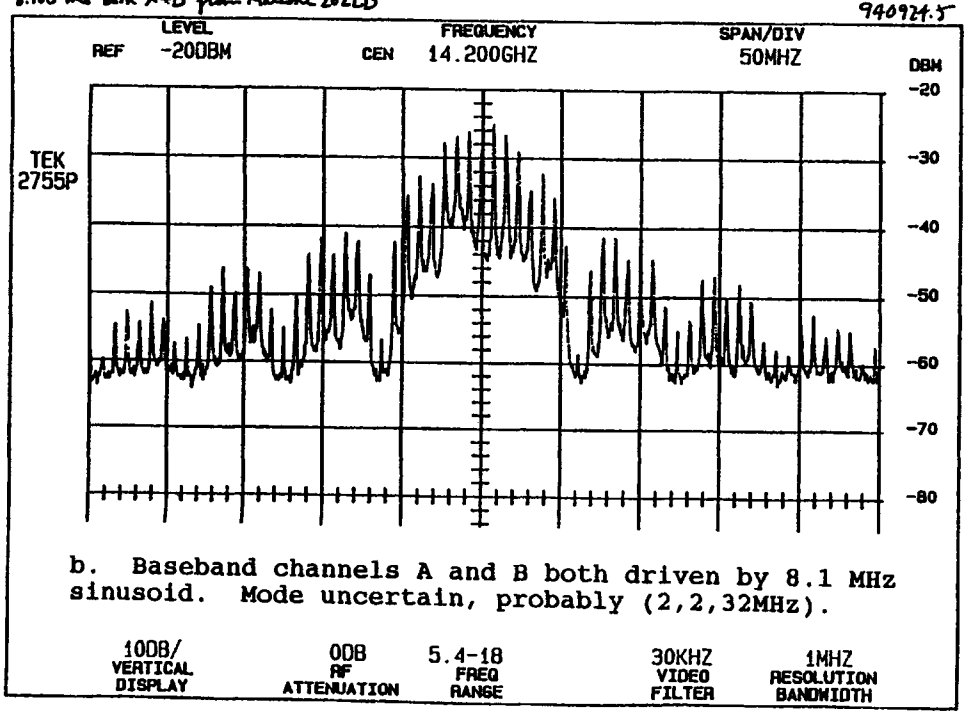
Fig. 4: Spectra of NEC Simulator's downlink output at port KMOD-2, with modulation off. Taken in lab while locked to HP8672A synthesizer. Plots are of the same signal at three different resolutions.



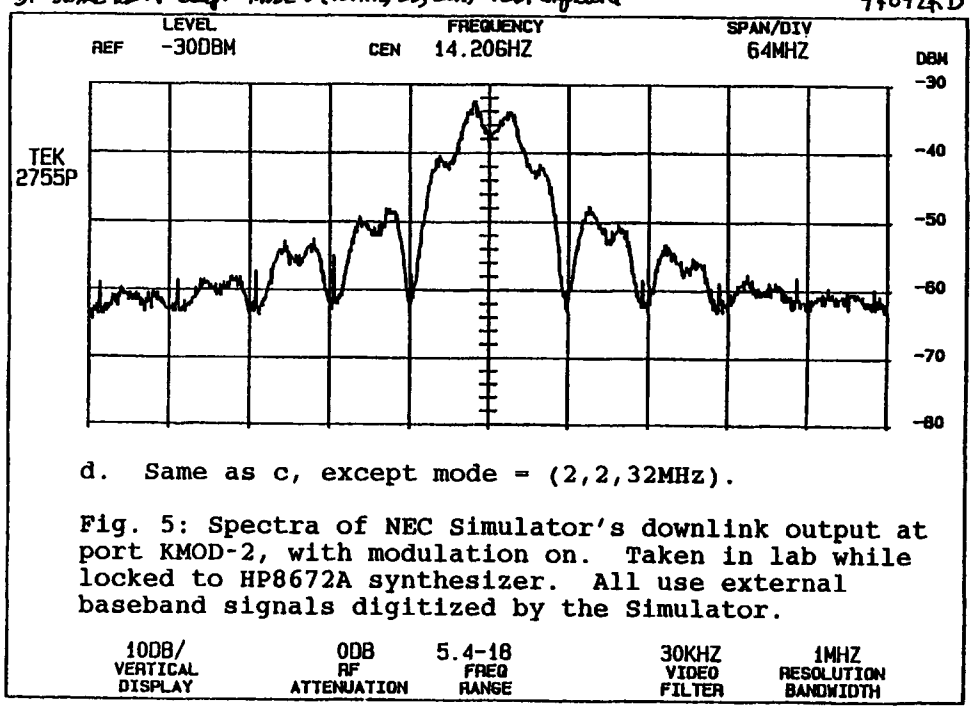
a. Baseband channel A open, channel B terminated. Mode uncertain, probably (chan,bits,sample rate) = (2,2,32MHz).



c. Baseband channels A and B driven by identical broadband noise with PSD=-8dBm/32MHz. Mode = (2,1,64MHz).

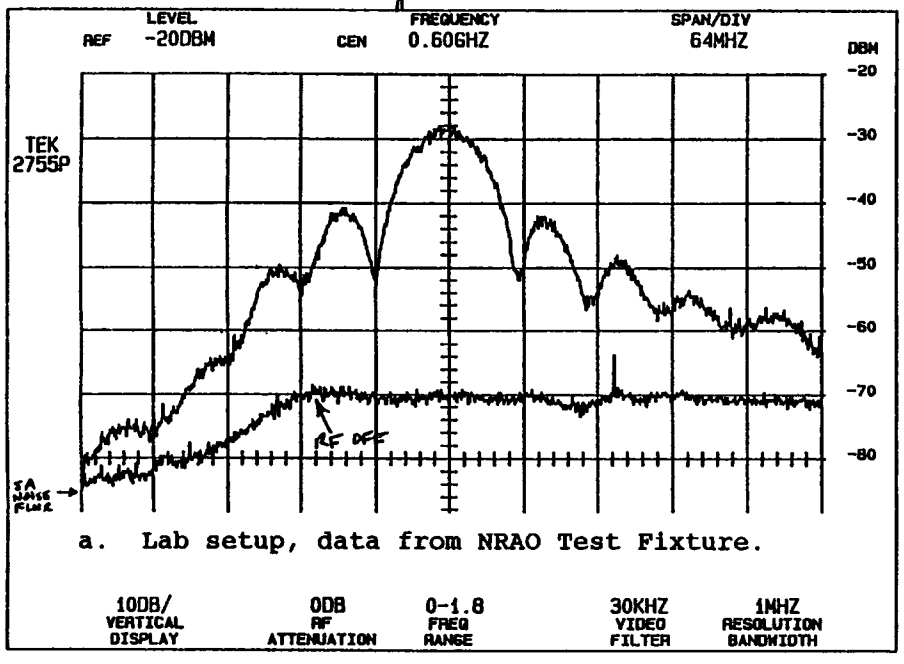


b. Baseband channels A and B both driven by 8.1 MHz sinusoid. Mode uncertain, probably (2,2,32MHz).

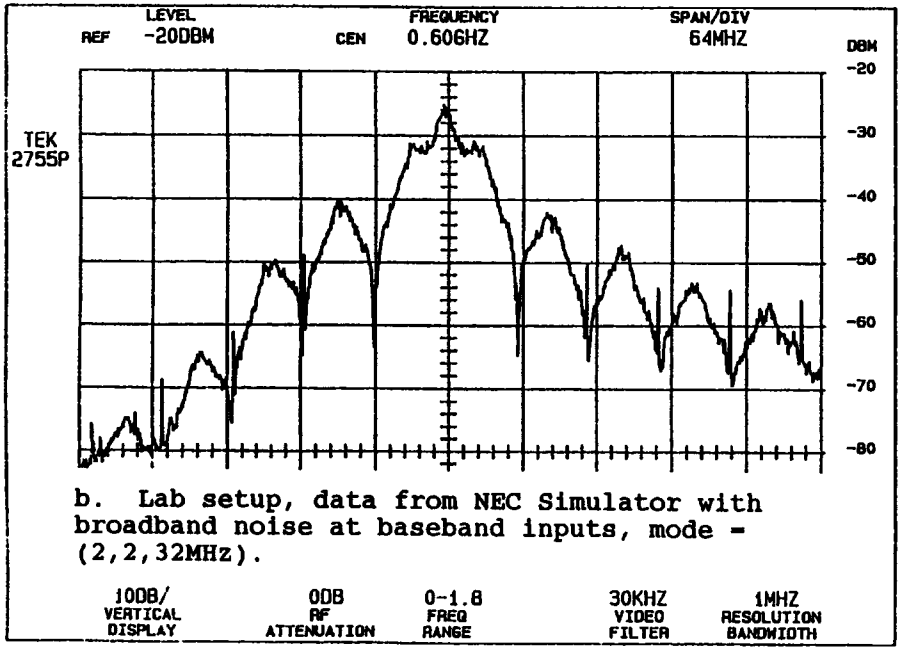


d. Same as c, except mode = (2,2,32MHz).

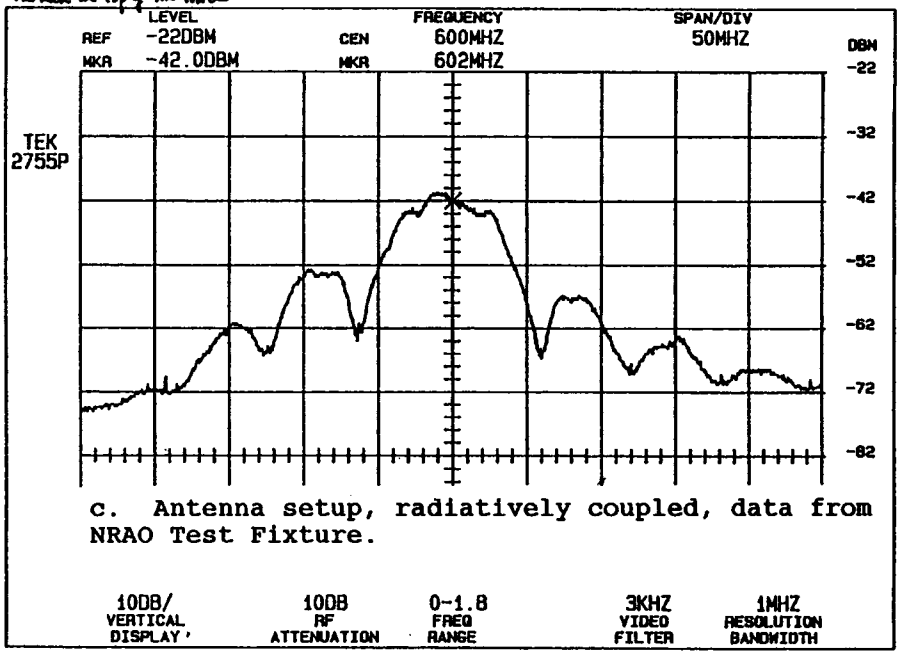
Fig. 5: Spectra of NEC Simulator's downlink output at port KMOD-2, with modulation on. Taken in lab while locked to HP8672A synthesizer. All use external baseband signals digitized by the Simulator.



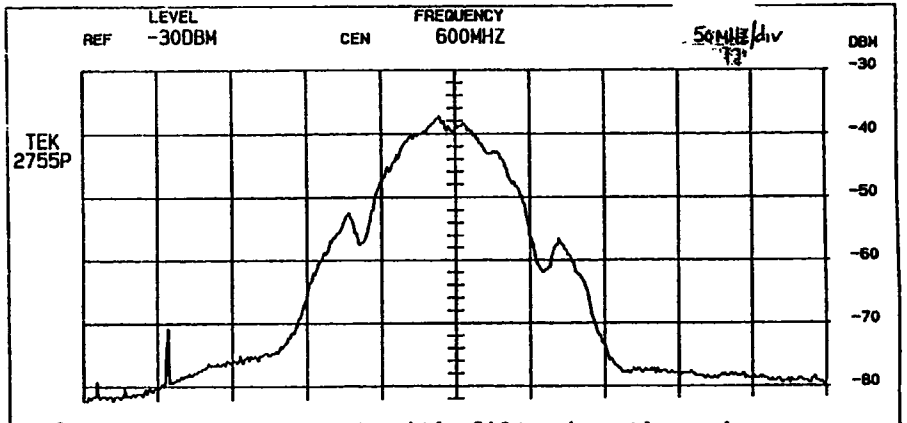
a. Lab setup, data from NRAO Test Fixture.



b. Lab setup, data from NEC Simulator with broadband noise at baseband inputs, mode = (2,2,32MHz).



c. Antenna setup, radiatively coupled, data from NRAO Test Fixture.



d. Same as c except with filtering through diplexer, setup of Fig. 2b.

Fig. 6: Downlink spectra at IF after downconversion in the Earth Station's electronics. a,b: taken in lab with cable connections and HP synthesizer for the LO. c,c: taken at antenna with radiated connection and full Earth Station signal processing.