NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

Spectral Processor Memo No. 29

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To: E. Childers, M. Clark, R. Lacasse, D. Schiebel, R. Weimer, S. White

From: R. Fisher

Subject: Summary of discussion on digital interface and displays in the spectral processor IF drawers.

Communication between the spectral processor IF drawers and the rack controller will be via a 57 k-bit serial line using the VLBA serial interface card and through a spectral processor card that contains total power and IF synthesizer counters. From the point of view of the rack controller the serial line will be read/write, but the counter card will be read only except for a couple of control words.

The counter card expects two TTL pulse streams from each IF drawer. One will be from the frequency synthesizer that sets the center frequency of the IF passband. This frequency must be prescaled to roughly 4 MHz or less. The second will be a V/F conversion of the total power seen by the flash A/D convertors. This pulse frequency should be about 32 kHz when the total power is set for the largest usable input level to the flash A/D's.

Each IF drawer will have one VLBA serial interface card and the eight cards will be daisey chained on the serial line. These cards convert to or from a serial data stream from or to a bus with 16 data bits and 6 address bits with handshaking. Also, these cards provide conversion of 16 analog channels to serial digital information. Each card has its own address, and up to 64 devices can be addressed on each card bus. IF drawer functions to be put on the serial card are as follows:

Read by rack controller

- Synthesizer lock indicator bit
- Total power overload bit

Written by rack controller

- Bandwidth selection (10 choices)
- Attenuator setting (0-63 dB in 1 dB steps)
- Upper/Lower sideband selection
- Intermod. filter in/out selection
- Synthesizer frequency
  - 5 digits of 9's complement BCD (XXX.XX MHz)
  - twice frequency value for 100-500 MHz output
  - actual frequency value for 500-660 MHz output

Synthesizer doubler bit (set for synthesizer freq. > 500 MHz)
RFI excision information
    Fast integrator time constant (9 settings, 1 us to 10 ms in 1, 3, 10 sequence)
    Slow integrator time constant (9 settings, 100 us to 1 sec in 1, 3, 10 sequence)
    Clipper level (8-bit D/A)
    Threshold level (at least 8-bit D/A)

The exact format of the above data depends on the most convenient hardware implementation. Conversion to 9's complement BCD will be done in software. Settings do not need to be read back to the rack controller.

Some display of IF drawer settings is required on the front panel of each drawer. The exact format is not critical so long as the observer can confirm that his/her requests were acted upon correctly and engineers and programmers get sufficient feedback for troubleshooting. The following formats are suggested:

Total power overload..... 1 or 2 LED's
Synthesizer lock......... 1 LED
Intermod. filter in/out.. 1 LED
Sideband selection....... 1 LED
Synthesizer doubler...... 1 LED
Bandwidth selection...... 10 LED's or 1 Hex digit
Attenuator setting....... 2 Hex digits
Fast integ. time const... 1 Hex digit
Slow integ. time const... 1 Hex digit
Clipper level............ 2 Hex digits
Threshold level.......... 2 or 3 Hex digits
Synthesizer frequency.... 5 Hex digits (9's complement format)
Noise power level........ small analog meter

The Hex digit displays may be combined into one 5-digit display with a selector switch if more convenient.

A noise generator for testing will be incorporated into the IF signal distribution module to be constructed by Bill Albing.

The detailed data format for the IF drawer functions above will be specified by Steve White by the end of February, and someone in the digital group will design the circuitry associated with the serial data card.