NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

Spectral Processor Memo No. 32

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To: Spectral Processor Group
and Mailing List

From: R. Lacasse

Subj: **More Accumulator Control Bits**

Introduction:

Several control bits were inadverdently left out of memo 31. They are described herein.

What needs to be controlled:

This section describes control bits which were not listed in memo 31.

ITEM	DESCRIPTION
MYCYCERR-	When low enables the insertion of error data in the frames sent to the Masscomp every M data cycles as described in Appendix B of memo 31.
RFIMASK<0:7>	Used to individually mask RFI flags from the IF converters. Bit positions 0 to 7 correspond to IF's 1 to 8. A high in a bit position masks the RFI flag, i.e., RFI blanking is disabled for that IF.
RFIBUFS0 RFIBUFS1	Used to specify the coarse delay of RFI flags. Details may be found in Appendix A.
TGBUFS0 TGBUFS1	Used to specify the coarse delay of Timing Generator Data. Details may be found in Appendix B.

How to Access Bits:

LOCATION	CONTROL BITS
CONREG0 4	TGBUFS0
CONREG0 5	TGBUFS1
CONREG0 6	RFIBUFS0
CONREG0 7	RFIBUFS1
CONREG0 8	MCYCERR-
CONREG1 <8:15>	RFIMASK<0:7>

APPENDIX A

On the Delay of RFI Blanking Signals

The RFI blanking signals must be delayed by an amount equal to the pipeline delay to line them up in time with the transformed data. This is done in two stages. The first stage delays the blanking signals by 1, 2, 3, or 4 FFT cycles, accounting for most of the pipeline delay. The second stage aligns the signals with the FFT cycles as they arrive at the accumulator. The first stage consists of four registers which are clocked once per FFT cycle, in phase with the data acquisition by the flash ADC's. The second stage consists of one register which is also clocked once per FFT cycle, but in phase with data arriving at the accumulator.

To quantify the above, it is convenient to number the accumulator clock pulses, starting at the beginning of scan. This is depicted in the timing diagram of Figure A1. The signals of interest are C1.2XA+, C1XAA+, and SYNCA-. C1.2XA+ clocks the Square and Cross Multiplier and following stages (including the accumulator). C1XAA+ clocks the stages preceeding the Square and Cross Multiplier. In this diagram, the rate of C1.2XA+ is twice that of C1XAA+ (x2 clocking mode). This is only one of two possible cases; the other case is when the rate of C1.2XA+ equals that of C1XAA+ (x1 clocking mode). The SYNCA- signal goes low for one period of C1XAA+ to mark the beginning of scan. C1.2XA+ and C1XAA+ are both numbered starting at zero as shown in the diagram.

The first data point of an FFT cycle arrives at the accumulator at C1.2XA+ clock number

$$T_D = DP + Ni$$

where DP is the delay of the data pipeline measured in units of C1.2XA+ clocks,

N is

256 for 2/256 channesl with x1 accumulator clock,

512 for 2/256 channels with x2 accumulator clocks and all 1024 channel combinations with x1 accumulator clock,

1024 for all 1024 channel combinations with x2 accumulator clock, and

i = 0, 1, 2, ... to the end of scan.

The coarse delay registers for the RFI blanking signals are configured as follows:

RFI BLANKING SIGNALS --> REG 3 --> REG 2 --> REG 1 --> REG 0

i.e., REG3 feeds REG2, etc.

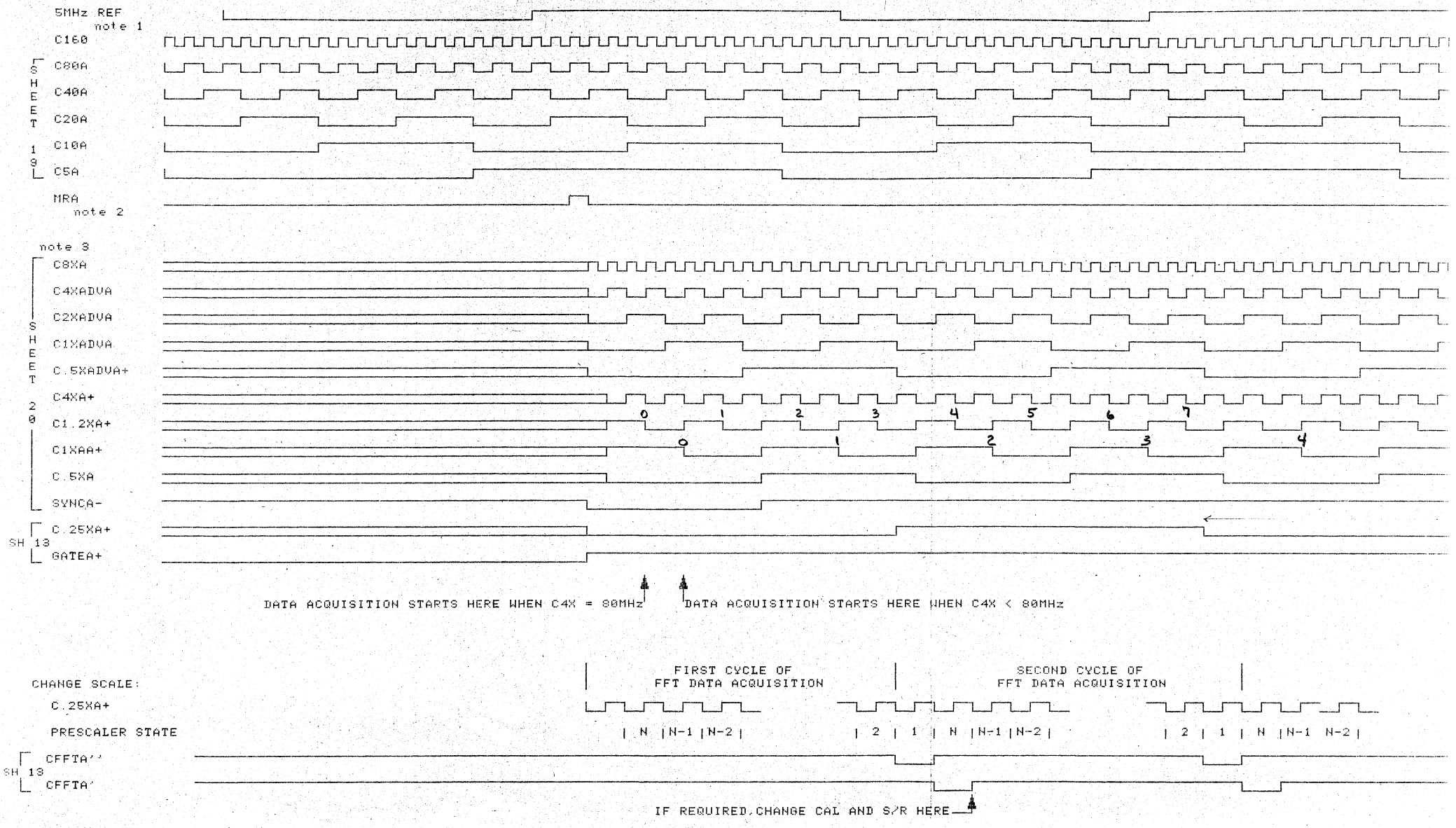

Figure A1: Timing diagram showing the numbering of C1.2XA+ and C1XAA+ clock pulses relative to the start of scan. A clock pulse is defined as the time between rising edges of the waveform. The "N" used above is not the same "N" used in the text.

The RFI blanking signals are in REG 3 during the following clock pulses:

$$N + Ni <= DR3 <= 2N - 1 + Ni,$$

in units of C1.2XA+ clocks.

The delay of signals in the other registers simply increases by N for each stage. In particular,

$$2N + Ni <= DR2 <= 3N - 1 + Ni,$$

$$3N + Ni <= DR1 <= 4N - 1 + Ni,$$

$$4N + Ni <= DR2 <= 5N - 1 + Ni.$$

The output of one of the above registers is sampled by the fine delay register at clock pulses

$$DRFI = DP - 6 + Ni.$$

(Six clock pulses are required due to pipelining in the accumulator itself.)

Specifying the coarse delay then amounts to specifying the coarse delay register which matches the data pipeline delay. In particular, select

REG3 if $N <= DP - 6 <= 2N - 1$

REG2 if $2N <= DP - 6 <= 3N - 1$

REG1 if $3N <= DP - 6 <= 4N - 1$

REG0 if $4N <= DP - 6 <= 5N - 1$

The desired register is selected with the two control bits, RFIBUFS1 and RFIBUFS0 as follows:

RFIBUFS1	RFIBUFS0	REG
0	0	0
0	1	1
1	0	2
1	1	3

As a means of visualizing this a graphic example is given in Figure A2.

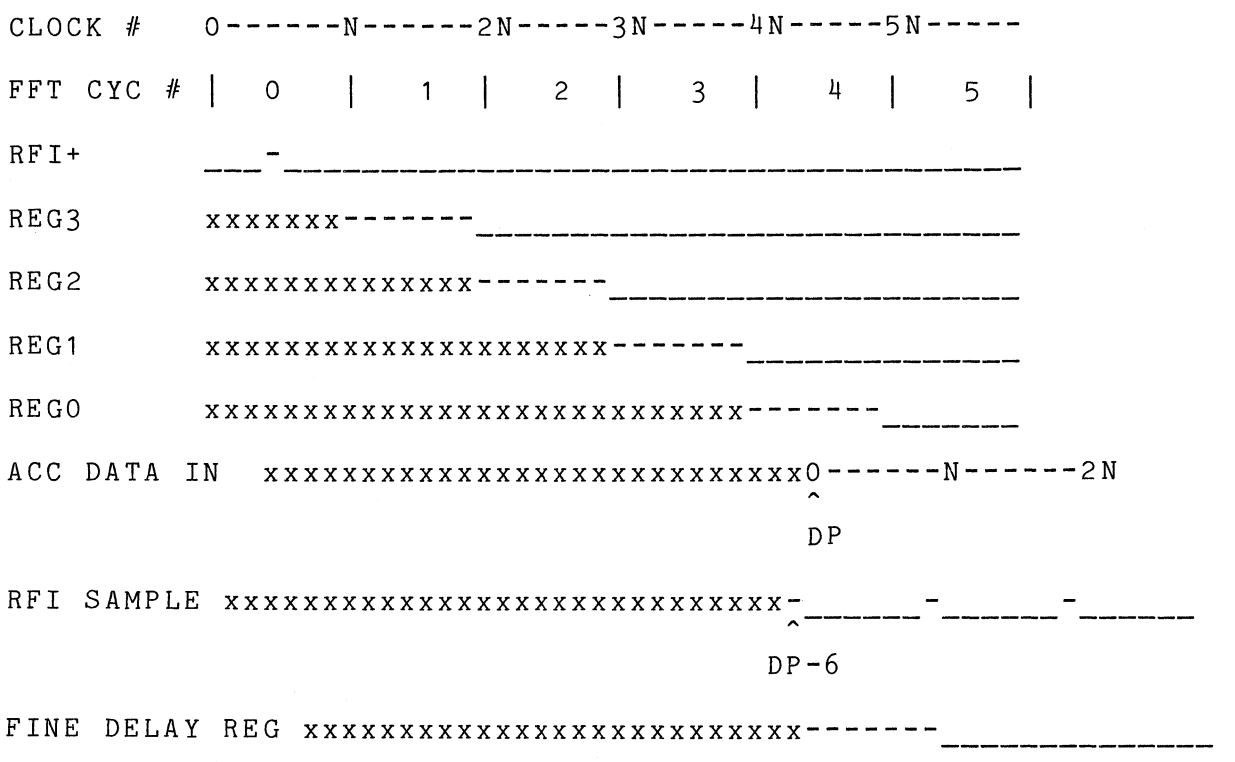

Figure A2: An example of RFI blanking signal delay. A burst of RFI is detected during FFT Cycle 0. It is captured and the blanking signal propagates through REG3, REG2, REG1, and REG0. With the pipeline delay shown, REG0 must be selected as the input to the FINE DELAY REG.

APPENDIX B

On the Delay of Timing Generator Bits

The delay of the timing generator bits is done similarly to that of the RFI blanking bits discussed in Appendix A. The discussion below assumes that the reader has read and understood Appendix A.

The Timing Generator Delay Registers contain the Timing Generator Data during the following clock pulses:

$$64 + Ni <= DR3 <= 64 + N - 1 + Ni,$$

$$64 + N + Ni <= DR3 <= 64 + 2N - 1 + Ni,$$

$$64 + 2N + Ni <= DR3 <= 64 + 3N - 1 + Ni,$$

$$64 + 3N + Ni <= DR3 <= 64 + 4N - 1 + Ni.$$

The output of one of the above registers is sampled by the fine delay register at clock pulses

$$DRFI = DP - 8 + Ni.$$

(Eight clock pulses are required due to pipelining in the accumulator itself.)

Specifying the coarse delay then amounts to specifying the coarse delay register which matches the data pipeline delay. In particular, select

$$REG3 \text{ if } 64 <= DP - 8 <= 64 + N - 1,$$

$$REG2 \text{ if } 64 + N <= DP - 8 <= 64 + 2N - 1,$$

$$REG1 \text{ if } 64 + 2N <= DP - 8 <= 64 + 3N - 1,$$

$$REG0 \text{ if } 64 + 3N <= DP - 8 <= 64 + 4N - 1.$$

The desired register is selected with the two control bits, TGBUFS1 and TGBUFS0 as follows:

TGBUFS1	TGBUFS0	REG
0	0	0
0	1	1
1	0	2
1	1	3