NATIONAL RADIO ASTRONOMY OBSERVATORY

VLA ELECTRONICS MEMO #103

September 22, 1972

Digital Delay System Investigation

A. M. Shalloway
Peter Camana

INTRODUCTION

An investigation and preliminary design work, including some prototyping has been done on a digital delay system for the VLA.

Specifications are:

Bandwidth = 100 MHz

Digital Bits = 2

Sensitivity relative to a continuous correlator = 0.81

Digital delay resolution = 10 ns. digital steps

Finer resolution obtained by phase shifting sampler aperture.

Switching Rate = 50 Hz

Dump Time Period-max. = 10 sec.

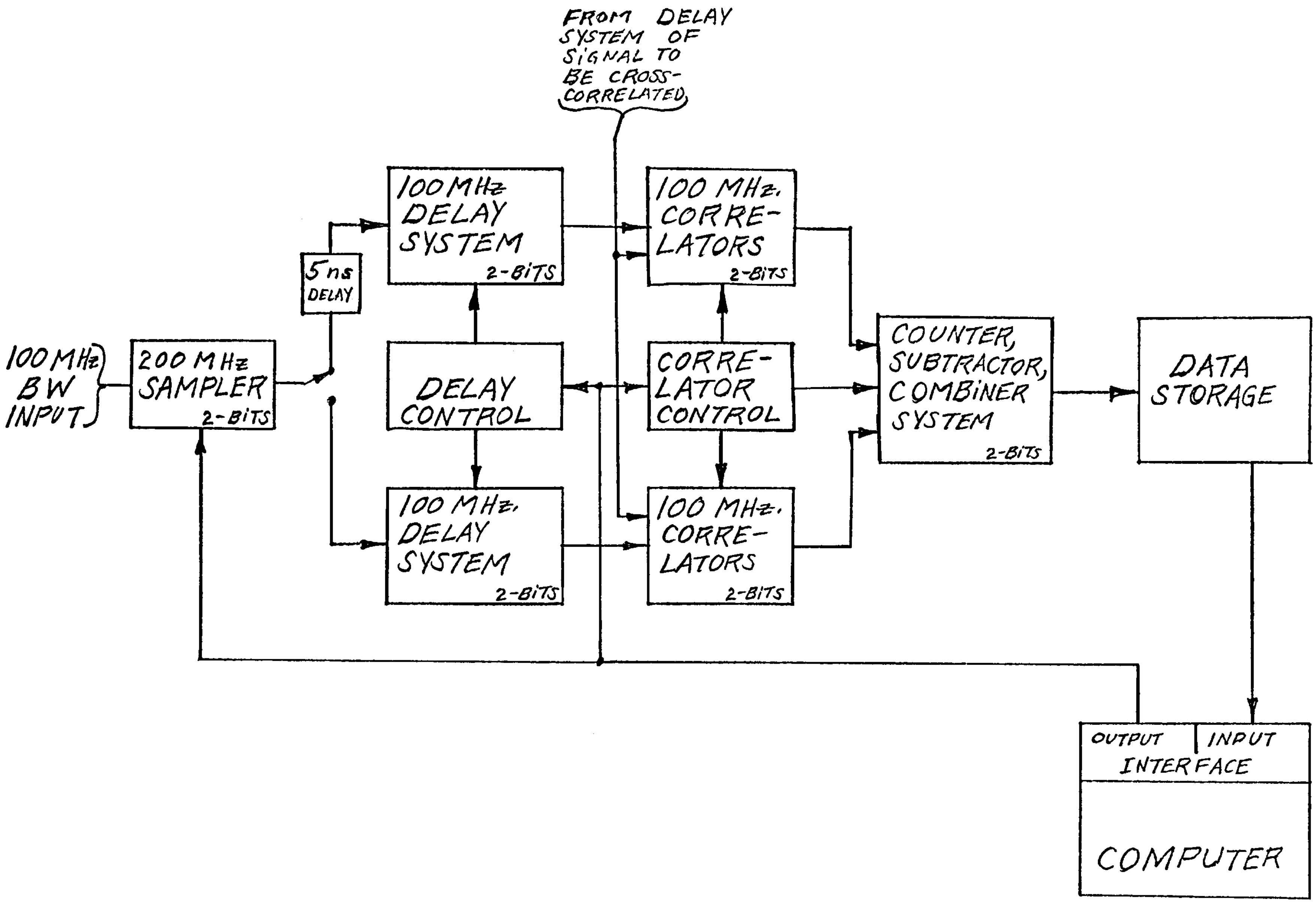
Racks = 15 to 20

Power (including power supply efficiency) ≅ 45 KW

A block diagram of the system is shown in Figure 1.

DELAY SYSTEM

The 100 MHz bandwidth signal is levelled, sampled at a 200 MHz sampling rate and its output is alternately strobed into one of two flip flops. The data is shifted into two parallel delay systems at 100 MHz and correlators reconstruct the alternating signals. This means that a 100 MHz B.W. signal is



9/20/72

FIG. 1 BLOCK DIAGRAM—DIGITAL DELAY SYSTEM VLA fed into the sampler and that one controller drives four delay systems (one for each of two (2) bits on each of the alternate samples).

The basic operation of the delay system is to store the sampled signal in the Random Access Memories until the computer given delay is reached. The data is then transferred from the RAMS into the output parallel to serial shift register.

The data is clocked into the 16 bit input shift register at the clock frequency of 100 MHz. The 16 bits are then strobed into the input latches. The contents at the address in the RAMS is read into the output latch and the contents of the input latches are written into the RAMS, the ADDRESS is then incremented by one. The data in the output latches is strobed into the output shift register at a variable time during the 160 ns cycle of the memory to give the final resolution of 10 ns. The clock then shifts the data out of the output shift register at the 100 MHz rate. Once the address counter reaches the number given by the computer the counter is reset to zero and the cycle starts again.

Figure 2 illustrates the delay system.

CORRELATORS

For each cross correlation we must produce one center cross correlation channel plus the channel before and after the center channel. The center channel and the difference between the other two channels provides all of the necessary information. Because the 200 MHz samples are being processed as alternate groups of data, the correlator starts out with a design of two sets of three two-bit channels (a total of twelve counters) which get combined

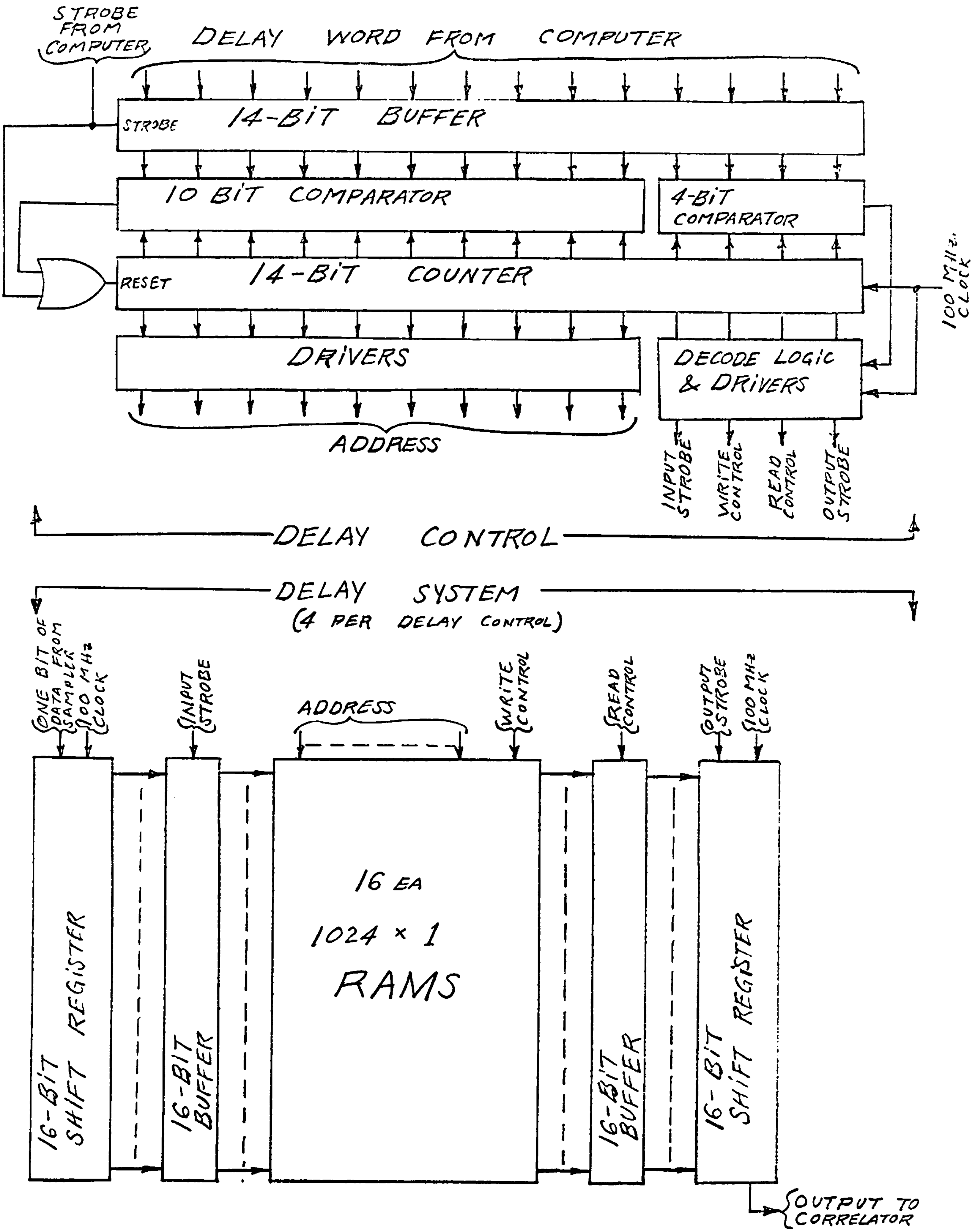


FIG. 2

DIGITAL DELAY SYSTEM VLA

DELAY

9-20-72
aml

eventually and emerge as two numbers (channels). One number represents the center channel, the other number represents the difference between the two channels adjacent to the center channel.

For details on signal to noise sensitivities and sample levels in the following discussion, reference should be made to:

Australian Journal of Physics; Correlators with Two-Bit Quantization by B. F. C. Cooper; 1970, 23, p. 521-7.

The design proposed is based on a two-bit correlator with the low and intermediate products deleted and n=2 (see reference above). This provides a Relative Sensitivity of 0.81 as compared to 0.88 for the best two bit combination of products and n values. An infinite bit correlator would give a sensitivity of 1.0.

For each correlator (cross correlation of two antennas, one polarization per antenna) we will provide three (3) channels; a center channel and one channel on each side of the center channel.

DATA DEFINITIONS:

Receiver A data (stored data) = XYZ

where: X=A for receiver A

Y=A for amplitude bit

=S for sign bit

Z=1,2,3, etc. for channel number

Receiver B data (non-stored data)=MN

where: M=B for receiver B

N=A for amplitude bit

=S for sign bit

The only four product combinations we have to consider are when XYZ=$\pm$ 1 and MN=$\pm$ 1. In these two equations we arrive at a definition for "1" as follows:

Four states can exist for the sampled data:

	↕ State 2
$+V_o$ volts	↕ State 1
0 volts	↕ State 3
$-V_o$ volts	↕ State 4

$0 < \text{State 1} < +V_o$ volts V_o volts $< \text{State 2}$

$0 > \text{State 3} > -V_o$ volts $-V_o$ volts $> \text{State 4}$

If we say that in these four states we can have $\pm$ 1 and $\pm$ 2 we have; State 1=+1, State 2=+2, State 3=-1 and State 4=-2. As discussed in the above reference, we could assign other values to replace $\pm$2 (n in the reference) i.e., $\pm$3, $\pm$4, etc., but little is lost by using 2 except that the accuracy of the sampler should be more precise. However, the value of 2 simplifies the digital logic considerably. Using these relations, deleting the low and intermediate products (i.e., set them equal to zero) and converting values so that we may apply the data in a binary digital system, we set the results of a correlation (multiplication) as per the following identities:

+1=0, -1=0, +2=0, -2=0, +4=+1, and -4=-1

As an example:

Ex. 1. (+2)x(+2) = +4 but by the above identities +4=+1

$\therefore$(+2)x(+2) = +1

Ex. 2. (+2)x(+1) = +2 but by the above identities +2=0

$\therefore$(+2)x(+1) = 0

The above identities would be obtained if the output of the samplers was as follows for the four different sampled states:

State 1 = 0

State 2 = +1

State 3 = 0

State 4 = -1

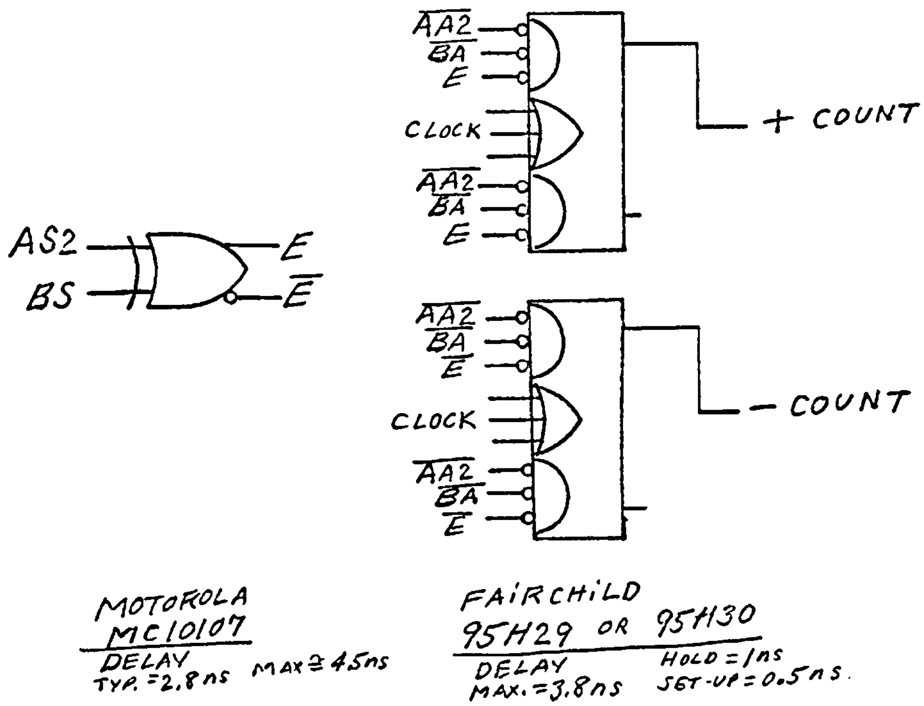
In the two bit system, one bit (the least significant) would indicate a 0 or a 1 (i.e., 0=0, 1=1) and the other bit (the more significant) would indicate a - or a + (i.e., 0=-, 1=+).

Therefore in a straight forward two bit cross correlator we would only count when both terms (sampled outputs from both receivers) are =1. We would count into one counter for + and another counter for -. For the center channel (channel 2), in Boolean Algebra we obtain:

$AA2 \cdot BA \cdot (\overline{AS2 \oplus BS})$ = If true, count in the + counter.

$AA2 \cdot BA \cdot (AS2 \oplus BS)$ = " " " " " - "

Logically this could be done as follows:



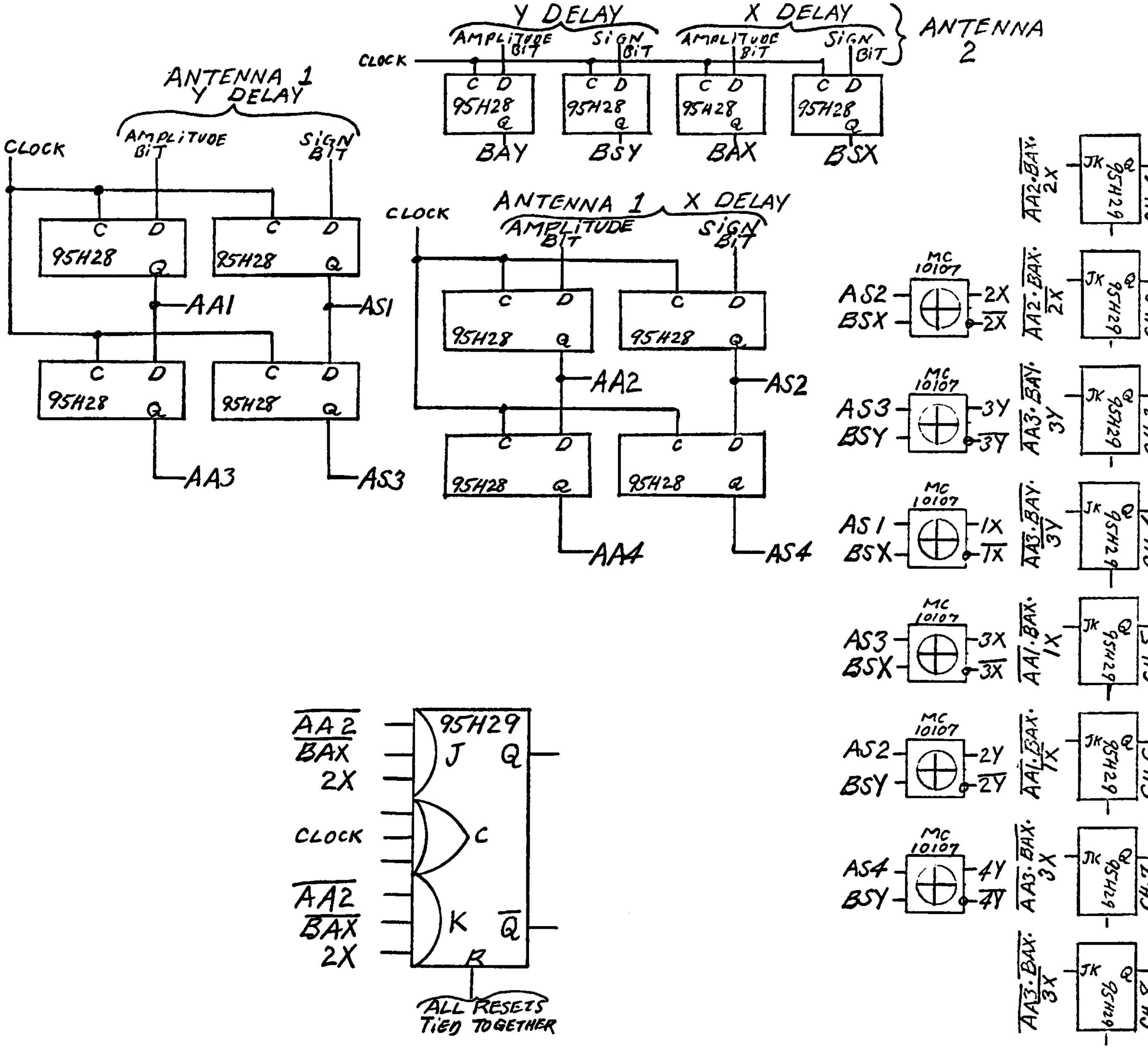
This provides a relatively simple two bit correlator for the center channel. To obtain the other component (sin and cos) we must obtain the difference between channel 1 and channel 3. Besides the value of "0", which is not counted, there can be four different values for this difference: ± 4 and ± 8. To simplify the logic, we can count a 4 as one count and an 8 as two counts. The following Boolean Expressions represent the result of correlating channels 1 and 3 and the taking the difference:

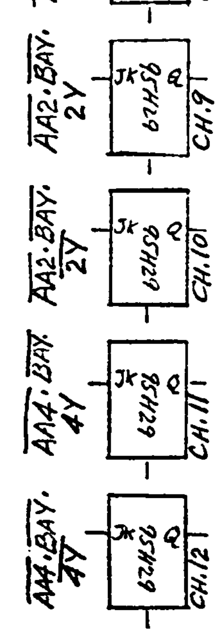
$$-4 \text{ or } -1 \text{ count} = \overline{AA1} \cdot AA3 \cdot BA \cdot \overline{(AS3 \oplus BS)} + AA1 \cdot AA3 \cdot \overline{BA} \cdot (AS1 \oplus AS3)$$

$$+4 \text{ or } +1 \text{ count} = \overline{AA1} \cdot AA3 \cdot BA \cdot (AS3 \oplus BS) + AA1 \cdot AA3 \cdot \overline{BA} \cdot \overline{(AS1 \oplus AS3)}$$

$$+8 \text{ or } +2 \text{ counts} = AA1 \cdot AA3 \cdot BA \cdot (AS3 \oplus BS) \cdot \overline{(AS1 \oplus AS3)}$$

$$-8 \text{ or } -2 \text{ counts} = AA1 \cdot AA3 \cdot BA \cdot \overline{(AS3 \oplus BS)} \cdot (AS1 \oplus AS3)$$





EXAMPLE OF LOGIC FOR CORRELATORS AND FIRST STAGE OF COUNTING-CHANNEL 1

FIGURE 3

DIGITAL DELAY SYSTEM VLA CORRELATOR HIGH SPEED SECTION

9-20-72
eml

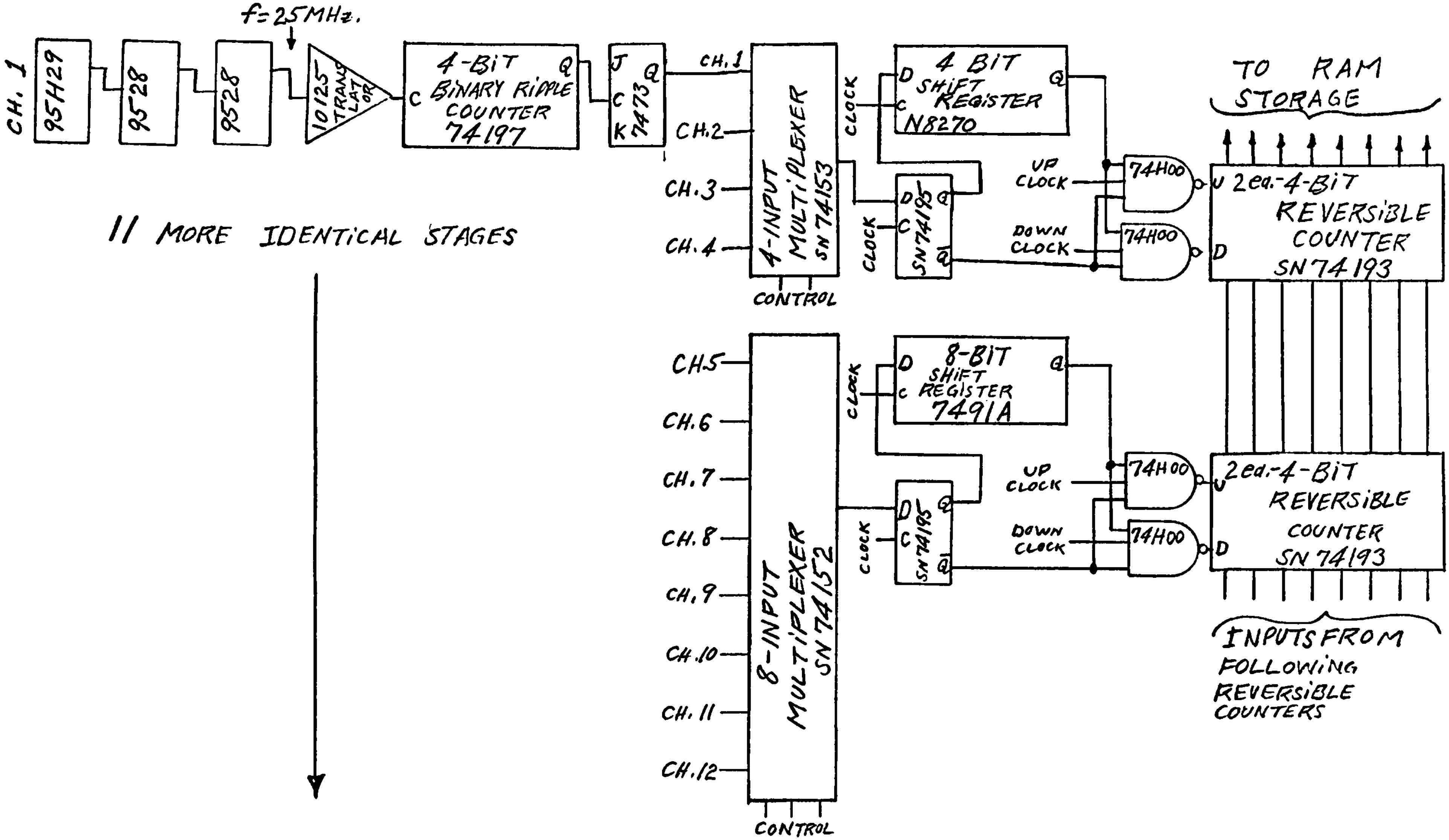


FIGURE 4

DIGITAL DELAY SYSTEM VLA CORRELATOR
LOW SPEED SECTION

9-20-72

Although these equations simplify the logic, it is still more complex than desired. For this report we have decided not to take the difference between channels 1 and 3 prior to counting. However, if a digital delay system is built, this method of subtracting will be reviewed. Therefore, a system was devised in which channels 1 and 3 were correlated and integrated separately until a low speed point in the counters was reached. They are then combined (subtracted). The combination actually involves combining 1 and 3 of both groups of 100 MHz samples and separately combining channel 2 for both groups of 100 MHz samples. The result is that after a certain point in the correlator counters, there are only two reversible counters per 100 MHz bandwidth for each cross correlation. Thus there are (351)X(4)X(2) = 2808 output points (numbers) for the cross correlation functions of the 351 antenna combinations and 4 polarization combinations per two antennas.

Figures 3 and 4 illustrate the correlators.

PRICING

Table 1 tabulates prices for the digital delay line.

Table 2 tabulates prices for the associated correlators.

Table 3 is a condensed combination of pricing for the entire system.

For pricing purposes interfaces are considered between the samplers and the delay system, between the memory output and the computer interface, and between the delay control system and the computer output interface. Therefore, the pricing does not include the samplers or computer interfaces. Pricing assumes all samplers are located in the same racks as the delay system but that the computer interfaces are located in the computer racks. Pricing assumes no RFI requirements. Pricing includes control, display for test purposes and generation of test signals. Pricing is based on use of off the shelf integrated circuits. If the project progresses farther, a study will be made of the possibilities of using hybrid and custom integrated circuit designs to improve reliability and reduce costs.

It is felt that the total costs given are very conservative. A decrease from these costs is a very good possibility.

TABLE 1

DIGITAL DELAY SYSTEM VLA

DELAY SECTION

9/21/72

IC TYPE	QUANTITY	COST EACH	TOTAL COST	POWER EACH (ma.)	POWER TOTAL A	POWER TOTAL W
95H00	1728	11.20	19353.00	76	131	681
9534	1944	4.70	9137.00	80	156	811
R7550	3456	30.00	103680.00	80	276	1435
9504	1134	1.55	1758.00	62	70	364
95H28	54	4.50	243.00	64	3	16
9528	324	3.00	972.00	64	21	109
95H55	182	4.95	802.00	85	15	78
9502	108	1.07	184.00	35	4	21
SUB-TOTAL →	8930		136129.00		676	3515
5% SPARES / 5% CONTINGENCY	893		13613.00		68	351
	9823		149742.00		744 AMPS	3866 WATTS
RACKS & HARDWARE			5000.00			
POWER SUPPLIES			2000.00			
PACKAGING IC's			10000.00			
SUB-TOTAL			166742.00			
LABOR, PROFIT ETC			166742.00			
TOTAL →			333484.00			

TABLE 2

DIGITAL DELAY SYSTEM VLA CORRELATOR

9/21/72
ame

IC TYPE	QUANTITY	COST EACH	TOTAL COST	POWER EACH ma.	POWER EACH mw.	POWER TOTAL A	POWER TOTAL W
95H28 [2] FF	8424	4.50	37908.00	64		539	2804
10107 [3] ⊕	2808	2.00	5616.00	20		56	292
95H29 FF	16848	3.00	50544.00	46		775	4030
9528 [2] FF	16848	3.00	50544.00	64		1078	5607
10125 TRANS.	4212	3.00	12636.00	≅ 65		274	1424
74197 [4] FF	16848	1.21	20386.00	48		809	4044
7473 [2] FF	8424	.43	3622.00	20		168	842
74153 2-4 MULT.	702	2.45	1720.00	36		25	125
74152 8 BIT MULT	1755	2.50	4387.00	26		46	228
74195 PAR. SR4	702	1.04	730.00	39		27	137
7494 SER. SR4	1404	1.00	1404.00	35		49	246
7491A SER SR8	1404	1.18	1656.00	35		49	246
74H00 4-2in NAND	2106	.24	484.00	18		38	190
74193 UD COUNT.	5616	4.00	22464.00	65		365	1825
93410 256 RAM	1012	20.00	20240.00	95		96	481
7483 4 Σ	176	1.36	239.00	78		14	69
95H04 4-2in NOR	3000	1.75	5250.00	62		186	930
CONTROL	1000	2.00	2000.00	40		40	200
SUB TOTAL →	93289		241830.00			4634	23720
5% SPARES } 5% CONTINGENCY }	9329		24183.00			463	2372
SUB TOTAL →	102618		266013.00			5097 AMPS	26092 WATTS
RACKS & HARDWARE			50000.00				
POWER SUPPLIES			15000.00				
PACKAGING IC'S			100000.00				
SUB TOTAL →			431000.00				
LABOR, PROFIT ETC.			431000.00				
TOTAL →			$862000.00				

TABLE 3

DIGITAL DELAY SYSTEM VLA

9/21/72
amd

TOTAL SYSTEM

	QUANTITY OF IC'S	COST	POWER AMPS	POWER WATTS
DELAY	9823	149742.00	744	3866
CORRELATOR	102618	256013.00	5097	26092
TOTALS →	112441	405755.00	5741	29958
RACK & HARDWARE		55000.00		
POWER SUPPLIES		17000.00		
PACKAGING IC'S		110000.00		
SUB TOTAL →		587755.00		
LABOR, PROFIT ETC.		587755.00		
TOTAL →		1,175,510.00		