VLA ELECTRONICS MEMO #113

DIGITAL DELAY AND MULTIPLIER SYSTEM

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May 1973

INTRODUCTION

This report covers the latest design for a Digital Delay Line and Multiplier System for the VLA. For previous work on this subject see VLA Electronics Memo #103 (dated September 22, 1972 - A. M. Shalloway and Peter Camana).

The present specifications for the system are:

Bandwidth = 100 MHz

Broken up into two completely independent systems of 50 MHz each.

Digital Bits = 2

Sensitivity relative to a continuous correlator = 0.81

Delay Resolution: Digital = 10 ns

Analog = 625 ps

Range of Delays: 0 to 163.83 μs

Switching Period: Delay Line = every 50 ms change delay values as required.

Multipliers = blank for 1 ms out of every 50 ms. Dump integrated results into computer every 300 ms.

Racks = 8 plus 2 control consoles

Power (including power supply efficiency) ≃ 29,000 watts

Breakdown of antenna outputs, samplers, delays and multipliers:

Antennas: Each antenna will have the following signals fed to samplers.

Two each Right Sine Polarizations RS

Two each Left Sine Polarizations LS

Two each Right Cosine Polarizations RC

Two each Left Cosine Polarizations LC

The two signals for each polarization will consist two adjacent 50 MHz bandwidth signals.

Two frequencies may be used instead of two polarizations.

Total Antenna Signals to be delayed = (8)(27) = 216

Samplers: The samplers will receive the above signals in the video range with a frequency bandwidth of approximately 1 to 50 MHz. The samplers will be located in the delay racks. Timing and amplitude tolerance specifications are contained in VLA Electronics Memos #109 and #112 (A. R. Thompson, March 19, 1973 and April 9, 1973, respectively).

Total number of Samplers = 216

Delays: Each sampler output requires two delay cards - one for each bit. Because the sine and cosine signals are generated just prior to the samplers, associated sine and cosine signals (RS & RC) from the same antenna receive the same delay. Therefore in the digital delay system there are 108 different delays possible; thus the system is designed with 108 control units for 216 delay lines which consist of 432 delay cards. (One card per bit.)

Multipliers: For any two antennas (A and B), the following multiplications are performed for each of the 50 MHz bandwidths:

RSA x RSB

RSA x LSB

LSA x LSB

LSA x RSB

RSA x RCB

RSA x LCB

LSA x LCB

LSA x RCB

Total Cross Multipliers = (16)(351) = 5616

Every signal is also self multiplied for use in normalization by the computer.

Total Self Multipliers = 416 (208 are redundant)

DIGITAL DELAY SYSTEM

Each of 216 50 MHz bandwidth signals from the antenna array is sampled by a two bit sampler at a 100 MHz rate. The resulting 432 100 MHz digital signals are each to be delayed by up to 164 microseconds in 0.625 nanosecond increments.

Several steps are taken in providing this much delay with such resolution. First, a serial to parallel conversion reduces the 100 MHz data into four each 25 MHz signals. Next in TTL logic a further breakdown into 16 each 6.25 MHz signals is required to reduce the speed to a point where economic bulk delays can be used. This delay takes place in three stages of MOS shift registers. Finally after this bulk delay has been provided recombination

DIGITAL DELAY SYSTEM (cont.)

into four each 25 MHz TTL data signals and finally into a single 100 MHz signal in ECL logic takes place. The programmed delay is achieved in several stages in this process.

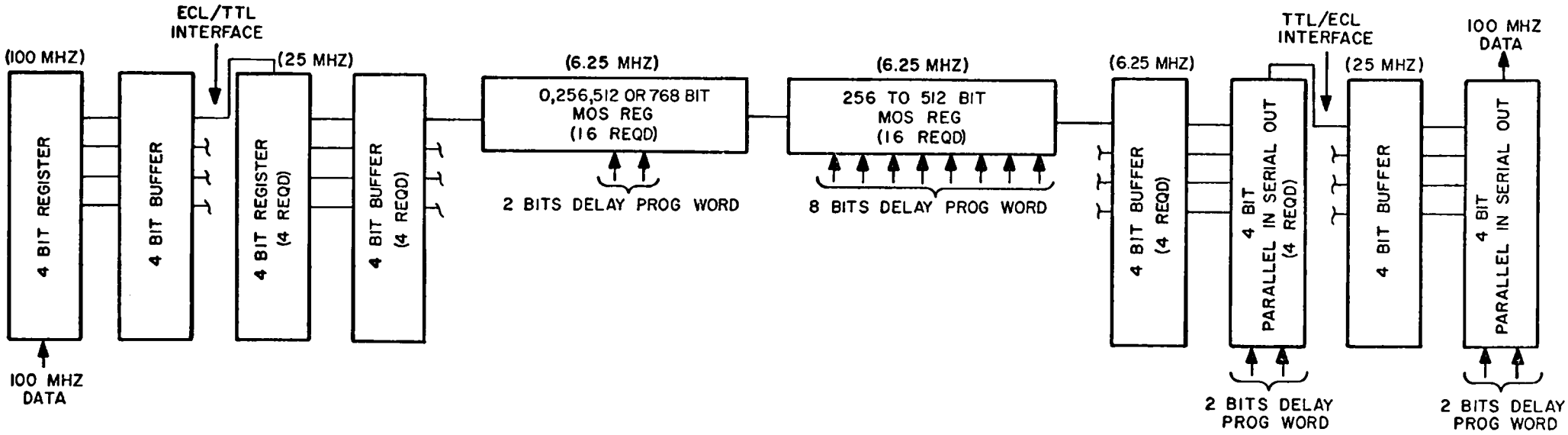
A) 0-10 nsec Delay (0.625 nsec Increments): By phase shifting the sample signal, delays of up to 360° at the sample rate are provided.

B) 10-40 nsec Delay (10 nsec Increments): The timing of the transfer from secondary storage into the 25 MHz to 100 MHz converter (a parallel in serial out register) provides up to 40 nsec delay in four 10 nsec steps.

C) 40-160 nsec Delay (40 nsec Increments): The timing of the transfer from secondary storage into the 6.25 MHz to 25 MHz converters provide up to 160 nsec delay in four 40 nsec steps.

D) 160-40960 nsec Delay (160 nsec Increments): This bulk delay is provided by putting data into a 512 bit MOS register and shifting the register at the data rate part of the time and twice the data rate part of the time. The ratio of time spent clocking at the data rate to the time spent clocking at twice the data rate programs the thru-put time of the 512 bit register from 40.96 to 81.92 μsec in 160 nsec increments, a variation in delay of up to 40.960 μsec.

E) 40960 to 163840 nsec Delay (40960 nsec Increments): The final delay is provided by patching the 16 parallel 6.25 MHz data signals through or around 512 bit and 256 bit MOS shift registers.



DELAY LINE CARD BLOCK DIAGRAM
FIGURE 1

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PACKAGING

As presently envisioned one PC card will contain all logic required to provide the delay for one 100 MHz signal. Both bits of both the sine and cosine components of a given antenna signal will be programmed to identical delays. A single delay line control circuit will program the delays of four delay line cards. Thus for 432 cards 108 delay line controls will be required and as two delay line controls will be contained on one PC card, there will be 54 cards for delay line control. A total of 483 PC cards in four racks are thus required for the digital delay line system. Samplers are to be located on the control cards. Location of the quadrature generators has not yet been resolved.

SELF TEST

The delay system will provide spare delay lines that, under computer control, will scan and check the 432 delay line cards for proper operation. If a defective delay line, or delay control, is detected its output data will be replaced by that of the test delay line until repair is effected. Panel displays will be provided to give an operator the overall status of the delay system. As presently planned each of four racks will contain four spare delay line cards and one spare delay control and outputs of operational delay cards will be checked four at a time. Thus each delay line will be checked for valid operation at a one in 27 duty cycle. This will insure that a minimum of time will expire between the time a delay line receives a new delay program word and it is re-varified at the new delay.

A total of 16 additional delay cards or an increase of about 4% in hardware is required to provide this self test capability.

CLOCK DISTRIBUTION SYSTEM

The VLA Digital Delay Line and Multiplier Systems will be divided into two independent systems of 3024 multipliers and 216 delay cards. Each independent system will require the synchronous operation of approximately 17,000 flip-flops at 100 MHz! In the discussion below only one system is described since each is independent and identical.

With the present packaging plan the 100 MHz system clock must be fanned out to 216 multiplier cards with 58 ECL loads each and 27 delay line control cards with 80 ECL loads each. This yields a total of 243 points for clock distribution. The 216 delay line outputs must each fan out to an average of 18 multiplier cards for a total of 3888 data interconnects. The maximum distance that clock or data must be transmitted will be about 8 ft.

Synchronous operation will be achieved by maintaining all clock cable lengths equal and all data cable lengths equal. The transmission medium will probably be 50 ohm coax although higher impedance coax, twisted pair cable, and triad cable is being considered.

Two options for distributing clock to so many loads are being studied at present.

1) The first method would use a gate tree using high speed clock drivers to develop the 243 clock drive requirement and a second tree on each card to develop the card fan out requirements. Two levels of gates external to the cards would be used and propagation delays of these gates would be matched so as to maintain clock timing. Two additional levels on each card would provide the required drive and would introduce up to 3 nsec clock skew throughout the system.

2) The second method being studied for clock distribution would provide 243 sine wave clock signals for fan out to the individual cards. RF power amplifiers would develop the required power drive and phase shift adjustments would allow for timing correction. Each card would also have a power amp and distribute either shaped or sine wave clocks to individual loads.

MULTIPLIER SYSTEM

A two bit, three level digital signal is produced by the samplers. For details on this type of signal, reference should be made to:

Australian Journal of Physics; Correlators With Two-Bit Quantization, B.F.C. Cooper; 1970, 23, p521-7.

A condensed discussion of this subject is also contained in VLA Electronics Memo #103 (A. M. Shalloway and Peter Camana, September 22, 1972).

Briefly stated, the output code of the samplers indicate that the signal was in one of three levels as follows:

LEVEL OF SIGNAL(S)	ASSIGNED VALUE	OUTPUT CODE OF SAMPLER		
			A1	A0	
S > + 0.612 RMS of Signal	+1		0	1	
-0.612 RMS < S < 0.612 RMS	0		0	0	
-0.612 RMS > S	-1		1	0	

The output code is chosen arbitrarily to simplify the logic. A normal multiplication table for the above would be:

ANT. A → / ANT. B ↓	-1	0	+1
-1	+1	0	-1
0	0	0	0
+1	-1	0	+1

To perform this multiplication and integrate the results would require reversible counters. To simplify the system, an altered multiplication table is used in which +1 is added to each multiplication result:

ANT. A→ ANT. B↓	-1	0	+1
-1	2	1	0
0	1	1	1
+1	0	1	2

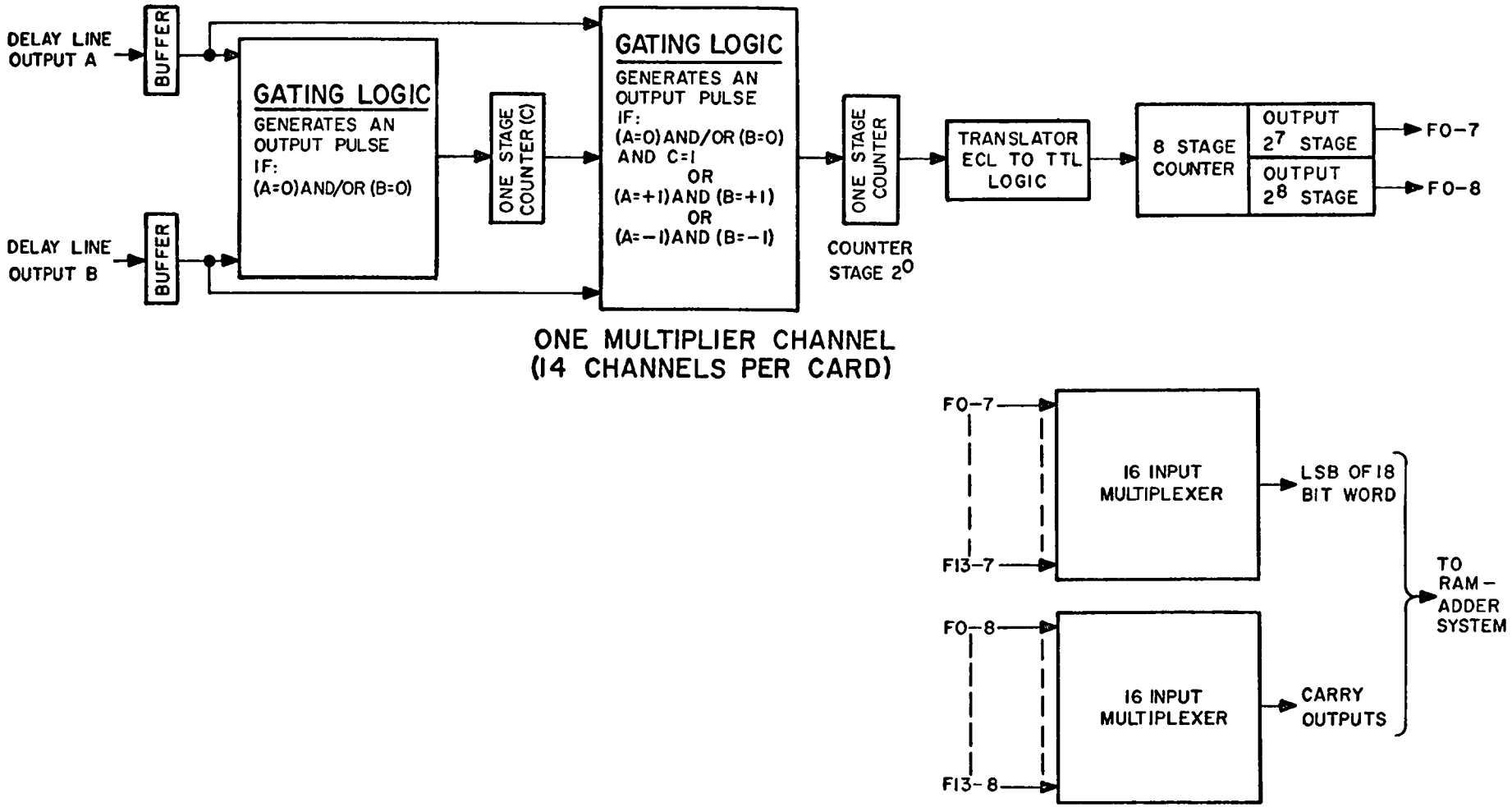
The control section can correct for this change simply:

$$V_n' - V_0 = V_n$$

where V_n' = results of integration of multiplier N after a period T, V_0 = number of multiplications performed during T and V_n = results desired; that is, the results that would have been obtained with the unmodified multiplication table.

A logic circuit has been designed and is being tested to accomplish the above multiplication and integration. This is shown in block diagram form in Figure 2. This drawing illustrates one channel and the multiplexing of 14 channels.

All that is shown in Figure 2 is contained on one PC board. One channel is a self multiplier and thirteen channels are cross multipliers. The arrangement of channels per board for one set of 50 MHz B.W. multipliers is shown in Table 1. In this arrangement there normally would be 108 self multiplier



MULTIPLIER CARD BLOCK DIAGRAM
FIGURE 2

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channels not used. However, because of the simplicity of the additional connections, these 108 channels are used to provide redundant self multiplier channels, since the loss of a self multiplier channel is a greater loss than that of a cross multiplier channel.

The multiplexers, shown in Figure 2, feed a system of small fast RAMs (Random Access Memories) and adders, and larger slower RAMs and adders to obtain the additional stages of the counters. The large RAMs are sufficient in size to integrate the present data while also holding and distributing simultaneously the data from the previous 300 ms to the computer.

Starting with counter 2^0, there are 25 stages of counters required to integrate for 300 ms. A minimum of the 16 most significant bits must be saved for the computer. An additional one, two or three bits would provide some improvement in the signal. By operating the memory following the multiplexers at high speed and by the use of one multiplexer per board it is possible to save the 18 most significant bits.

At the end of each 300 ms period, the computer can remove from the multiplier system any channels it requires. The removal must be complete before the end of the next 300 ms period. For one millisecond out of every 50 ms, transmission in the waveguide system is reversed and during this time the the multipliers are blanked.

TABLE I

VLA MULTIPLIER INTERCONNECTION ARRAY

Abbreviations: R = right circular polarization
L = left circular polarization
S = sine
C = cosine

Example: RS2 represents the right circular polarization, sine component of antenna #2.

For each 50 MHz B.W. there will be eight arrays with 27 printed circuit cards per array, arranged as follows:

	SELF-MULTIPLIED ANTENNA OUTPUT		CROSS MULTIPLIED ANTENNA OUTPUT A	x	B
ARRAY #1	RS		RS		RS
" 2	LS		LS		LS
" 3	RC		RC		LC
" 4	LC		LC		RC
" 5	RS		RS		RC
" 6	LS		LS		LC
" 7	RC		RC		LS
" 8	LC		LC		RS
PC CARD NUMBER	↓		↓		↓
1			1	x	2-8
	2	x	2	x	3-8
2			2	x	9-15
	1	x	1	x	9-14
3			3	x	4-10
	4	x	4	x	5-10
4			4	x	11-17
	3	x	3	x	11-16
5			5	x	6-12
	6	x	6	x	7-12
6			6	x	13-19
	5	x	5	x	13-18
7			7	x	8-14
	8	x	8	x	9-14

PC CARD NUMBER	↓		↓		↓
8			8	x	15-21
	7	x	7	x	15-20
9			9	x	10-16
	10	x	10	x	11-16
10			10	x	17-23
	9	x	9	x	17-22
11			11	x	12-18
	12	x	12	x	13-18
12			12	x	19-25
	11	x	11	x	19-24
13			13	x	14-20
	14	x	14	x	15-20
14			14	x	21-27
	13	x	13	x	21-26
15			15	x	16-22
	16	x	16	x	17-22
16			16	x	23-27,1-2
	15	x	15	x	23-27,1
17			17	x	18-24
	18	x	18	x	19-24
18			18	x	25-27,1-4
	17	x	17	x	25-27,1-3
19			19	x	20-26
	20	x	20	x	21-26
20			20	x	27,1-6
	19	x	19	x	27,1-5
21			21	x	22-27,1
	22	x	22	x	23-27,1
22			22	x	2-8
	21	x	21	x	2-7
23			23	x	24-27,1-3
	24	x	24	x	25-27,1-3
24			24	x	4-10
	23	x	23	x	4-9
25			25	x	26-27,1-5
	26	x	26	x	27,1-5
26			26	x	6-12
	25	x	25	x	6-11

Card number 27 does not fit as smoothly in the array - although it is physically identical to the other cards. Therefore, card number 27 for each array is listed separately below:

PC CARD NUMBER	↓		↓		↓
27(1)			27LC	x	1,8-13RS
	27RS	x	27RS	x	8-13RS
27(2)			27RC	x	1,8-13LS
	27LS	x	27LS	x	8-13LS
27(3)			27LS	x	1,8-13LC
	27RC	x	27RC	x	8-13LC
27(4)			27RS	x	1,8-13RC
	27LC	x	27LC	x	8-13RC
27(5)			27LC	x	1-7RC
	27RS	x	27RS	x	2-7RC
27(6)			27RC	x	1-7LC
	27LS	x	27LS	x	2-7LC
27(7)			27LS	x	1-7LS
	27RC	x	27RC	x	2-7LS
27(8)			27RS	x	1-7RS
	27LC	x	27LC	x	2-7RS

ADDITIONAL DATA

Total number of 100 MHz data transmission lines (includes both 50 MHz sections) from delay cards to multiplier cards = 7776.

Total number of 100 MHz clock transmission lines (includes both 50 MHz sections) from clock distribution system to multiplier cards = 432.

A method to reduce this large number of cables to a much smaller number of flat cable transmission lines connecting into "mother-boards" is being investigated.

CONTROL

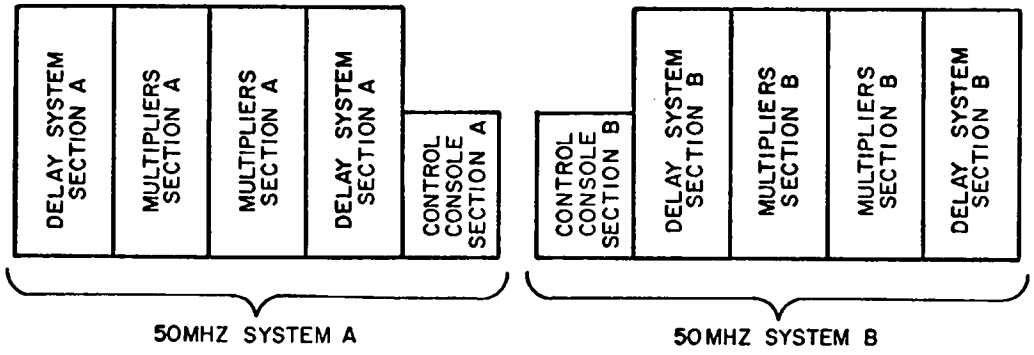
There will be a central control system. This will consist of a micro-computer plus some high speed peripheral logic to accomplish the following tasks:

1. Control transfer of data from counters to fast small RAMs and from fast small RAMs to large RAMs.
2. Gate clocks at blanking time.
3. Subtract V_0 from all counter output data to correct for modified multiplication table.
4. Accept delay values from computer and enter into delay registers.
5. When a bad delay line card is indicated, decide whether the spare or the operating card is defective. Switch in spare if called for and notify computer and operator that a defective card exists with an indication of which card he should change.
6. Automatically turn on multiplier test signals and check outputs.
7. For maintenance purposes, display data from any multiplier channel desired by operator.
8. Monitor temperatures, air flow, and voltages.
9. Accomplish any tasks necessary in maintenance, such as integrating a particular channel for more than 300 ms or 10 sec.

10. Communicate with the computer to supply it with the multiplier data and any monitor data required.

SYSTEM PACKAGE

The entire system will be packaged in eight racks and two control consoles as shown in Figure 3. The system will be located in a screen room to allow servicing while the array is in operation.



NOTE: RACK PANEL AREA=24" WIDE BY 63" HIGH PLUS POWER SUPPLY SPACE. IT WOULD BE HIGHLY DESIRABLE TO MOUNT POWER SUPPLIES (ONE SET PER RACK – ABOUT 19" x 20" PANEL SPACE) OUTSIDE OF ABOVE RACKS.

RACK LAYOUT–DIGITAL DELAY–MULTIPLIER SYSTEM
FIGURE 3