NATIONAL RADIO ASTRONOMY OBSERVATORY

VLA ELECTRONICS DIVISION MEMO #121

RELIABILITY STUDY OF VLA DIGITAL DELAY AND MULTIPLIER SYSTEM

R. P. ESCOFFIER
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This memorandum gives the result of a survey of semiconductor reliability and contains an estimate for the reliability to be expected of the VLA Digital Delay and Multiplier System.

1. MANUFACTURERS DATA

Each of the major suppliers of IC's being used in the VLA Digital Delay and Multiplier System has an on-going reliability study program to determine failure rates of each of its larger product lines. Unfortunately, due to high reliability levels of integrated devices only very large lines such as the 7400 logic family have accrued sufficient device time to yield calculated failure rates. Other logic lines such as ECL logic have device hour limited estimates of failure rate.

Reliability tests vary little from supplier to supplier but interpretation of raw data to produce published failure rates vary quite a bit. Samples of a produce line selected at random are operated at high still air temperatures (generally 125°C) under various loads and at rated voltage. Various conditions of static or dynamic operation are used and the devices are periodically tested against their specifications. Failures are generally reported as degradation or catastrophic failures. Most manufactures report all failures, however some such as National Semiconductor have devised fudge factors whereby some failures may be thrown out as due to infant mortality. Calculated failure rates at 125°C are then derated to yield failure rates at the desired operating temperature. Derating factors however vary widely from supplier to supplier. The table below gives the derating factors used by various manufacturers. These factors are used as below.

$F_C = F_{125}\,(D_C)$ where F_C = Failure rate at temp C.

F_{125} = Failure rate at 125°C

D_C = Derating factor at temp. C

TABLE I

Manufacturer	125°C Factor	50°C Factor	25°C Factor
Motorola	1.0	.26	.1
TI	1.0	.147	.054
Signetics	1.0	.06	.018
National Semi.	1.0	.0009	.000045
Intersil	1.0	.09	.03

Each manufacturer (including National Semiconductor) defends its own derating factors and cites literature to prove its own to be correct.

In order to combine failure rates of various suppliers IC's to obtain overall failure rates for a system, a common derating factor was applied to manufacturers raw 125°C data. Since only Signetics supplied both 125°C and 25°C raw data in significant device hours their factors were applied to all data in Table II. In addition to manufacturer supplied data Table II also contains some high device hour data obtained from government sponsored reliability tests. This data comes from the "Microcircuit Generic Failure Rates" book put out by the Reliability Analysis Center (TK7874 in NRAO Engineering Library). Again raw data was modified using Signetics derating factors.

TABLE II

Manufacturer	Semiconductor Type	Device Hours x 10^6	Failures	125°C Failure Rate %/1000 Hr	25°C Failure Rate %/1000 Hr
Motorola	ECL 10,000	2.33	3	0.177	.0032
TI	TTL SSI 7400	12.7	8	0.062	.0011
TI	TTL MSI 7400	1 to 2	?	0.102	.002
(1) Signetics	All products	31.4 @ 125°C	17	0.058	---
(1) Signetics	All products	460 @ 25°C	3	-----	.001
Signetics	ECL 10,000	1.34	0	0.07	.0013
National Semi.	Bipolar	2.9	0	0.031	.00056
National Semi.	MOS	3.65	9	0.25	.0045
Intersil	MOS	1.5	?	0.3	.0054
TI	Transistor +Diodes	?	?	0.015 (2)	0.001 (3)
(4)	TTL Complex Gate	465 (5)	13	0.052	.00094
(4)	TTL Gate	688 (5)	0	0.0022	.00004
(4)	TTL Flip-Flop	77 (5)	6	0.15	.0027
(4)	TTL Gates	25 (5)	1	0.13	.0023
(4)	TTL Gates	108 (5)	14	0.23	.0041
(4)	TTL Complex Gate	1800 (5)	12	0.012	.00021
(4)	MOS	16.7 (6)	0	?	?
(4)	ECL	31.3 (7)	0	0.132	.0024

NOTES:

(1) Data from which derating factor calculated.

(2) Junction temp. 100°C

(3) Junction temp. 60°C

(4) From "Microcircuit Generic Failure Rate"

(5) Device hours at 50°C

(6) Device hours at unspecified temp.

(7) Device hours at 30°C

From Table II most device failure rates at 25°C (still air) turns out to be between 0.005 and 0.001 %/1000 Hr. Some of the very low failure rates such as 0.00004 %/1000 Hr. come from devices with unknown burn-in history. All manufacturers data are taken from off the line devices with no burn-in.

2. DIGITAL DELAY LINE AND MULTIPLIER FAILURE RATE

A parts count for the full 27 antenna VLA High Speed Digital System is given below:

ECL SSI	31K
ECL MSI	2K
TTL SSI	5.7K
TTL MSI	32.6K
MOS LSI	10.5K
Linear	2.5K
TOTAL	84.3K
Transistors	23.1K

Most manufactures agree that IC reliability depends more on bond failures, chip surface area and batch oriented fabrication problems than on IC type, family, or circuit complexity. In addition in most entries of Table II some portion of the device hours listed were non-operative storage hours. Hence all things considered there seems to be sufficient lack of precision that little is to be gained in trying to assign specific values of failure rate to each type or classification of IC used. Hence in calculating a value for the mean time between failure of the VLA Digital System a single value of failure rate was applied against all 85,000 IC's. Failure rates of 0.002%/1000 Hr. for IC's and 0.001%/1000 Hr. for transistors were selected on the assumption that with the 15°C moving air environment they would produce a pessimistic MTBF figure.

From these assumptions the MTBF calculates to be:

$$(MTBF)_{IC} = \frac{1000x100}{Fx85,000x24} = 24.5 \text{ days}$$

$$(MTBF)_{TRAN} = \frac{1000x100}{Fx23,100x24} = 180 \text{ days}$$

MTBF = 22 days

One item that seems to reduce the meaning of the above figure is that most manufacturers claim an order of magnitude or more improvement in failure rate for their burned-in components. Yet Signetics and TI both stated when asked that no difference could probably be detected between high price burned-in components and unscreened components that had operated 1000 hours or more in normal applications. The calculated MTBF or 22 days is therefore an average (over an uncertain time) of infant mortality time (first 1000 hours of operation) and normal operation. The 22 day MTBF will therefor get significantly better after the first 40 days of operation. If some of the failure rates of the very large device hour items in Table II which were presumably either burned-in components or operated for sufficient time to swamp out early failures, than an MTBF of well over 100 days is indicated.

3. BURNED IN COMPONENTS

Most semiconductor manufacturers will supply at additional cost various levels of burned-in or screened components. The effect of such effort is to eliminate infant mortality. Somewhere between 0.1 and 0.15% of devices fail within the first 1000 hrs. of operation and burning-in rejects a like number of devices. An improvement of a factor of 10 or more in failure rate is claimed for burned-in parts, however as stated before burning-in or 1000 hrs. of normal operation produce the same result.

Below is a brief review of some screening programs available:

a) TI REL II, Level I: (7400 series only) 48 hours bake at 150°C, 100% electrical test, 0.25% complete military QC testing. Cost 12¢ per IC (1K price).

b) TI REL II, Level II: (7400 series only) same as above except additional 168 hour power on burn-in at 125°C. Cost 27¢ per IC (1K price).

c) Signetics Super Dip (7400 series at present): 100% visual inspection of chip and bonds, 15 cycles 0 to 100°C shock, 100% electrical test, 100% high temp. test, 0.15% complete military QC testing. Price 3¢ to 6¢ per IC.

As stated about 0.1 to 0.15% of devices fail during the first 1000 hours of operation. Thus with 95K semiconductors the VLA Digital System can expect 100 to 140 early failures. Card test should catch a fair percentage (especially if temperature tests are preformed at card level test) of these reducing the early failures to somewhere below 100.

Another factor to be considered in evaluating the need or convenience of screened components is the gradual buildup of hardware over almost 10 years expected in the VLA. Such a buildup will spread out the early semiconductor failures over the several discrete steps in hardware.