NATIONAL RADIO ASTRONOMY OBSERVATORY
Charlottesville, Virginia

VERY LARGE ARRAY PROJECT

VLA Electronics Division Memo #124

THE DESIGN OF THE VLA FRINGE ROTATOR SYSTEM

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I. INTRODUCTION

The output of the multiplier of a simple two-element interferometer contains a sinusoidal component caused by the rotation of the earth which sweeps the fringe pattern across the area of sky under investigation. The frequency of this output is usually referred to as the natural fringe frequency. Measurement of the amplitude and phase of the fringe-frequency output involves fitting a sine curve to sampled data points, and since the sampling rate must be at least twice the output frequency the computing task can become large if the baseline is long. To avoid this problem an instrumental phase shift can be introduced into the received signals to cancel or reduce the shift resulting from earth rotation. In effect the fringe pattern is rotated relative to the earth to follow the part of the sky being observed. This is most conveniently accomplished by introducing a continuous phase shift, i.e. a frequency offset, into one of the local oscillators used in converting the signals before they are multiplied together. In a synthesis array like the VLA a fringe rotating phase shifter is used for each antenna, and the frequency offset is set to cancel the natural fringe rate for a baseline from the antenna to a common reference point. Output fringe frequencies for all antenna pairs of the array are thereby reduced to zero.

Rotation of an interferometer fringe pattern to reduce the fringe frequency in the output for large antenna spacings was first used in an interferometer constructed by the author and colleagues at Jodrell Bank (Hanbury-Brown, Palmer & Thompson 1955). In an earlier instrument used for solar

observations the fringe pattern was swept across the sun to increase the output frequency when the natural fringe frequency was inconveniently low (Little and Payne-Scott, 1951).

2. REQUIRED PARAMETERS FOR THE VLA FRINGE ROTATORS

First consider the range of frequency offsets required. The center of the wye will be taken as the phase reference point. For any antenna the natural fringe frequency f_n is given by

$$f_n = -\omega_o D \cos\delta \cos d \sin (H-h) \qquad (1)$$

where ω_o is the angular rotation frequency of the earth, D is the baseline measured in wavelengths to the center of the wye, H&δ are the hour angle and declination of the field center and h&d the same parameters for the baseline direction from the wye center to the antenna.* Maximum f_n occurs for an antenna at the end of the SE or SW arm for which, at an observing frequency of 24 GHz, $D = 1.68 \times 10^6$ and $\cos d \simeq 0.91$. Then for $\delta = 0°$ and $H - h = 90°$, $f_n = 111$ Hz. In the normal operation of the array this will be the highest frequency offset which the fringe rotators will be called upon to provide. However to allow for possible future use of shorter wavelengths or extended baselines using outrigger antennas a capability of handling fringe frequencies of to about 500 Hz should be provided.

The systems which have been considered most suitable for the VLA involve phase shifters with adjustment in discrete steps; these are convenient for digital control and avoid drift problems which can occur with continuously variable devices with analog control signals. The choice of the minimum step size, $\Delta\phi$, is governed by the criterion that we want the fringe rotation sysem to introduce no more than about 1° of phase error into the measured fringe visibilities. When the fringe frequencies are high the effects of the discrete

*With this convention f_n is positive when the fringe effect causes the received signal to appear to be at a higher frequency at the antenna than at the wye center.

steps average out, and serious errors are likely to occur only when the fringe frequency for any antenna pair passes through zero. The error in the measured phase, which is the sum of the errors of two fringe rotators, has a triangular probability distribution with maximum values $\pm\Delta\phi$ and and rms value of $\Delta\phi/\sqrt{6}$. A minimum step size of about 1° is therefore called for. The statistical considerations are identical to those given in VLA E.M. #109 concerning the phase errors resulting from the finite step size in the delay system. In that case the minimum step of 625 ps corresponds to 5.6° at the IF center frequency of 25 MHz. Since the delay system is more difficult and expensive to construct than the fringe rotators, it is logical that of the two it should set the limit of accuracy.

The natural fringe frequency varies as a sine function of hour angle (eq. 1), and the setting of the fringe rotators to provide a particular rate of change of phase must be readjusted at frequent intervals. Over a short time period the change of fringe phase closely approximates a parabolic function of time, so the setting of the initial phase and rate of change of phase of the fringe rotators involves determing the straight line that best fits a section of a parabola. This problem is examined in Appendix 1 where it is shown that if the rms deviation of the linear phase shift from the desired parabolic one is not to exceed 1° with the highest rate of change of fringe frequency encountered in the array, the fringe rotators must be reset at intervals of not greater than 2.5s. For a fringe frequency of 111 Hz the phase change in 2.5s is 10^5 deg., so the offset frequency of the fringe rotator must be set to an accuracy of 1 part in 10^5 if the phase changes introduced are to remain within 1° of the best straight line fit over 2.5s. It is assumed that some increase in the rms deviation can be tolerated with fringe frequencies greater than 111 Hz.

The required parameters of the VLA fringe rotators can be summarized as follows:

Frequency range $\pm$(0 - 500 Hz)

Frequency setting accuracy 5×10^{-3} Hz

Minimum phase shift increment $\simeq 1°$

3. SOME POSSIBLE PHASE SHIFTING SCHEMES

A simple method of introducing phase shifts in a local oscillator involves inserting a DC offset in the phase detector of a phase lock loop. This however is an example of the kind of drift-prone arrangement that we want to avoid. A method that has been examined in more detail involves a switchable binary sequence of transmission-lines cut to provide shifts of 180°, 90°, 45°, etc. at the oscillator frequency. An eight-bit phase shifter provides a minimum increment of 1.4°, and a nine-bit one 0.7°. The optimum frequency for such a system is in the vicinity of 100 MHz since then all but the longest bits can be fabricated in microstrip, the shortest bit is not inconveniently short, and the frequency is high enough that PIN diodes can be used for switching. The switches would be controlled by a binary counter with one stage for each bit, driven by a pulse generator the rate of which is set to correspond to the required frequency offset. A quotation for a nine-bit phase shifter of this type for a frequency of 100 MHz was obtained from Daico Industries, Inc. of Compton, California. The price for a single unit was about $1200 but dropped by almost half for a quantity of 100 or more. The number required in the VLA is 108 plus spares, one for each 500 MHz IF channel of each antenna. A problem with this scheme, though not a serious one, is that the effects of residual amplitude modulation must be eliminated by use of a limiting amplifier or, better still, by using the phase shifter on the reference frequency of a phase locked oscillator.

The system that was finally chosen uses a type of digital frequency synthesizer and is described in detail in the following section. It is less expensive than the last scheme, it is flexible in design, and with the exception of a crystal filter involves only commonly available integrated circuits and simple components.

4. OPERATION OF THE FRINGE FREQUENCY SYNTHESIZER

Consider a frequency divider chain with an input frequency f_1 and an output frequency f_1/N. If the count of the first stage is inhibited for one cycle the phase of the output frequency is retarded by 360°/N, and if an extra pulse is inserted at the input the output phase is advanced by 360°/N. Now suppose that inhibiting a count or adding an extra one is caused by a pulse from a variable-frequency pulse generator, the frequency of which, f_v, is less the f_1. The output frequency of the counter now becomes $(f_1 \mp f_v)/N$. Furthermore, the phase of the counter output at the time that it is started can be selected by appropriately setting the initial state of each flip-flop. If the counter output is added on to a local oscillator that converts the received signal, such a scheme can perform the required fringe rotation.

A simplified block diagram of the system designed for the VLA is shown in Figure 1. The high frequency that is counted down is 50 MHz, the division factor N is 500, so the output frequency is 100 kHz for zero frequency offset. The division factor was chosen as 500 rather than an integral power of two because the input and output frequencies can then be equal to standard reference frequencies in the system which are round numbers in decimal terms. The minimum phase step is 360°/500 = 0.72°. The variable-frequency generator is a rate multiplier and this produces a frequency in the range 0 to 12.5 MHz that can be set to 1 part in 2^{18} ($=2.6\times10^5$). The output is frequency-divided by 50 and enters a pulse synchronizer which for every input pulse produces an output pulse in synchronism with the 50 MHz clock. The output of the synchronizer

operates an add/subtract circuit that causes the main divider to count zero or two depending on the value of the sign-of-rate control bit.

The basic principle of operation of the rate multiplier is shown in Figure 2.a. A divider chain of n flip-flops is fed at an input frequency f_o. Suppose that the positive going edge of the output from each stage triggers the following stage. Then if the other edge, the negative going one as shown in the figure, is used to generate a pulse, we obtain a series of pulses at frequencies $f_o/2$, $f_o/4$ $\cdots\cdots$ $f_o/2^n$, which have the property that none of the pulses in the n different trains coincide in time. By gating and summing the appropriate pulse trains any frequency from zero to $f_o \sum_{m=1}^{n} 2^{-m} = f_o\,(1-2^{-n})$ can be obtained in steps of $f_o/2^n$. The pulses in the output of the summing network do not, of course, come at regular intervals, and to investigate this effect consider a case where the highest frequency pulse train for which a gate is open is at frequency f_o/ℓ. The longest interpulse period that can occur is then ℓ/f_o. If all of the lower frequency gates are open the frequency of the summed pulse trains approaches $2f_o/\ell$. Thus the longest period minus the shortest period can take values up to $\ell/2f_o$, which, expressed as a fraction of the mean period lies between 0.5 & 1.0. If the frequency of the summed pulse train is then divided by a factor k (which is 50 in the system of Figure 1) this relative jitter should decrease approximately as $k^{-1/2}$.

An alternative scheme for producing a variable pulse rate was suggested by B. G. Clark and is shown in Figure 2.b. A number N_1 is set into an n bit binary register and then added into another register f_o times per second. The output, taken as the most significant bit of the adder, has a frequency $N_1 f_o/2^n$ and as N_1 is varied can take values from zero to $f_o\,(1-2^{-n})$ in steps of $f_o/2^n$. The interpulse periods are more even than obtained with the rate multiplier described above since in this case the difference between the longest and shortest periods is zero or f_o^{-1} which may be only a small fraction of the mean output

period. However a special integrated circuit is available for implementing the rate multiplier system of Figure 2.a, with six stages of division and gating in a single 16-pin package (Texas Instruments SN7497). The rate multiplier scheme was therefore chosen for the fringe rotator application since it requires fewer integrated circuits and thus should result in greater reliability. The irregularity in the output period is not serious since some further frequency division following the variable frequency generator is easily provided.

The circuitry of the pulse synchronizer, the first two stages of the counter and the add-subtract gating uses ECL logic and the remainder of the system uses TTL. The pulse synchronizer is shown in Figure 3.a. Both flip-flops are initially in the zero state. When the clock input of F_1 receives a positive going pulse from the variable frequency generator, F_1 goes to state 1. This allows F_2 to go to state 1 on the next pulse of the 50 MHz clock, and the Q output of F_2 resets F_1 to the zero state. Since the D input of F_2 is then low, it returns to the zero state at the next clock pulse.

The first two stages of the counter and the add-subtract circuitry are shown in Figure 3.b., and the truth table indicates the conditions under which the flip-flop F_2 changes state when a clock pulse occurs. When B, the output of the pulse synchronizer, is high, clocking of the flip-flop is inhibited if the sign-of-rate bit is low, effectively subtracting a count. When B is high and the sign-of-rate is high the second flip-flop counts but the first one remains in the same state, resulting in a count of two which effectively adds a pulse. This circuit is adapted from one designed by A. M. Shalloway to integrate the outputs of the signal multipliers by adding counts of zero, one or two.

Note that the maximum clock frequency that can be used is determined by the propagation time not only of F_1 in Figure 3.b., but also that of the or-gates since the inputs to F_2 must have settled before the next clock pulse comes

along. The use of ECL circuitry was therefore deemed necessary in an initial design in which the clock frequency was 2^{26} Hz ($\simeq$ 67 MHz), and ECL was retained for 50 MHz operation because of the desirable performance margin it provides. The first two stages of the counter are followed by an ECL to TTL level translator and three stages of division by five.

At intervals of approximately two seconds the output frequency of the rate multiplier is reset and the phase of the 100 kHz output waveform is required to start with a given value relative to the phase of a 100 kHz reference waveform provided by the oscillator system. A number n_p representing the required initial phase is received from the computer and set into the ÷500 counter by a reset pulse that is synchronized with the 100 kHz reference as indicated in Figure 1. The phase of the counter output waveform then leads that of the reference by $2\pi\ n_p/500$. The arrangement for setting the two ECL first-stages of the counter to unity or zero is shown in Figure 3.c. For the maximum fringe frequency of 111 Hz an accuracy of 0.5° in setting the initial phase requires that the reset time be specified to an accuracy of 12.5 μs, which is just compatible with the synchronization requirement with the 100 kHz reference.

The phase of the output waveform can be further varied by 180° by passing it through either an and-gate or a nand-gate. This condition is determined by one control bit and is used to provide the phase switching required to eliminate the effects of DC offsets at the samplers described in VLA E.M. #122.

As a visual indicator of the fringe rate a light-emitting diode is driven by a nor-gate the inputs of which are fed by the 100 kHz output waveform and the 100 kHz reference. The light is off when both waveforms are in the low state, and its average brightness thus varies as the relative phase of the two 100 kHz waveforms changes, being a minimum when they are in phase.

5. COMMUNICATION WITH THE COMPUTER

Communication between the fringe rotators and the computer takes place through the Monitor and Control System. Instructions from the computer are received in the form of 24-bit words which are received in serial form, the first bit being the most significant. Serial to parallel conversion for two words is included in each phase rotator unit. The most significant bit of the first word sets the sign of the rate and the next 18 bits set the output frequency of the rate multiplier. In the second word the 11 most significant bits set the initial phase, the first three groups of three bits specifying numbers in the range 0-4 and the last two bits each specifying 0 or 1. Thus if the bit values of 0 or 1 are represented by B1 to B11, B1 being the most significant, the phase number n_p is equal to

$$100(4B1 + 2B2 + B3) + 20(4B4 + 2B5 + B6) + 4(4B7 + 2B8 + B9) + 2B10 + B11 \quad (2)$$

Computation of the required bit values is described in Appendix 2.

It is currently planned to reset the fringe rotators six times in each 10s receiving cycle so the four units located at each antenna will require a total of 288 words per minute. The addresses to be assigned to these words and the location of the phase-switch control bit have not been finally determined at this time.

6. LOCATION OF THE FRINGE ROTATORS

In the initially envisaged block diagram of the VLA (March-April 1973) the fringe rotators were located at the central control building and included in the IF receiver block. The synthesizer output was added to a local oscillator in the 1-2 GHz region which converts the IF signals down to a 0-50 MHz band. Tests were made of a single-sideband, suppressed-carrier mixer using two Relcom MIJ units with appropriate phasing to add the 100 kHz to a 1-2 GHz signal, but it was found possible to get suppression of the unwanted responses by only about 25 dB,

and then only with careful adjustment. A suppression of at least 33 dB is required as explained in VLA E.M. #116. A mixer followed by a crystal filter was found to give satisfactory results, the 100 kHz being first added to a frequency of 65 MHz which was chosen because it lies outside the 0-50 MHz IF band but is not too high for crystal filter manufacture. A four-pole monolithic crystal filter with 30 kHz bandwidth by Peizo Technology gave 60-70 dB suppression of the unwanted responses.

A subsequent discussion of spurious responses in the system described in VLA E.M. #122 indicated advantages in performing the fringe rotation on the signals as early in the system as possible. In particular it should occur at the antennas otherwise spurious signals introduced in the modem and waveguide system can result in fringe-frequency components at the multiplier outputs. It has therefore been decided to perform the fringe rotation at the mixer at which the signals are converted from the 4.5-5.0 GHz range of the parametric amplifiers to the 1-2 GHz range used to modulate the waveguide-frequency carriers. In the VLA block diagrams the local oscillator involved is part of the Slave L.O. (antenna) and consists of a 2-4 GHz YIG tuned oscillator that is locked to harmonics of the standard 50 MHz. The 100 kHz synthesizer output is added to 10 MHz and the resultant 10.1 MHz is selected using a crystal filter and is used as an IF reference in the phase lock loop of the 2-4 GHz oscillator.

7. PHASE-FREQUENCY CHARACTERISTICS OF THE CRYSTAL FILTER

The slope of the phase characteristic of the crystal must not be too great or phase errors can result from the frequency offset introduced for fringe rotation and from temperature changes that shift the center frequency of the filter. Consider first the fringe frequency offset of the oscillator. The natural fringe frequency given by eqn. 1 can also be written

$$f_n = \omega_o \, u \cos \delta \qquad (3)$$

where u is the (u,v)-plane coordinate of antenna spacing parallel to the east-west direction of the sky. Suppose that the filter phase slope, α radians Hz^{-1}, introduces a phase error $\alpha f_n = \alpha \omega_o u \cos \delta$ to the measured fringe visibility when a source is mapped. This is equivalent to multiplying the visibility $\exp (i \alpha \omega_o u \cos \delta)$ which after Fourier transformation results in a shift of the map coordinates in the east-west direction of $\alpha \omega_o \cos \delta/2\pi = 2.39\alpha$ arc sec for $\cos \delta = 1$. If this shift is not to exceed 10^{-3} arc sec, α must be less than 4.2×10^{-4} radians Hz^{-1}. For a 4-pole filter the phase slope is roughly 2π radians per half-power bandwidth*, so the requirement becomes that the filter bandwidth not be less than 15 kHz. Usual observing procedures will involve calibration obserations to recalibrate the instrumental phase at various times during a mapping observation, so the above effect will be reduced and may result more in a broadening of the beam than in a shift of its position.

Temperature effects on the crystal filter put a similar lower limit on its bandwidth. If β is the temperature coefficient of the resonant frequency, f_r, a temperature change ΔT will shift the frequency response by $\beta f_r \Delta T$ and introduce a phase change $\alpha\beta f_r \Delta T$. Taking $\Delta T = 5°C$, $\beta = 10^{-6}$ per °C and $f_r = 10$ MHz, α must not exceed 3.5×10^{-4} radians Hz^{-1} if the phase shift is not to exceed 1°, which corresponds to a minimum bandwidth of 18 kHz. Tests of the Peizo Technology crystal filter mentioned in Section 6 for which $f_r = 67$ MHz showed a mean value of β of 5×10^{-7} from 18 to 23°C, and $<2 \times 10^{-7}$ from 23 to 29°C.

A bandwidth specification of 20 kHz minimum for the 10.1 MHz filter should therefore reduce both the above effects to within tolerable limits.

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*See, for example, Figure 4.41 of the Handbook for Electrical Filters published by White Electromagnetics, Inc., Rockville, Maryland, 1963.

8. MECHANICAL ARRANGEMENT OF THE COMPONENTS

The frequency synthesizer and the serial to parallel data converters for communication with the Monitor and Control system are all located on one wire-wrap board of overall dimensions 7-1/2" x 6-1/4". The mixer, crystal filter and various amplifiers for the 50 MHz and 10 MHz signals are mounted on a printed circuit board in a shielded box. Both boards are contained in a single-width VLA module, type 1SA. At each antenna four fringe rotator modules and four 2-4 GHz oscillator modules will be mounted in one bin in the LO/IF rack (rack A of VLA E.M. #123).

ACKNOWLEDGEMENTS

A frequency-synthesizer type of fringe rotator was devised by B. G. Clark and built by R. Hallman for the Green Bank interferometer, and the present system is a further development of that scheme. Numerous ideas and much information have been contributed by A. M. Shalloway. Summer student T. W. Leonard built and tested the single-sideband suppressed carrier mixer mentioned in Section 6. A breadboard version of the synthesizer was constructed by C. Broadwell. C. R. Pace has constructed the prototype synthesizer board and designed a test unit for it to simulate the data output of the Monitor and Control system.

REFERENCES

Hanbury-Brown, R., Palmer, H.P., and Thompson, A.R., 1955, "A Rotating-Lobe Interferometer and Its Application to Radio Astronomy", Phil. Mag., 46, 857.

Little, A.G., and Payne-Scott, R., 1951, Aust. J. Sci. Res. A, 4, 489.

Swenson, G.W. and Mathur, N.C., Proc. IEEE, 56, 2114, 1968.

APPENDIX 1

Fitting a Linear Phase Shift to the Fringe Phase Function

The phase of the signal arriving at an antenna leads that of the signal at the reference point by (see, for example, Swenson and Mathur, 1968, eqn. 56)

$$\phi(H) = 2\pi D\,[\sin\delta \sin d + \cos\delta \cos d \cos(H-h)] \qquad (A1)$$

where the symbols are as defined in Section 2. We now consider a short time interval from $H = H_o$ to $H = H_o + H_1$ and determine the linear phase function with the least rms deviation from the fringe phase. If ΔH represents hour angle measured from H_o we have

$$\phi(H_o + \Delta H) = 2\pi D\,[\sin d \sin\delta + \cos d \cos\delta \cos(H_o-h) \cos\Delta H - \cos d \cos\delta \sin(H_o-h) \sin\Delta H] \qquad (A2)$$

If we put

$$\sin\delta \sin d = A$$

$$\cos\delta \cos d \cos(H_o-h) = B$$

$$\cos\delta \cos d \sin(H_o-h) = C$$

and use the series expansions for cos ΔH and sin ΔH eqn (A2) becomes

$$\phi(H_o + \Delta H) = 2\pi D\,[A + B - C\Delta H - B\Delta H^2/2 + C\Delta H^3/6 + \cdots\cdot] \qquad (A3)$$

Since the fringe rotators are reset at intervals of a few seconds ΔH does not exceed $\sim 10^{-3}$ radians and terms in ΔH^3 and higher powers can be neglected. The problem therefore becomes that of fitting a straight line to a section of a parabola.

For the parabola

$$y = P + Qx^2$$

the straight line with minimum rms deviation between $x = 0$ and $x = x_1$ is

$$y = P + Qx_1 x - Qx_1^2/6$$

and the rms deviation of the y coordinate is $Qx_1^2/\sqrt{180}$. So for equation (A3) the best linear approximation is

$$\phi(H_o + \Delta H) = 2\pi D \left[A + B + BH_1^2/12 - (C + BH_1/2)\ \Delta H\right] \qquad (A4)$$

and the rms deviation of the phase in radians is

$$\pi D \cos d \cos \delta \cos (H_o - h)\ H_1^2/\sqrt{180} \qquad (A5)$$

The maximum deviation is found for antennas at the ends of the SE or SW arms for which $D = 1.68 \times 10^6$ at 24 GHz observing frequency and $\cos d = 0.91°$. Then for $\delta = 0°$ and $H_o = h$, (A5) becomes $2.05 \times 10^7\ H_1^2$ degrees which is equal to 10.8° for $H_1 = 10s$ or 0.7° for $H_1 = 2.5s$. For the fringe pattern formed by a pair of antennas two fringe rotators are involved for which the combined rms deviation must be considered. A limit 1° on the rms deviation for any antenna pair therefore requires that with the largest configuration and 24 GHz observing frequency the fringe rotators must be reset at intervals not greater than 2.5s.

APPENDIX 2

Determination of the Frequency Offset and Initial Phase Settings

The phase lock loop of the 2-4 GHz L.O. makes use of both high lock and low-lock conditions in order to reduce the frequency intervals between the lock points. (A high lock is one where the locked oscillator frequency is 10.1 MHz higher than the S-band reference plus the appropriate 50 MHz harmonic, and a low lock is one where the oscillator frequency is 10.1 MHz lower than the same combination of frequencies.) In the high lock condition the phase of the output waveform of the fringe frequency synthesizer is added to the phase of the received signals and in the low lock condition it is subtracted.

First consider the fringe rotator settings for the high lock case. We want to decrease the signal phase by an amount equal to the lead resulting from the natural fringes for which we use the linearized approximation of equation (A4). Thus the required initial phase, in modulo 2π form, is

$$-2\pi\ D(A + B + BH_1^2/12) \tag{A6}$$

To obtain the required phase number n_p from (A6) add or subtract integral multiples of 2π until the remainder lies between 0 and 2π and then multiply by $500/2\pi$. Expression (2) indicates how the required bit values are related to n_p. The frequency offset is

$$\frac{\omega_o}{2\pi}\ \frac{d\phi}{dH} = -\omega_o\ D(C + BH_1^2/2) \tag{A7}$$

where ω_o is the rotation velocity of the earth in radians s^{-1}. The required 18 bits for setting the rate multiplier are obtained by multiplying (A7) by $2^{18}/500$ and expressing the nearest integer as an 18 bit binary number. If $\frac{d\phi}{dH}$ is positive the phase lead at the antenna is increasing with time and we must decrease the oscillator frequency to cancel this effect. Thus if (A7) is positive the sign-of-rate bit should have value 0, and if (A7) is negative it should have value 1.

In the low lock case the initial phase is equal to 2π minus that for the high lock and the sign-of-rate bit takes the alternate value.

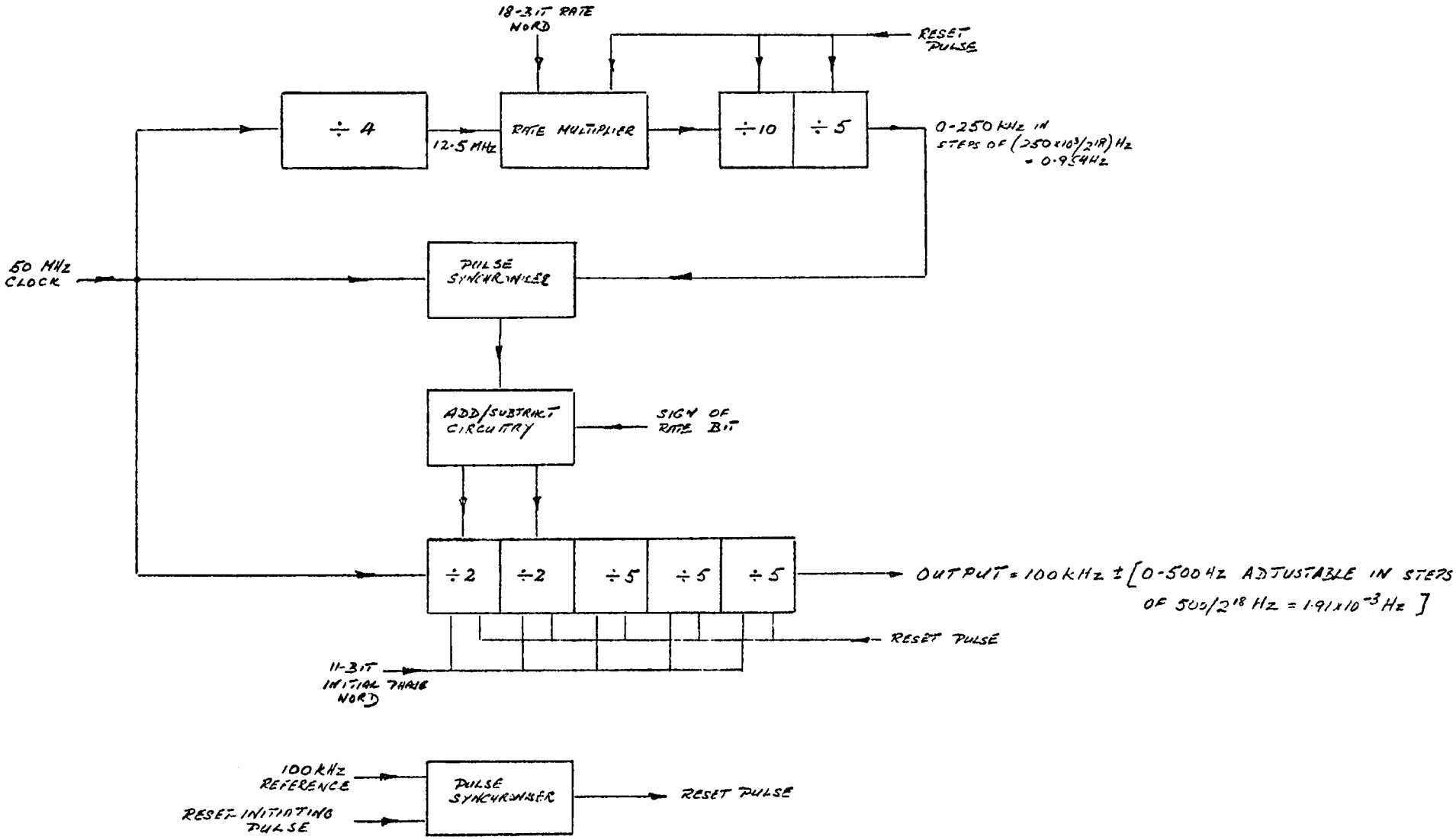

FIG 1. THE VLA FRINGE-FREQUENCY SYNTHESISER.

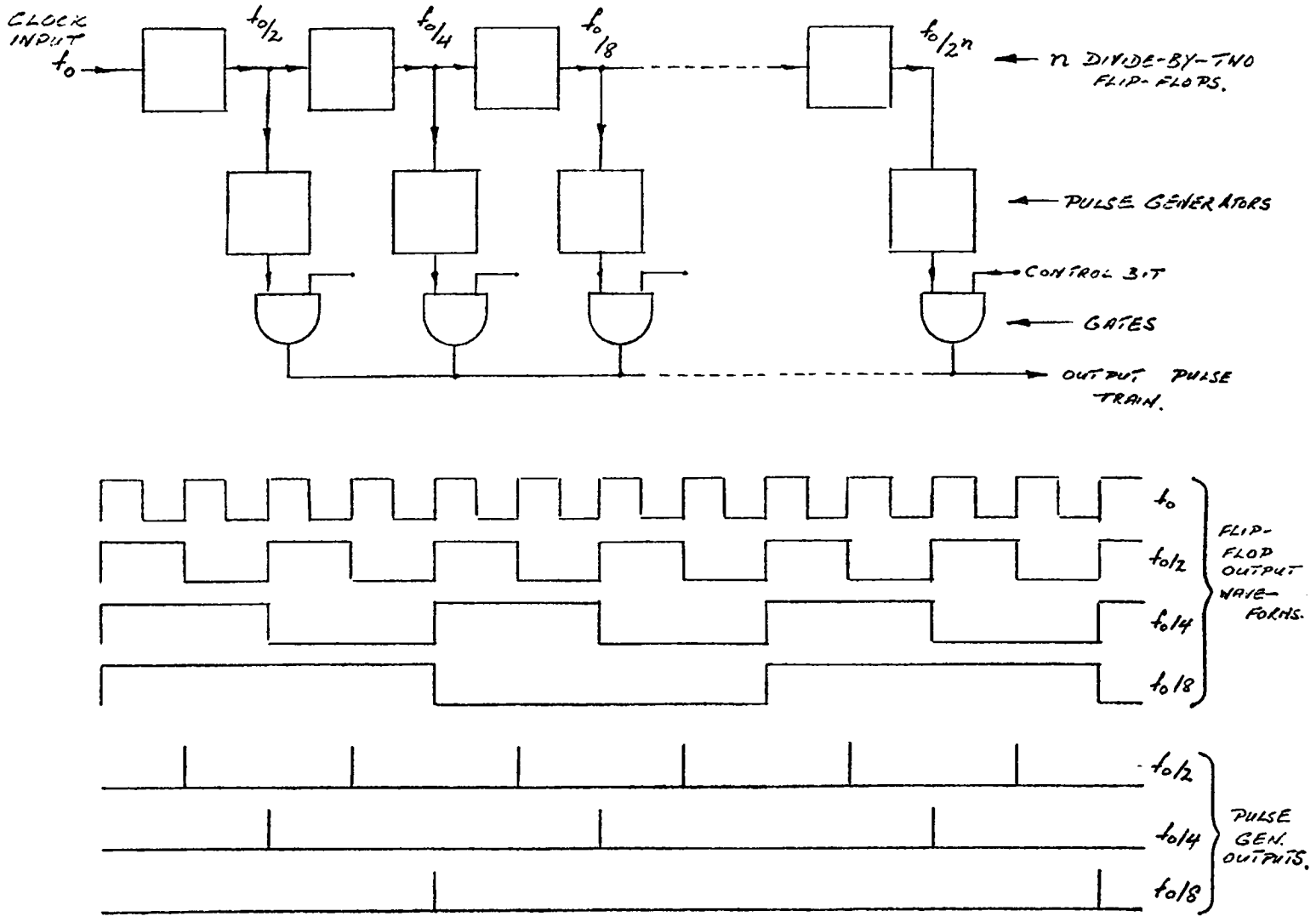

FIG. 2(a) OPERATING PRICIPLES OF THE RATE MULTIPLIER.

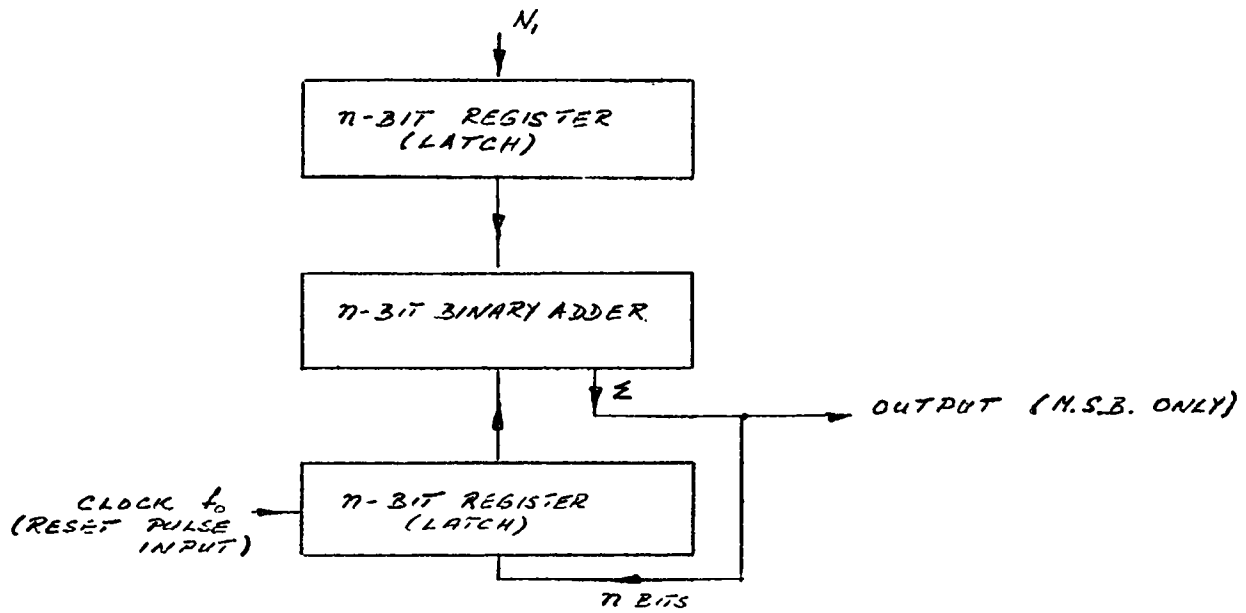

FIG. 2(b) ALTERNATIVE VARIABLE-FREQUENCY GENERATOR.

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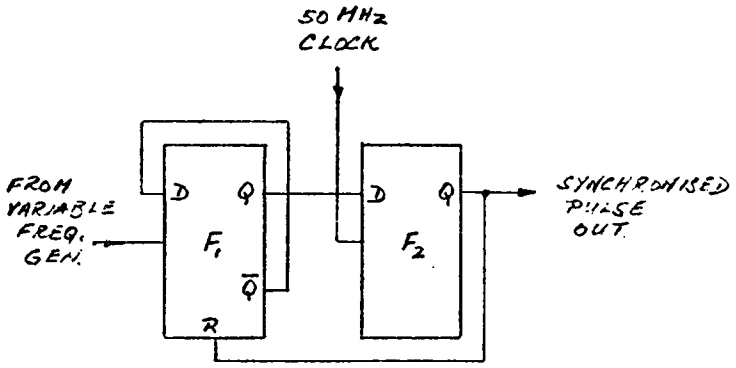
VLA E.M. #124



F_1, F_2 D-TYPE FLIP-FLOPS. (10131)

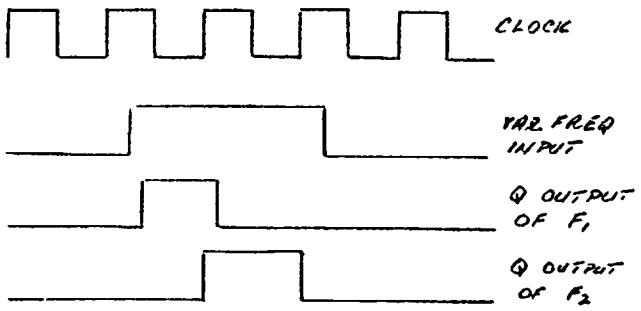
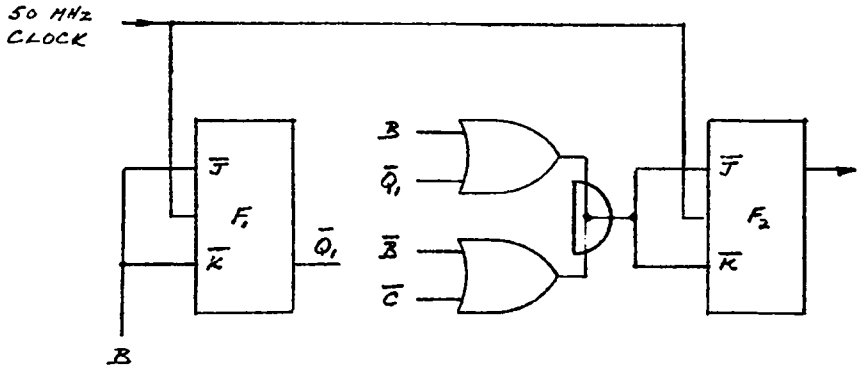


FIG. 3(a) OPERATION OF PULSE SYNCHRONISER.



F_1, F_2 J-K FLIP-FLOPS (10135)

B = OUTPUT OF PULSE SYNCHRONISER

C = SIGN-OF-RATE BIT (HIGH FOR INCREASED COUNT RATE).

B	C	Q_1	F_1	F_2
0	X	1	Y	Y
1	1	X	N	Y
1	0	X	N	N
0	X	0	Y	N

Y, N (YES, NO) INDICATES WHETHER FLIP FLOPS COUNT ON NEXT CLOCK PULSE.

FIG. 3(b) OPERATION OF FIRST TWO COUNTER STAGES.

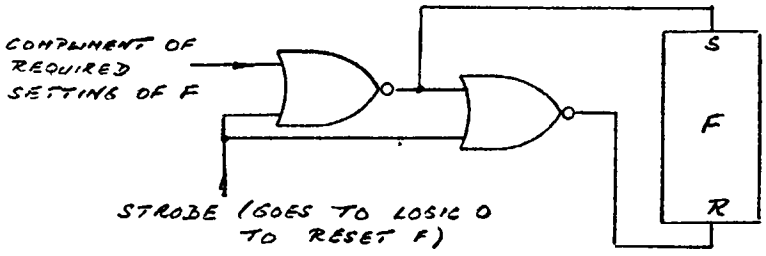


FIG. 3(c) SETTING OF LOGIC LEVELS OF FIRST TWO COUNTER STAGES.