NATIONAL RADIO ASTRONOMY OBSERVATORY
VERY LARGE ARRAY PROJECT
CHARLOTTESVILLE, VIRGINIA

VLA ELECTRONICS MEMORANDA #131

October 1975

A COMBINED CONTINUUM AND SPECTRAL LINE DIGITAL DELAY AND MULTIPLIER SYSTEM

Arthur M. Shalloway

I. INTRODUCTION

The following describes a combined continuum-spectral line system which utilizes a maximum amount of the previously designed continuum system. Two previously written references which will be of help in understanding the material contained herein are: 1) VLA Electronics Memo #113 dated May 1973 and 2) VLA Technical Report #16 dated May 1975.

The proposed system operates in the continuum mode exactly as described in references 1 and 2. In the line mode the system is based on what I have termed a "Recirculating Correlator". The original idea was suggested by Alan Rogers and reports on the subject written by G. Papadopoulos and John Ball. The references are:

A Proposed Plan for Millstone Correlator, G. Popadopoulos, Lincoln Laboratory, MIT (DS-3909).

The Harvard Minicorrelator; John A. Ball, IEEE Transactions on Instrumentation and Measurement, Vol. IM-22, No. 2, June 1973, pp.193-196.

Briefly stated, the principle is based on the fact that the incoming sampled data is arriving at a slower rate than the correlator clock. By inserting storage (hereafter called recirculating memory) between the incoming data and the correlator, (N) (C_H) channels (lead-lag channels in the case of cross correlators) can be generated, where N is the ratio of the correlator clock frequency to the sampled data

frequency and C_H are the number of hardware channels available. The recirculating memory consists of two memories of equal size, one is being loaded with sampled data information while the other - which contains previously stored data - is being used to produce $(N)(C_H)$ channels of data. A further description of the recirculator correlator principle will not be given here and the reader is directed to the above references for more details. However, certain principles and design requirements apply to this specific design and these will be explained where necessary in this report.

II. SPECIFICATIONS

The specifications listed here are the result of meetings and studies by a group of engineers, scientists and programmers on the NRAO-VLA project. These specifications are what appear to be the most desirable at the time of this writing.

A. The system will be a modular one, consisting of the following modules:

2 each Sampler modules. Each module - 54 sampler PC (printed circuit) boards, 27 left and 27 right polarization inputs, 50 MHz bandwidth each, output for each input consists of sin and cos (two bits-three levels each). One module per rack.

2 each Delay Line modules. Each module - 108 two-bit delay lines, 216 PC boards, one-bit delay per board. One-half module per rack.

4 each Driver-Multipler-Integrator modules. Each module - 2808 cross multipliers, 216 PC boards, 13 cross multipliers per PC board. Each module - 108 two-bit drivers, and 216 multipliers (these are self-multipliers for the continuum mode - two for each sampled signal, and they are autocorrelators for the line mode). 54 PC boards, 4 one-bit (least or most) drivers per PC board, and 4 multipliers per board.

B. Spectral Line Bandwidth and Channels:

Each module can produce the following number of frequency channels at the given bandwidth:

B.W. In MHz	Frequency Channels	Recirculation Factor	Oversample Factor
50.	4	1	1
25.	8	2	1
12.5	16	4	1
6.25	32	8	1
3.125	64	16	1
1.5625	64	16	1
.78125	64	32	2
.390625	64	64	2
.1953125	64	64	2
.09765625	64	64	2

The sampling rate is the Nyquist rate times the oversample factor. There will be four modules in the final system.

C. Modes of Operation of Final System with Four Modules:

1. Continuum - eight cross multipliers per antenna pair:

   RSxRS LSxLS RCxLC LCxRC

   RSxRC LSxLC RCxLS LCxRS

   Plus two self multipliers (one redundant) for each signal and two sin x cos multipliers per each antenna output. This is identical to the present continuum system design.

2. Spectral Line - cross correlator - RxR OR LxL
   - autocorrelator - R OR L

   Number of channels = 4 times quantity in 1 above

   Usage - maximum resolution

3. Spectral Line - cross correlator - RxR AND LxL
   - autocorrelator R AND L

   Number of channels = 2 times quantity in 1 above for each of the above sets.

3. (cont.)

Usage - a. Separate polarization measurements

b. Add RxR to LxL to increase sensitivity.

4. Spectral Line - cross correlator - RxR AND LxL AND RxL AND LxR

- autocorrelator - R AND L AND L AND R

Number of channels = 1 times quantity in 1 above for each of the above sets

Usage - separate polarization measurements

5. Spectral Line - cross correlator - R'xR' AND R"xR" OR L'xL' AND L"xL"

- autocorrelator - R' AND R" OR L' AND L"

Number of channels = total number is 8 times quantity in 1 above for B.W.'s of 50 MHz through 6.25 MHz, below these bandwidths the same number of channels as in 1.

Usage - maximum resolution at higher bandwidths

NOTE: This produces a ripple in the middle of the band unless the bandwidths are overlapped.

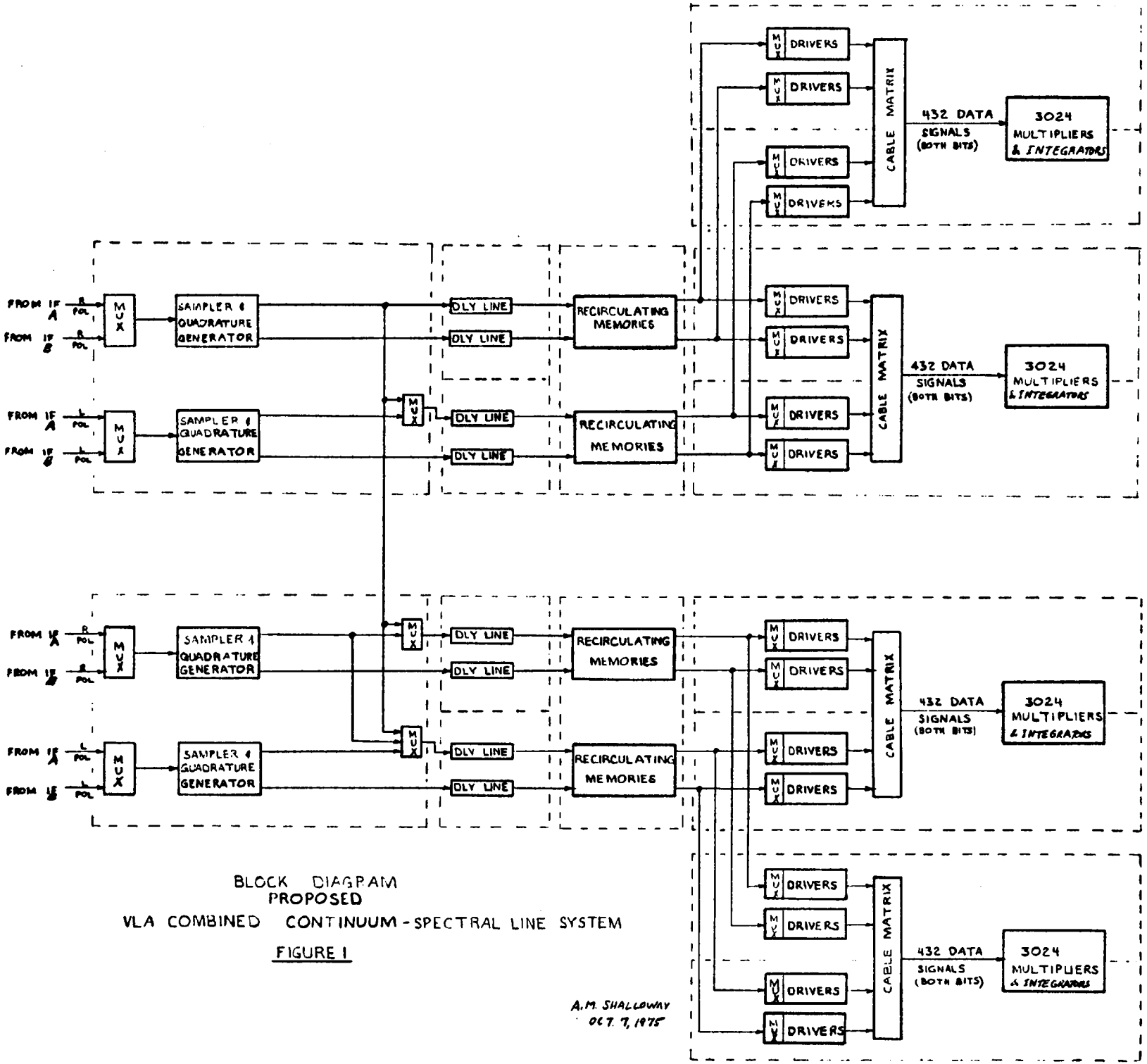
NOTE: In 2 through 5 above these will be a redundant set of autocorrelators. In all of the above there will be 4 operating and 4 spare Vs counters per multiplier rack, 8 per multiplier module.

III. DESCRIPTION

A block diagram of the system is shown in Figure 1. Figure 2 shows pictorially how one module of the system consists of eight hardware channels per cross correlator.

The samplers, delay lines, delay line controls and their associated input and output multiplexer cards and mother boards are unchanged from the continuum system. The multiplier PC boards are fundamentally the same except for the following:

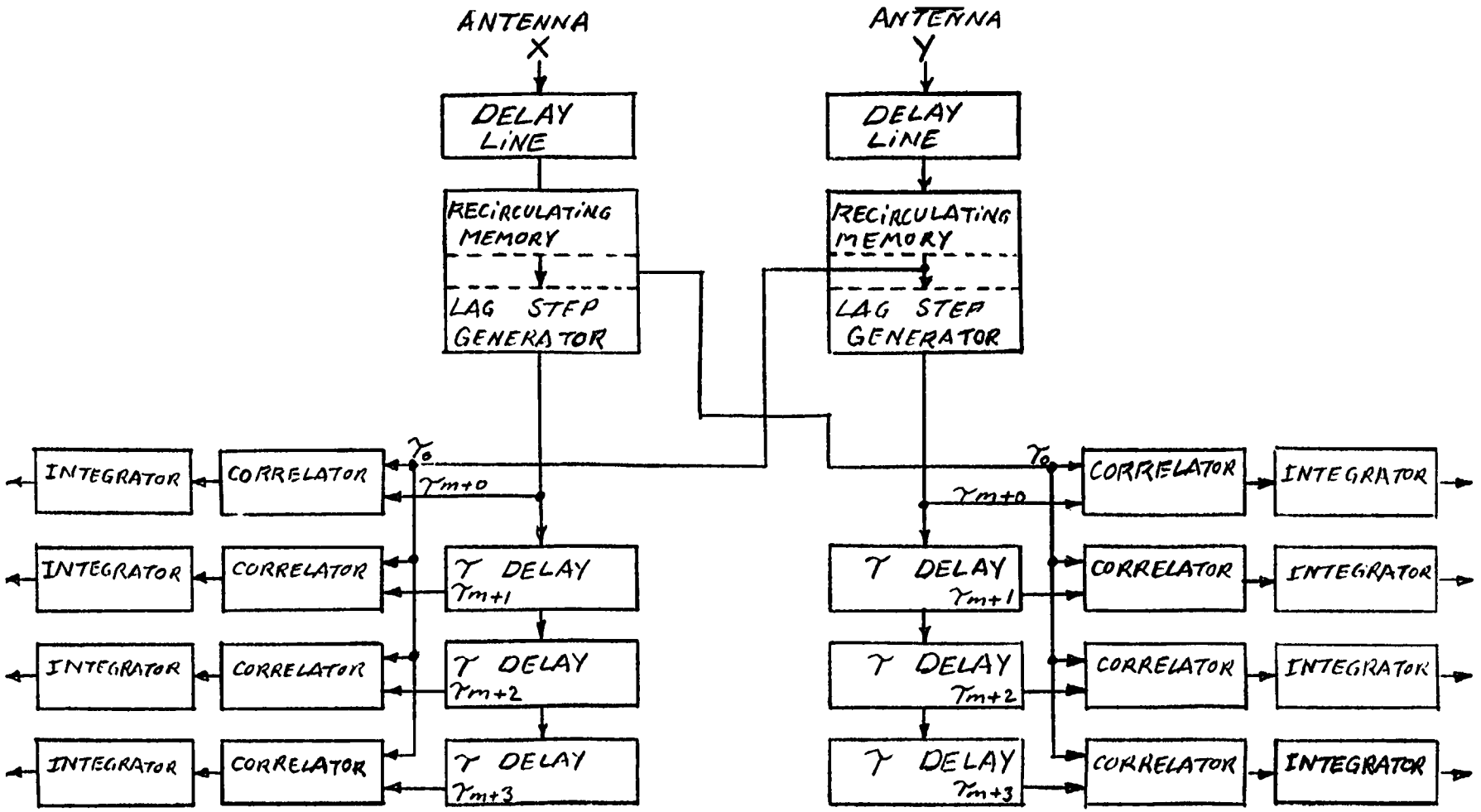
a. Two additional multiplexers are added to save two additional bits from the multiplier accumulators.



BLOCK DIAGRAM
PROPOSED
VLA COMBINED CONTINUUM - SPECTRAL LINE SYSTEM

FIGURE 1

A.M. SHALLOWAY
OCT. 7, 1975



SPECTRAL LINE MODE	VALUE OF m	MODULE
R×R	m = 16K K = all positive integers from 0→15	A1
	m = 16K+4 " " " " " "	A2
	m = 16K+8 " " " " " "	B1
	m = 16K+12 " " " " " "	B2
R×R	m = 8K " " " " " "	A1
	m = 8K+4 " " " " " "	A2
L×L	m = 8K " " " " " "	B1
	m = 8K+4 " " " " " "	B2
R×R L×L R×L L×R	m = 4K " " " " " "	$A_1 A_2 B_1 B_2$
R×R" R'×R' R"×R" R'"×R'"	m = 4K " " " " " " 0→63	" " " "

NOTES ON SYMBOLS:

τ_o = UNDELAYED DATA

τ_{m+n} = DELAYED DATA

WHERE $m = 4K$, K = any integer from 0 to 63

n = any integer from 0 to 3

When IT is not important to separate m & n, $\tau_{m+n} = \tau_L$ (LAG DATA)

A.M. SHALLOWAY
10/28/75

BLOCK DIAGRAM OF HARDWARE CHANNELS WITHIN ONE MODULE

Figure 2

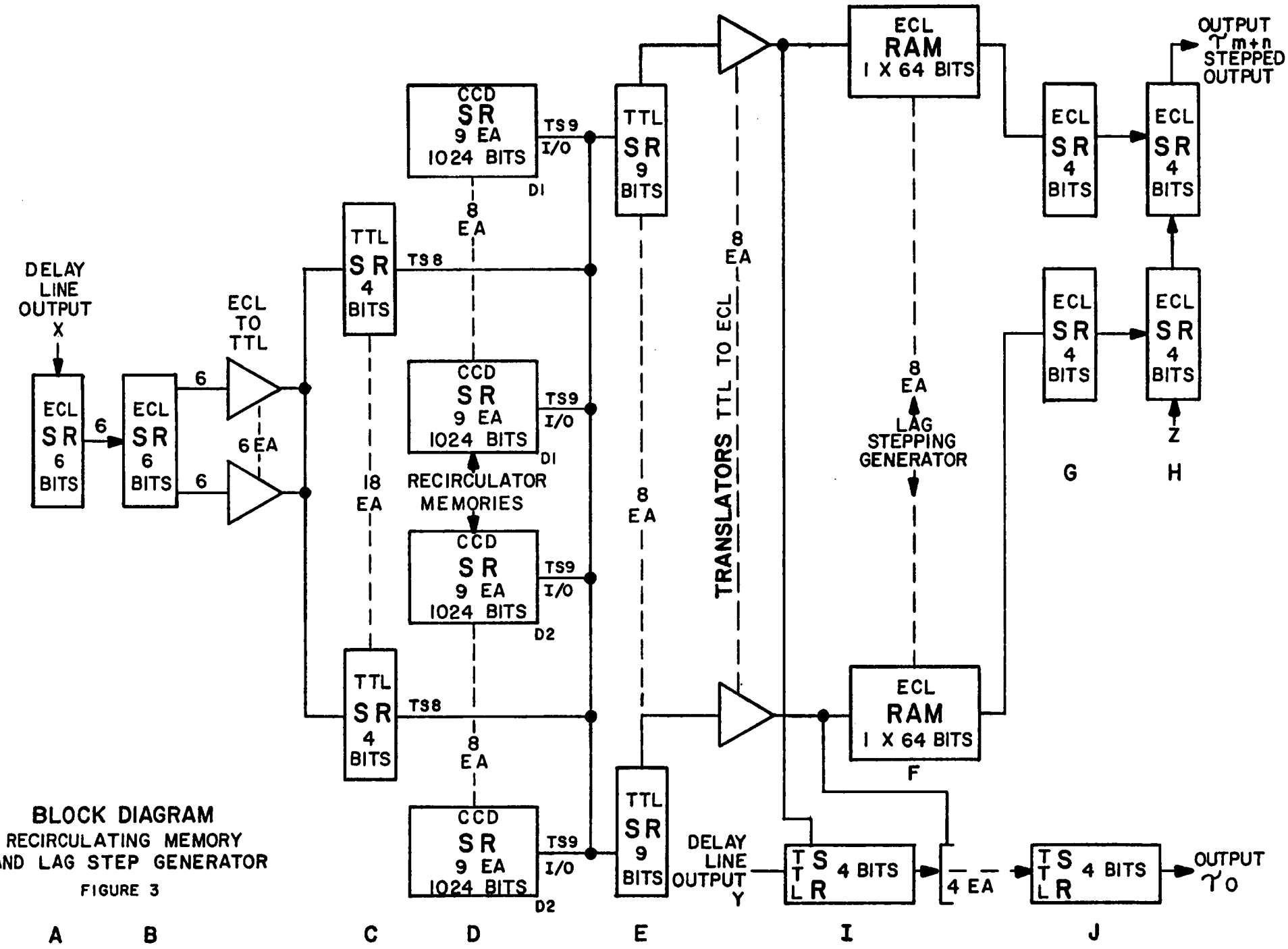
b. The self-multipliers are moved from the multiplier boards to the driver boards where they are used as self-multipliers for continuum work and as autocorrelators for line work.

Two new types of multilayer PC boards are required; the recirculating memory and lag step generator board and the driver board. There are also a set of multiplexers between the IF outputs and the samplers, between the samplers and the delay lines and on the inputs of the driver boards. These multiplexers provide complete flexibility to accomplish all of the modes listed in the specifications.

A block diagram of the recirculating memory representing one of two bits, is shown in Figure 3. In spectral line observations, sampled and delayed signals at frequency rates between 195.3125 kHz and 100 MHz are shifted in at X into a six bit serial shift register, A. The The data is parallel shifted from register A to register B at one-sixth the sampling rate. The data is then translated to TTL logic and parallel shifted - six bits at a time - into a 72 bit register, C. To fill C with data takes 12x6x(sampling rate)μsec. Upon completion of filling C, the data is written into one of the CCD (charge controlled device) shift register memory sets, D1 or D2. Each CCD chip consists of 9 each 1024 bit shift registers. Their inputs and and outputs are common and are tri-state. The shifting from register to register to this point has been to slow down the rate of data to match the input/output rate of the CCD's.

The choice of CCD's to implement the memory rather than RAM's was based on the projected future cost - 0.1¢/bit. The size of the memory is dependent on many factors and in this case two of the factors (memory chip size and speed and synchronous operations) give the same answer which strongly affected the result.

The memory must synchronize into a cycle of the receiving system. In the VLA case we have an integration period of 50.48 ms and a blanking time (called data invalid) of 1.6033··· ms. This is a one cycle period of 52.0833···ms. The data will be dumped from the spectral line system to the on-line computers (Cor A & B) every 10, 20 or 40 sec.,



BLOCK DIAGRAM
RECIRCULATING MEMORY
AND LAG STEP GENERATOR
FIGURE 3

which is every 192, 384 or 768 of the above cycles. It is possible to devise a system in which the portion of memory being loaded is smaller than the portion being unloaded, but because of many constraints, it appears to be less desirable or possibly impossible to use a memory of this type. For maximum flexibility and simplicity, the time to read out the memory to form one set of correlation channels plus the time to dump the correlator accumulators into storage should be a period which divides into the integration time (50.48 ms) to produce a binary number (1, 2, 4, 8, etc.) with a minimum of remainder.

The easiest way to clarify the above is to take as an example, the figures used in this design. Each memory (D1 or D2) is composed of eight CCD chips with 9 input/output wires and (9)(1024)=9216 bits of storage. While D1 is being loaded, D2 is being unloaded and vice versa. Therefore each set of eight CCD's must be able to transfer in or transfer out at a 100 MBit rate. Since D1 or D2 has 72 input/output wires and can read or write at 2 MBit/wire rate, D1 or D2 could operate to (2)(72)=144 MBit rate. This is more than sufficient and allows some safety for set-up time, pulse widths and tri-stating input and output registers.

CCD's are dynamic devices and can only be stopped for a certain maximum amount of time (9.560 μsec.). To go through a memory once takes $\frac{(8)(9216)}{100}$ = 737.28 μsec. This would produce one set of channels and the accumulator must then be dumped into the memory in a time that is short relative to 737.28 μsec in order to keep the efficiency of the system high. Using the presently designed continuum high speed integrators we can dump the accumulators in 20.16 μsec. To accomplish this only requires a small addition to the wire wrap high speed integrator boards. If we stop the integration process a little short, at 723.847 μsec instead of 737.28 μsec and allow 20.20 μsec for dumping, we obtain a cycle time of 744.047 μsec. The VLA electronics operates on a cycle based on 19.2 Hz - 52.0833···ms period, of which 50.48 ms is data valid, and 1.6033···ms is data invalid. The 744.047 μsec cycle time above divides into 52.0833···ms almost exactly 70 times. By proper synchronization of the system with respect to data invalid time we can have 64 of the

memory cycles occur during valid integration time. By making this a binary number we simplify the synchronization as we switch to narrower bandwidths as indicated in Table 1.

The 72 outputs of the recirculating memory are shifted every 720 ns in parallel into registers E. From registers E, eight serial lines feed eight 1x64 word RAM memories F through TTL to ECL translators. These RAMS make up what is called the Lag Stepping Generator. They provide the variable lag delay required for the generation of each set of channels. From the RAM's, the data passes through one shift register (G) in parallel and then into another (H) from which it is serially shifted out to the driver boards which then distribute the signals to the multipliers. The purpose of the two registers on the outputs of the RAM's is to provide a delay resolution of 40 ns. With only one register there would be a resolution of 80 ns, which is determined by the RAM's.

The underlayed output (τ_O) is shifted from the translators feeding the RAM's in parallel into two shift registers (I). From these registers, the data is serially shifted through two more registers (J) - 4 bits each - before being transmitted to the drivers, to provide a delay equal to the minimum delay in the rams so that a τ_{m+n} - where m and n = 0 - equal in delay to τ_O, can be generated. When operating in the continuum mode, the delay lines which are not required in spectral line observations are fed into the rear of shift registers I and passed through registers J from where they go to the driver cards. During continuum, the delay lines which normally feed into X, on the recirculating memories, now feed into Z - the serial input to registers H. This provides a flow through system with wiring minimized. Controls for the recirculating memory cards have not been designed and will require a fair amount of design time. The recirculating memory logic has been fairly completely designed and is available as NRAO-VLA logic drawing number D13830L1.

The delays τ_{m+1}, τ_{m+2} and τ_{m+3} are generated in the drivers by feeding τ_{m+0} through successive flip-flops before they leave the

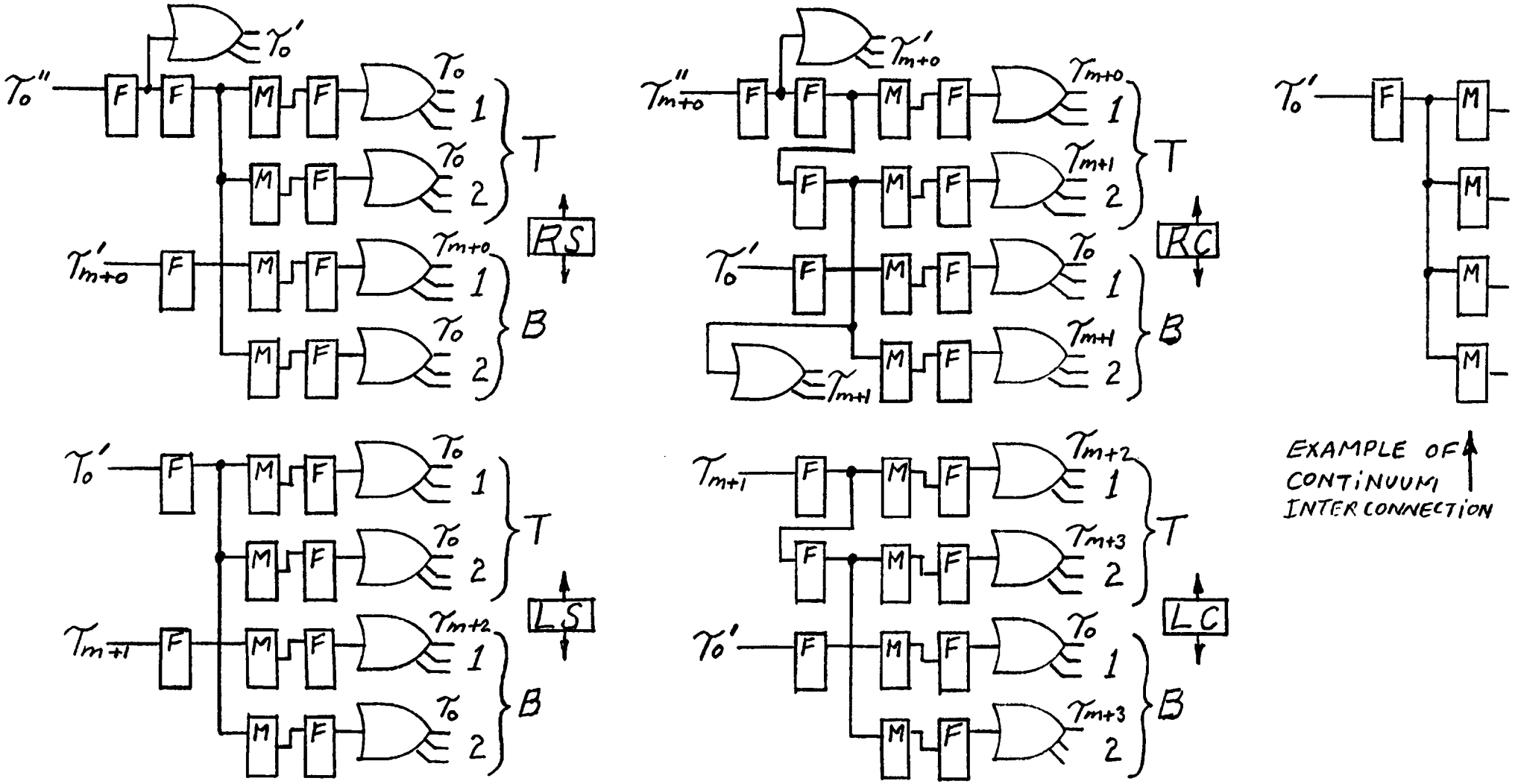
TABLE I

NOTE: Multiplier Clock always = 100 MHz

MHz		Cycles of RM Between D.I.'s	Max. No.	Oversampling	RM Input	RM Redundant
B.W.	S.R.	Data Invalids	of Channels	Factor	Clock	Bits/Sample
50	100	1	16	1	1.388···	0
25	50	2	32	1	.6944···	0
12.5	25	4	64	1	.3472···	0
6.25	12.5	8	128	1	.17361···	0
3.125	6.25	16	256	1	.086805···	0
1.5625	3.125	16	256	1	.0434027···	0
.78125	3.125	32	512 (256 Discarded)	2	.0434027···	1
.390625	1.5625	64	512 (256 Discarded)	2	.0434027···	3
.1953125	1.5625	64	1024 (768 Discarded)	2	.0434027···	7
.09765625	.78125	64	1024 (768 Discarded)	2	.0434027···	15

drivers for the multipliers. Some preliminary layouts of the driver boards have been made, but by no means a complete design. Refer to Figure 4 for a preliminary layout of the drivers for continuum and for one polarization spectral line observation. If the packing density of cables desired is possible, it is proposed that there be four drivers per PC board, 27 PC boards per mother board and rack and thus a total of 216 drivers per module. Each driver is equivalent to the output circuitry of the present delay lines, except that there are two sets of terminated and two sets of bridging outputs, each set with two wires going to multiplier boards. Each of the four sets on one driver can have a different signal coming out. For the various modes of the system, the signal at each driver output is tabulated in Table 2.

A suggested rack layout is shown in Figure 5. Power supplies would have to be external to the rack.



SPECTRAL LINE-ONE POLARIZATION (TABLE 2 COLUMN 3) INTERCONNECTIONS

A.M. SHALLOWAY
10/30/75

LOGIC DIAGRAM-ONE SET OF DRIVERS

Figure 4

TABLE 2

DRIVER OUTPUT TABLE

REFERENCE FOR NOTES BELOW → ① ② ③ ④ ⑤ ⑥ ⑦

	DRIVER	OUTPUT ARRAY		CONTINUUM		SPECTRAL LINE P×P (1)		SPECTRAL LINE R×R (½) AND L×L (½)		SPECTRAL LINE R×R L×L R×L L×R (¼ EA)			SPECTRAL LINE P×P P′×P′ P″×P″ P‴×P‴ (¼ EA)		
1	RS	1	T_1	RS	0	P	0	P	0	R	0		P^N	0	1
2		5	T_2		0		0		0	R	0			0	2
3		1	B_1		0		m+0		m+0	L	m+0			m+0	3
4		8	B_2		0		0		0	L	0			0	4
5															5
6	LS	2	T_1	LS	0	P	0	P	0	R	0		P^N	0	6
7		6	T_2		0		0		0	R	0			0	7
8		2	B_1		0		m+2		m+2	L	m+2			m+2	8
9		7	B_2		0		0		0	L	0			0	9
10															10
11	RC	3	T_1	RC	0	P	m+0	P	m+0	R	m+0		P^N	m+0	11
12		7	T_2		0		m+1		m+1	R	m+1			m+1	12
13		4	B_1		0		0		0	L	0			0	13
14		5	B_2		0		m+1		m+1	L	m+1			m+1	14
15															15
16	LC	4	T_1	LC	0	P	m+2	P	m+2	R	m+2		P^N	m+2	16
17		8	T_2		0		m+3		m+3	R	m+3			m+3	17
18		3	B_1		0		0		0	L	0			0	18
19		6	B_2		0		m+3		m+3	L	m+3			m+3	19
20						↑ X		↑ Y							20

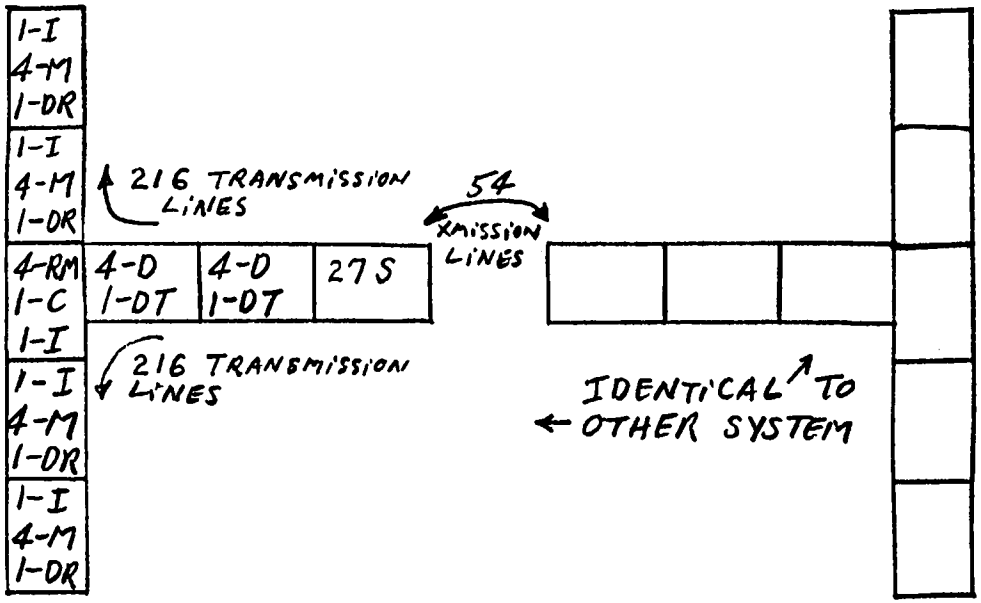
NOTES:

0. X COLUMN REPRESENTS THE POLARIZATION. Y COLUMN REPRESENTS THE DELAY τ (SEE Figure 2). FOR VALUES OF m SEE Figure 2.
1. T_1 & T_2 = TERMINATING OUTPUTS. B_1 & B_2 = BRIDGING OUTPUTS. SEE Figure 4. ARRAY = REFERS TO ARRAY TABLE PAGE 12 OF VLA ELECTRONICS MEMO #113.
3. P CAN BE RS, LS, RC OR LC. WHATEVER P IS, ALL P'S ARE THE SAME.
4. P CAN BE RS OR RC IN MULTIPLIER MODULES A1 AND A2. P CAN BE LS OR LC IN MULTIPLIER MODULES B1 AND B2.
5. R×R MAY BE RS×RS OR RC×RC; L×L MAY BE LS×LS OR LC×LC; R×L MAY BE RS×LS OR RC×LC; L×R MAY BE LS×RS OR LC×RC. R×R AND L×L NEED NOT BE FROM THE SAME SAMPLERS AS R×L AND L×R BUT ARE FROM THE SAME IF AMPLIFIER.
6. P, P′, P″ & P‴ NORMALLY REPRESENT ADJACENT BANDS FROM THE SAME FRONT END, BUT ARE NOT RESTRICTED TO THIS.

A.M. SHALLOWAY
10/27/75

I= INTEGRATORS
M= MULTIPLIERS
DR=DRIVERS
D= DELAYS
DT=DELAY TEST
S= SAMPLERS

NUMBER PRECEEDING ABBREVIATION
INDICATES NUMBER OF
MOTHER BOARDS IN RACK



SCALE: 12" ↔ APPROXIMATELY

VLA CONTINUUM & SPECTRAL SYSTEM
RACK ARRANGEMENT
FIGURE 5

10/3/75
A.M. SHALLOWAY