VARIABLE PHASE SAMPLER

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I. OVERALL DESCRIPTION

The Variable Phase Sampler is the primary A-to-D converter for the IF signals. It is located between the IF Amplifier Modules and the Digital Delay System. Each sampler module contains the circuits to process one 50 MHz IF band. The circuits are contained in a modified, single width module that mounts in a standard bin. Each unit receives an IF signal, a 100 MHz sine wave clock and digital delay data with an associated clock. The outputs consist of a dc leveling control signal, a clock timing test signal and four digital signal outputs. Figure 1 shows a block diagram.

The IF input is fed through a network to develop two signals having a quadrature phase relationship. The two signals are then sampled simultaneously to determine their amplitudes with respect to a positive and negative reference level. The time of sampling is adjustable in 0.625 ns increments over the clock period of 10 ns by command from the System Controller. These out-of-time sampled signals are re-timed in cascaded flip-flops and transmitted to the delay system.

II. VARIABLE PHASE SHIFTER

The 100 MHz sine wave clock input signal is shifted in 22.5 degree increments by a four bit decoded signal. Phase shift command signals come from the System Controller rack in serial form along with a clock. These signals enter an eight bit serial-to-parallel converter and four of the output bits drive a quad op amp used as a diode switch driver. Two converter outputs are used to disable the positive and negative sampler data outputs. Another output inverts sampler output data in synchronism with equivalent switching at the antenna.

The phase shifts are developed in RLC networks for the 22.5°, 45° and 90° steps. The 180° step is obtained from an inverting transformer. See Figure 2. Network switching is done with PIN diodes driven by saturated op amps. Paralleled inductors are used in some circuits to obtain a more accurate valve from standard components. The maximum phase error for the worst case combination of phase settings on any of the first 10 units was 9°. The average of the maximum

errors was 5.5°. Maximum amplitude changes at the shifter output for the worst combinations of phase settings were less than 1 dB. These results were obtained from 10% tolerance inductors, 5% capacitors and resistors without selection of components.

The 100 MHz input level should be +5 to +6 dBm for proper drive to the power amplifier that follows. Space for an attenuator has been provided should a higher input level be furnished. Also on the input is a 50 ohm plug-in phase shift network used in setting timing between the delayed and non-delayed clocks. The voltage gain from input to the collector of the third transistor is about unity. Limiting is detectable in the buffers around +10 dBm in.

III. POWER AMPLIFIER

A three stage amplifier boosts the output of the 100 MHz phase shifter from about +5 dBm to +27 dBm (0.5 W). The first two stages are class A drivers followed by a class C output. See Figure 3. A class C amplifier undergoes drastic impedance changes on its input with drive level sometimes resulting in a snap on and off as drive is varied. Transformer coupling was then used in place of the more common LC matching network to reduce this problem. The power stage output network furnishes about 5 V into a 50 ohm load. At that point a high impedance network removes a small amount of power to develop the delayed clock signal. The network transforms 1.2 K to 75 ohms and feeds a plug-in delay network. The delay is selected for optimum timing of the delayed clock with respect to the sampled signal. Compression in the amplifier limits output amplitude variations to about half the input changes at the nominal 5 V level.

IV. PULSE GENERATOR

The pulse generator consists of a matching network, two snap diodes and two regulated bias supplies. See Figure 4. The network transforms the 50 ohm power amplifier output impedance down to a diode-load combination of about 25 ohms. The diode conduction times; therefore the duty cycle of the output pulse is determined by the bias voltages on the diodes. These voltages are typically +10 V and -1.9 V. The bias supplies for the diodes are op amps with current boost transistors on the outputs. The average pulse is 9.6 V peak and 1.8 ns wide. The load is two equal length 95 ohm cables feeding four sampling gates.

V. LEVELING DETECTOR

The IF input signal of 1.5 V rms is detected by a Schottky diode. The resulting dc level is amplified by two parallel op amps. One is an integrating amplifier which drives a buffer and PIN diode attenuator in the IF Amplifier Module for leveling. The second op amp circuit provides a nominal +5 V output level for monitoring. Level and gain controls permit adjustment of the nominal levels.

VI. QUADRATURE NETWORK

When an IF signal is converted to digital form, more information can be gained by sampling quadrature signal components. These sine-cosine components are generated in an eight pole network designed by J. Granlund of ITT. The network provides a theoretical phase error of less than 0.2° peak from 0.9 to 55 MHz. One voltage source and one inverted current source are required as drivers. See Figure 5. Identical amplifiers are used by incorporating half of the load resistance into the current source. With this arrangement the voltage level on the inverted source side must be twice the level on the non-inverting input. These two-to-one voltage, out-of-phase signals are obtained from the input transformer. The floating secondary winding feeds a 75 ohm coax and termination on the voltage source driver and a 150 ohm coax and termination on the current source side in series. The 150 ohm coax was made by replacing the center conductor of RG 180 B/U, 95 ohm cable with No. 37 wire.

The amplifiers used as network drivers and for isolation on the outputs are cascaded emitter followers with complementary output stages. They are broad band, stable and provide high input impedance with less than 5 ohms output impedance below 50 MHz. Distortion must be held to a very low value to be a negligible contributor to phase error. One percent distortion can produce about 0.6° error. It is most likely to occur at maximum frequency and high level due to slew rate problems in the interstage circuit. These amplifiers were designed to produce harmonics more than 46 dB down at 50 MHz and 1.5 V rms input.

The values of network components were first adjusted on impedance bridges to the calculated values. Allowance was made for shunt capacitance on inductors and capacitance between lands on the p.c. board. Components were measured at a frequency in the range of the components' maximum influence in the circuit when instruments permitted. The instruments used were HP 4271A LCR Meter, Boonton 250A RX Meter, and GR 1608-A Bridge. Use of adjusted components resulted in an average phase error up to 0.5°. With further verification of component values

and compensation for strays, it was evident that some component changes were required. Values were changed on a trial and error basis to remove the phase error. The inductors were then used as standards to adjust additional coils. For capacitors the procedure gave less than consistent results, probably because of using paralleled components. Use of two parallel, fixed capacitors to obtain the right value was abandoned after testing a few boards. A trimmer was added on the back side of the board to allow adjustment. The whole procedure of developing standards and duplicating them was quite laborious. The overall phase error requirement of 0.5° rms across the band is considerably greater than the 0.2° theoretical peak errors, but there are plenty of reasons for the theoretical error to degrade. To name a few, network component temperature coefficient, amplifier flatness variations, non-zero network driving impedance, finite Q's, loading variations and aging. A change of one network component by 0.1% produces approximately 0.1° bump in the phase error curve. It was felt that component values should be set to within 0.1% because changes due to temperature and aging alone could use up all the permissible error.

Phase measurements on prototype circuits and the first 10 boards was done on a point by point basis. Obtaining phase measurements to an accuracy of 0.1° was a job in itself. The first attempt was to calibrate an HP 8405A Vector Voltmeter (VVM) by measuring the frequency of cables at one wavelength and assuming that $\lambda/4$ would be at 1/4 the frequency. This assumption was in error by an intolerable amount. Calibration using cables without a frequency change was done by assembling four equal length cables with male-female connectors, setting the frequency for one wavelength with the cables in series and assuming the average of the four to be 90°. Three sets of cables were made for calibration at 3.4, 15 and 45 MHz. Other errors appeared in the process preventing repeatable readings. It was learned that the frequency of the locked oscillator in the VVM influenced the readings by more than 0.5° at low frequencies. It was necessary to monitor the oscillator to be assured that the lock frequency during measurement was the same as during calibration. Even when the same frequency was used in the two cases, there was some error related to the frequency of lock. This was not troublesome except around 5 MHz where a difference of about 0.1° occurred. Contact resistance on the phase switch also contributed to non-repeatable readings. The VVM was modified to provide a 10 turn pot for phase zeroing and a toggle switch to go directly from 0° to 90°. These changes improved repeatability and reduced somewhat the very laborious job of calibrating and measuring the networks at each of eight frequencies. Adjusting the networks required considerably more time.

The frequencies selected for network measurement are the zero error crossover points on the theoretical curve. It was found by experience that setting these points gave better results than trying to adjust the error peaks to the ideal curve. Figure 6 shows the theoretical curve and the approximate center frequencies where each component has a strong influence. As may be expected, a component change affects a broad range, so there is significant interaction between adjustments. Measurements were made with the VVM attached through 50 ohm terminations to the OSM connectors provided. All networks were measured before the sampling bridges were connected. The average of the absolute value errors measured at the crossover points was 0.12°. A digital phase meter was built by Ray Escoffier during the latter part of the testing phase. This instrument uses the normal digital outputs from the board, thereby including phase errors due to the sampling bridges, comparators, clock timing, and interface problems. The digital measurements showed that error contributions were greater beyond the network output.

The output buffer amplifiers do not hold their low output impedance beyond about 150 MHz. The gating pulses in the bridges fed by these amplifiers have components up to about 2 GHz. Gate leakage pulses can travel unattenuated from one bridge to the other and into the amplifier. This problem was reduced by adding coax delay lines, about 1.5 ns in length, between the amplifier output and each sampler bridge. This gives time for the gating pulses to end before reflections or adjacent bridge leakage arrives at the bridge input. There was evidence of frequency components in the 300 to 500 MHz range traveling through the amplifier and network to the other output but, when reduced, the phase error improvement was disappointing. Overall phase error on the first 10 units seldom exceeded 1° up to about 40 MHz. At 50 MHz four of the 20 curves measured about 1.5° error. An investigation was made of many possible causes of error in the bridge-comparator area. No firm handle was found for controlling the magnitude or shape of the error curves.

VII. SAMPLER

The sampler circuit consists of a diode switch and high speed comparator. See Figure 7. The switch is operated by a 1.8 ns, 100 MHz pulse. The pulse produces a forward current of about 5 mA per diode in the bridge when balanced. During off-times the self biasing circuit develops about 3.2 V reverse bias per diode to prevent the peaks of the 1 V rms noise signal from overriding the switch. Diode capacitance could also transmit an attenuated signal between gate pulses. this feedthru signal is removed by low impedance loading between the

diodes by the self bias circuit. Diodes disconnect the load when the pulse is present. The balance pot has minor affect on comparator operation and will be omitted on future units. Note that a module signal input level of 1.5 V rms is required for 1 V at the sampler because of the reduction in the input transformer. During switch on-time the signal current flows into a 4.7 pF capacitor, the comparator impedance and stray capacitance. During off-time the lumped and stray C's tend to hold the voltage present at the time the switch opens.

The comparator is a Motorola MC 1650L, a very high speed, short delay IC but not sufficiently fast to perform adequately in this application without assistance. The high slew rate of 350 mV/ns is obtained with some sacrifice in overdrive. The Advanced Micro Devices AM 685 requires less overdrive but has a lower slew rate and greater delay time. The circuit is required to detect signal levels above or below 61.2% of the rms signal level within $\pm$ 5%. These and other limits are discussed in VLA Electronics Memoranda Nos. 112 and 114 by A. R. Thompson and B. G. Clark. If the last sample occurred at the peak of a wave and the next sample at the opposite 0.6 V threshold level, the slewing would be 3.6 V in a few nanoseconds. Time must be allowed for the sampler to stabilize and for obtaining the readout. If a step function input were obtained with a holding circuit capable of furnishing the comparator the required input current during slew with less than 5% voltage droop, the total clock period would be required to develop an output. Lower signal level operation would help this problem but would increase inaccuracy due to the resolution or overdrive error.

The comparator need operate only in the region of the threshold level of about 0.6 V, so it may be possible to live with the device limitations and get satisfactory results. The chip has been aided by adding limiting and recovery circuits. The recovery circuit consists of two diodes and a 200 ohm resistor between the signal and reference inputs on the comparator. This circuit discharges the capacitance during gate off-time bringing the signal input voltage to within 250 mV of the reference before the next sample. If the next sample is just across the threshold, the chances of capture are much improved because of the small voltage change. With a starting point voltage near threshold, the driving current requirements are much lower. If the input signal is far from threshold at gate time, it is not necessary to furnish sufficient current to transfer that voltage to the comparator input. Current limiting is provided by controlling the bridge current. With input and output voltages equal, the bridge diodes conduct about 5 mA each. When an unbalance is present the maximum current that will flow into the source and comparator circuit is about 10 mA.

This limit is as much an aid in reducing the driving amplifier requirements as reducing the maximum deviation from threshold.

The diode switch and driving circuit did not come close to ideal operation on the first tests. A large and variable gate leakage pulse appeared at the input to the comparator. The pulse was due to unequal capacitance and forward conduction characteristics in the diodes and a transformer core problem. The diodes originally used were HP 5082-2810's, unmatched. These were replaced with Aertech A2X919 (now known as A2S866) diodes, a batch matched version of the A2S810. Voltage drop is matched to $\pm$ 5 mV at 10 mA and capacitance matched to $\pm$ 0.05 pF at 0 V dc. The matched diodes removed much of the variation in gate leakage, but a pulse of about 120 mV peak remained at the bridge output due to transformer core problems. The original core chosen was a Stackpole 57-0184, C/5N material. A new search was made of many cores on hand and some new samples for a material that would give better balance. Two types were found. Stackpole 57-0915 C/12 material and Ferroxcube K5-050-40/1Z2. The C/12 cores reduced the leakage about 40% and the 1Z2 cores by about 70%. This improvement was not without loss in another characteristic. The reverse voltage on the diodes for 2 or 3 ns following the conduction period was not as great with the new cores. Another consideration is important at this point. The comparator has hysteresis in its transfer characteristic. For dc inputs the data sheet shows a typical value of 15 mV. A controlled amount of gate leakage can be used to overcome the hysteresis. The leakage is affected primarily by core material, gate pulse power, bridge signal source impedance, and capacitance on the output side. For the diode currents and reverse voltage chosen, and the source and load impedances the C/5N core became acceptable by reducing the nominal pulse width somewhat. Assume a test condition with no signal input, gating pulses present and the ability to manually adjust the dc input thru the threshold region. When the leakage pulse is small the comparator output snaps between states as input dc level is varied. If it is excessive, the leakage pulse will cause a complete change of state and return during a clock period. With an optimum level the comparator acts like a crude amplifier having little or no snap on the output but a very crude reproduction of the input with a maximum peak-to-peak value less than the normal logic swing. A minimum 50 MHz signal (5 to 10 mV) properly phased will enhance every other output pulse and suppress the intermediate ones. The delayed clock timing on the following flip-flops is set to capture at the peak of the gate leakage pulse so that maximum sensitivity is obtained.

VIII. DIGITAL RETIMING CIRCUITS

The variable phase shifter decodes a 4-bit digital delay word to shift the sample pulse, in 0.625 ns increments, over the 10 ns sample period. The digital output of the MC1650L comparator will follow the sample pulse time shifting since a logical state change at the comparator output will occur a propagation delay after the sample pulse. The sampler digital outputs, however, must be digitally captured by the delay line input stage working from a 100 MHz clock that is time stable. Thus, the comparator non-synchronous digital outputs must be retimed to interface with the synchronous delay line input.

Retiming is accomplished by capturing half of the time (for sampler phase shift commands 0000 thru 0111) on one edge of the clock and the other half (phase shift commands 1000 thru 1111) on the other edge of the clock.

First, however, the comparator is captured in a flip-flop using a clock that follows the sample pulse. Following sampler No. 1 (cos positive) digital logic string on the sampler schematic, Figure 8, this flip-flop is U8-A. The clock for this IC is a version of the shifted 100 MHz signal, timed for optimum capture timing with a discrete delay circuit. The output for this IC is captured on clock—not in IC U8-B for phase shift commands 0000 thru 0111 or on clock in IC U14-A for phase shift commands 1000 thru 1111. In the first instance, the clock—not flip flop is initially retimed to clock in IC U14-B. IC U18-A selects the path to output flip-flop U20-A via either the U14-A or U14-B routes by steering on the phase shift command MSB (on U18-A pin 7). IC U18-A also allows interchanging the positive and negative outputs. This function un-inverts the signal inverted in the fringe generator and is used to implement the Welsh function phase switches programmed in the system.

A second discrete phase shifter adjusts for optimum timing, for any sampler phase shift command, at the U8-A and U8-B/U14-A interface. This phase shift is selected such that the U8-B hold time for delay 0000, the U8-B set-up time for delay 0111, the U14-A hold time for delay 1000, and the U14-A set-up time for delay 1111 are all about equal. A resolution of about 1 ns in setting this delay means that where exact equality between these four terms cannot be achieved, always select in favor of larger set-up times at the expanse of less hold times.
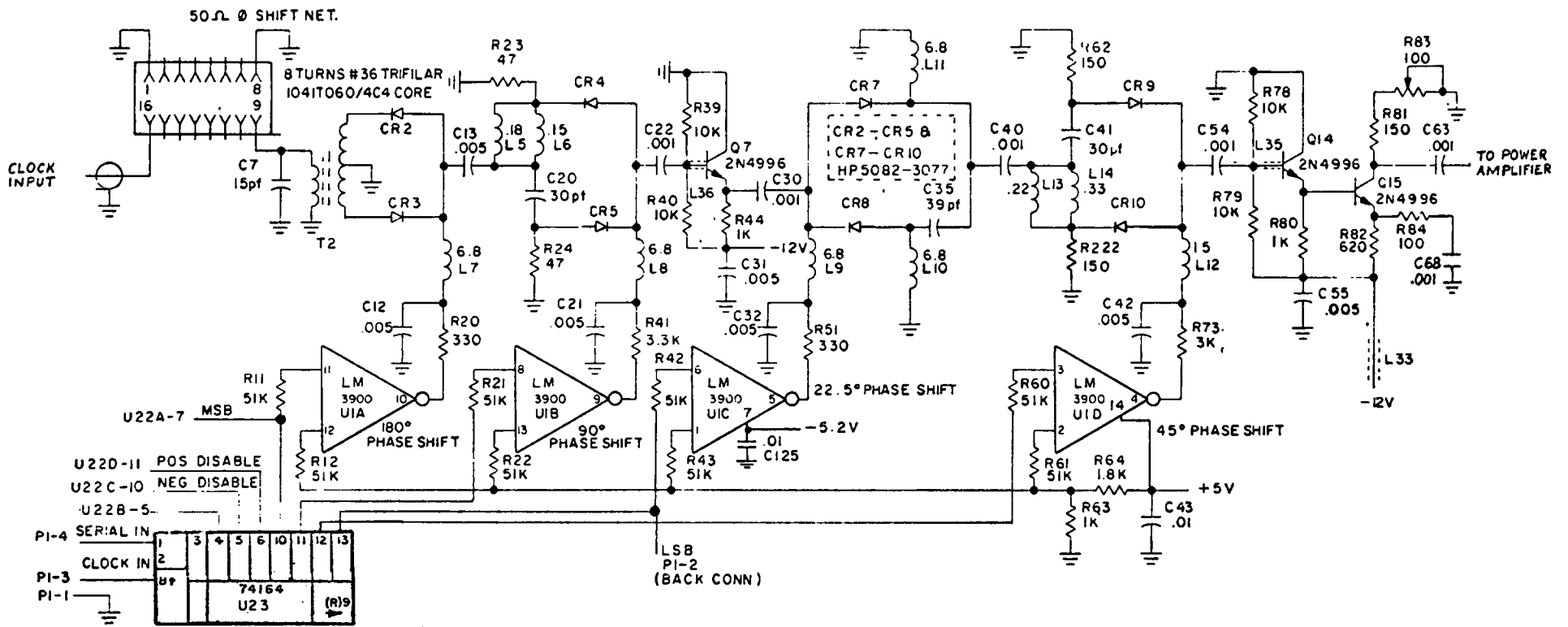
One additional function accomplished in the digital portion of the sampler is sampler disabling. Two digital bits that accompany the 4-bit phase shift command allow both positive or both negative samplers to be disabled (forced to logic 0). This function allows the VLA computer to measure the duty cycle of any sampler digital output since the multiplier system self multiplier integration results can yield duty cycle information of un-disabled sampler outputs.
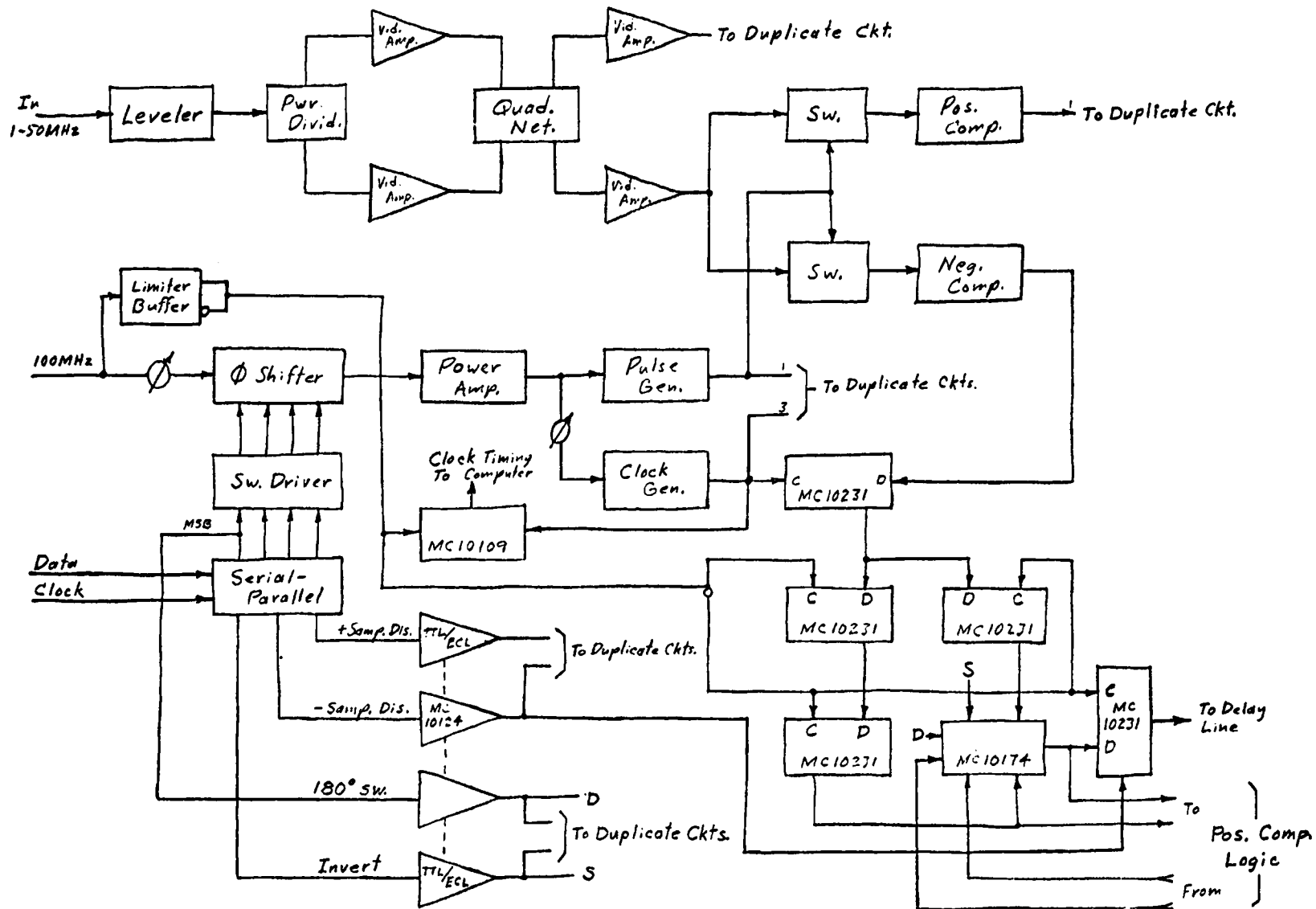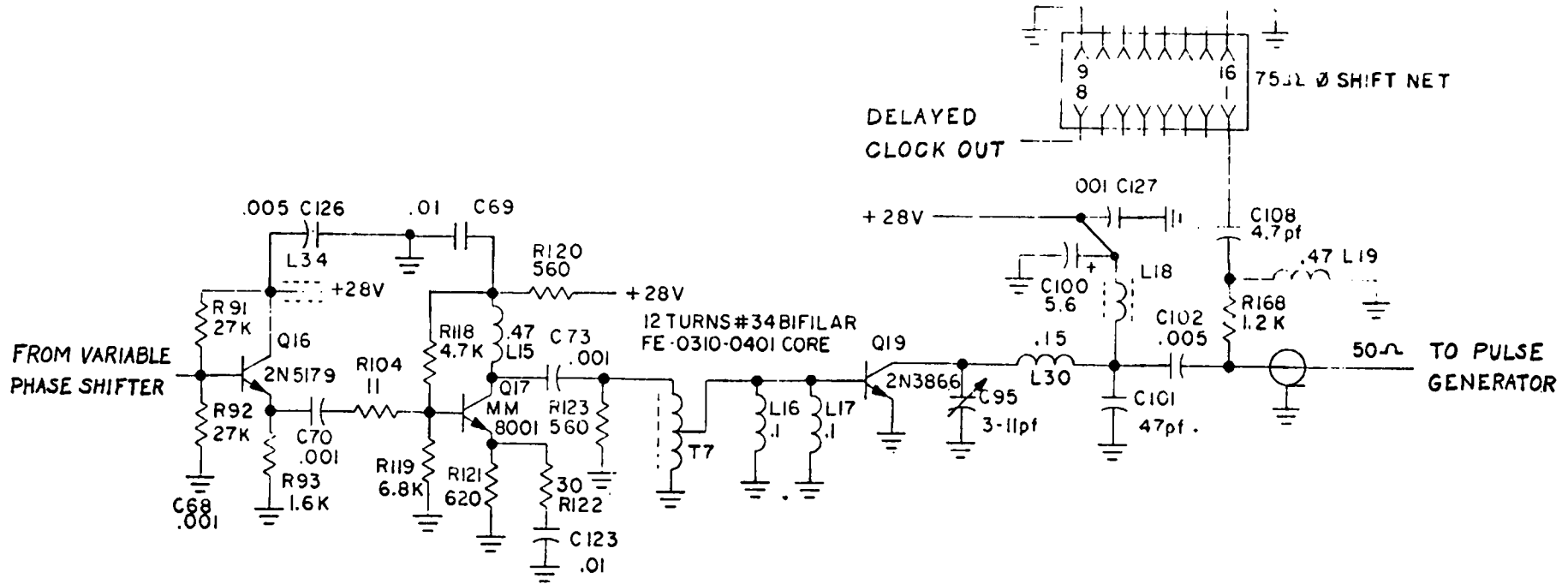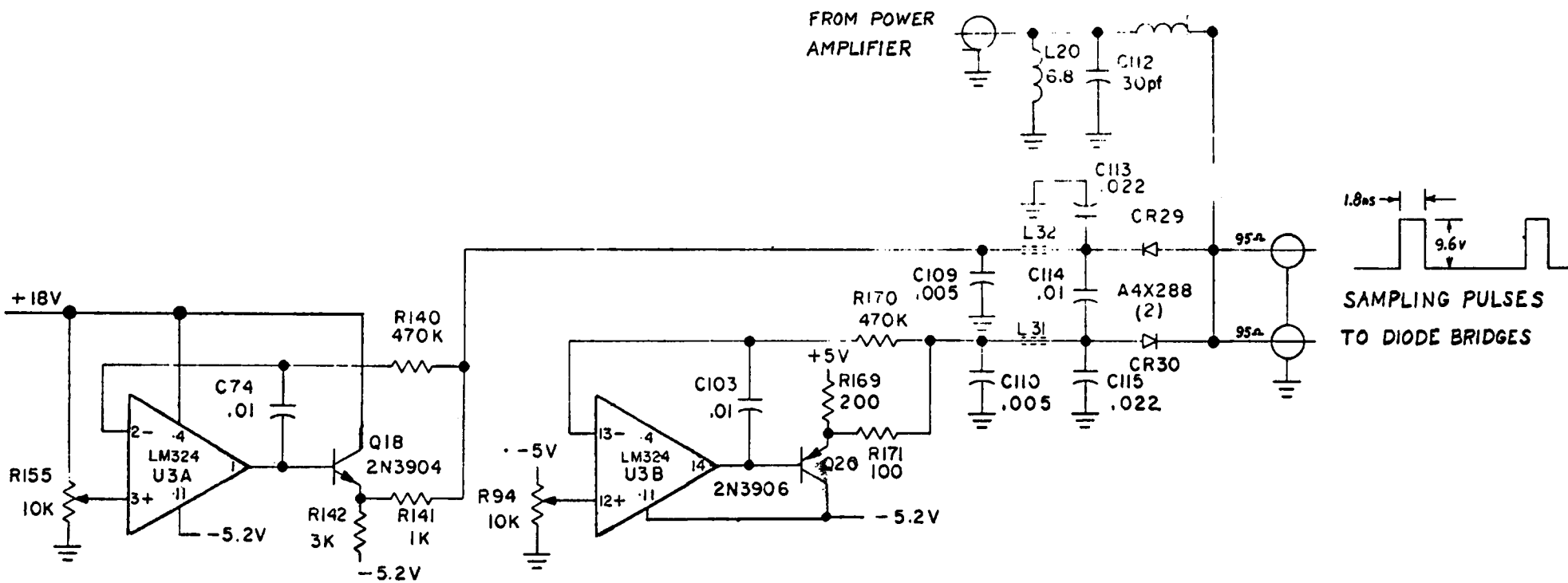
VARIABLE PHASE SAMPLER

FIGURE 1

VARIABLE PHASE SHIFTER

FIGURE 2

POWER AMPLIFIER

FIGURE 3

FROM POWER
AMPLIFIER
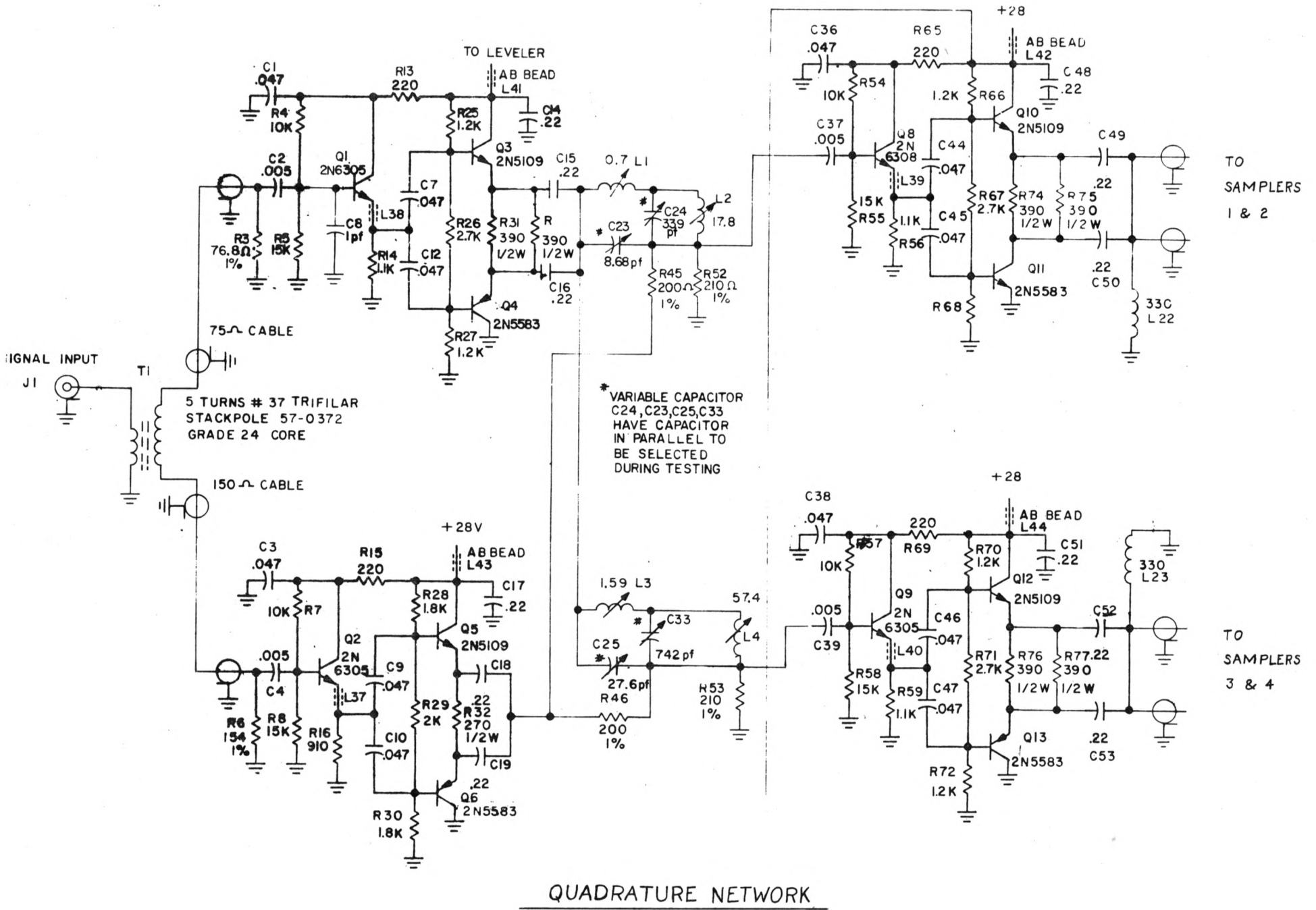
L20
6.8

C112
30pf

C113
.022

L32

CR29

1.8ns

9.6v

SAMPLING PULSES
TO DIODE BRIDGES

+18V

R140
470K

R170
470K

C109
.005

C114
.01

A4X288
(2)

95Ω

95Ω

C74
.01

Q18
2N3904

+5V

C103
.01

R169
200

L31

C110
.005

C115
.022

CR30

R155
10K

2-
LM324
U3A
3+ 11

1

-5.2V

R142
3K

R141
1K

-5.2V

-5V

R94
10K

13-
LM324
U3B
12+ 11

14

Q28
2N3906

R171
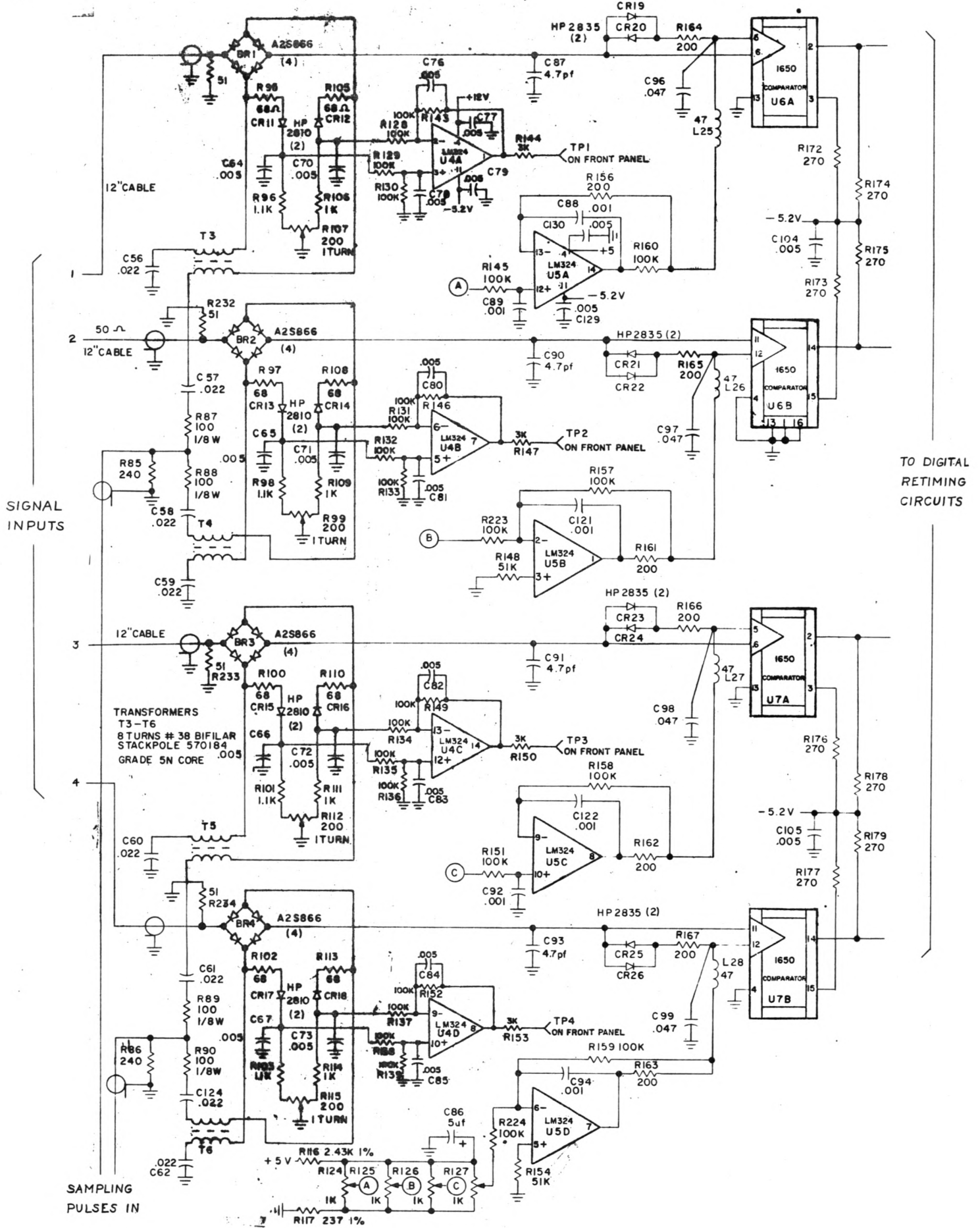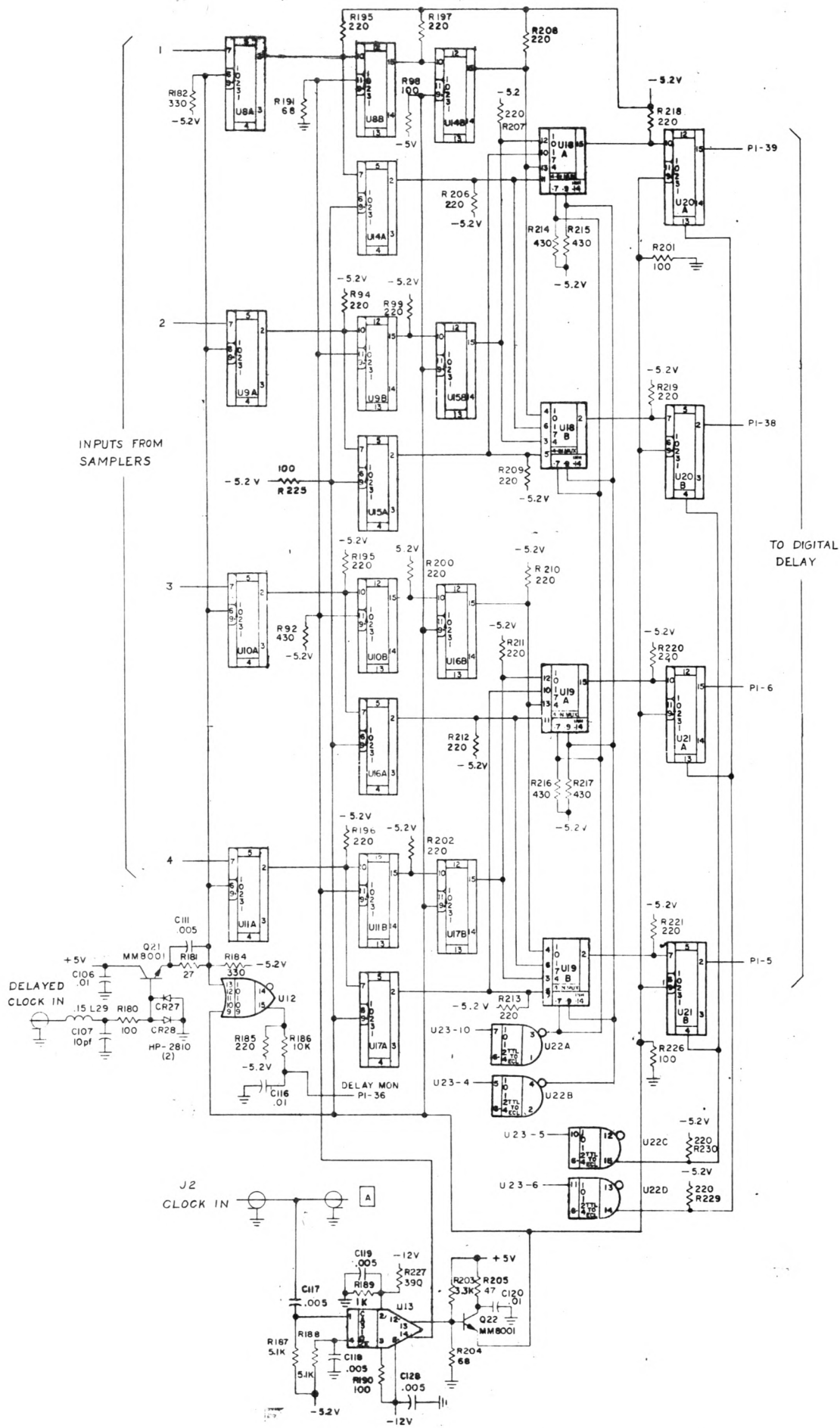100

-5.2V

PULSE GENERATOR

FIGURE 4

QUADRATURE NETWORK
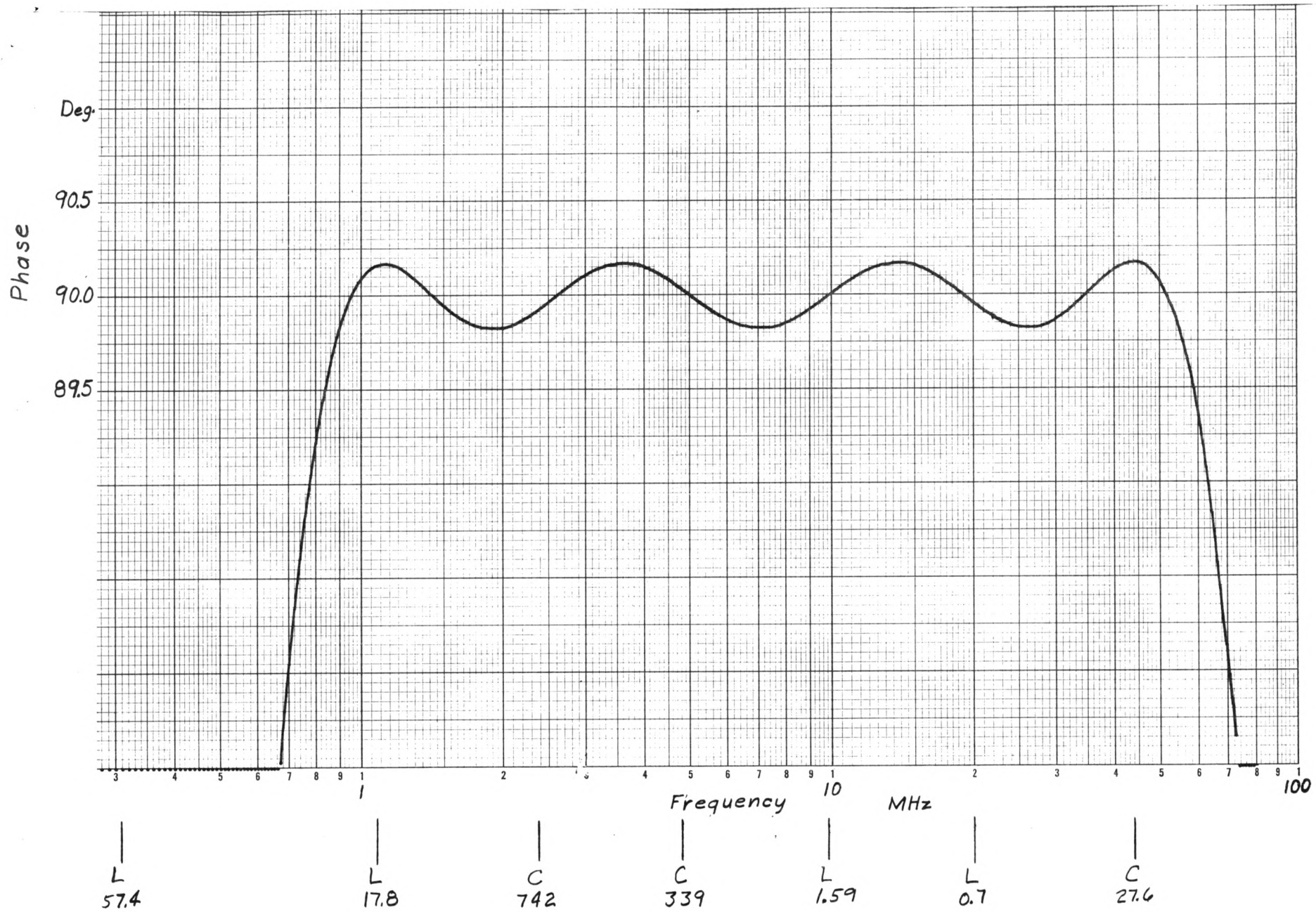
FIGURE 5

FIGURE 6

SAMPLERS

FIGURE 7

DIGITAL RETIMING CIRCUITS

FIGURE 8