NATIONAL RADIO ASTRONOMY OBSERVATORY
VERY LARGE ARRAY PROJECT
SOCORRO, NEW MEXICO

VLA Electronics Memo No.133

THE COMBINED CONTINUUM - SPECTRAL LINE DIGITAL DELAY AND MULTIPLIER SYSTEM

Ray Escoffier

February 20, 1976

I. INTRODUCTION

This report covers the latest design of the combined continuum - spectral line digital delay and multiplier system. This system was designed using technology and techniques utilized in the present continuum delay - multiplier design. Emphasis in this memo will be placed on the operational characteristics of the system and areas of change from the continuum system. The System Controller, which will be developed in Charlottesville by A. M. Shalloway, will not be discussed here.

II. THE COMBINED SYSTEM

Five operational modes have been specified for the combined system with the system configuration for each mode illustrated in Figures 1 through 5. These figures display the system on a per-antenna basis reflecting the modular system design. The AC-BD breakdown corresponds with the two independent 50 MHz systems that comprise the present 100 MHz bandwidth continuum system, A, B, C and D being the four front end outputs. In these figures and in later discussion the modular breakdown of a 50 MHz system (say AC) consists of: the sampler module (1 rack), the delay module (1 rack), the recirculator module (1 rack), two multiplier modules (2 racks each - see Figure 6).

FIGURE 1 CONTINUUM MODE

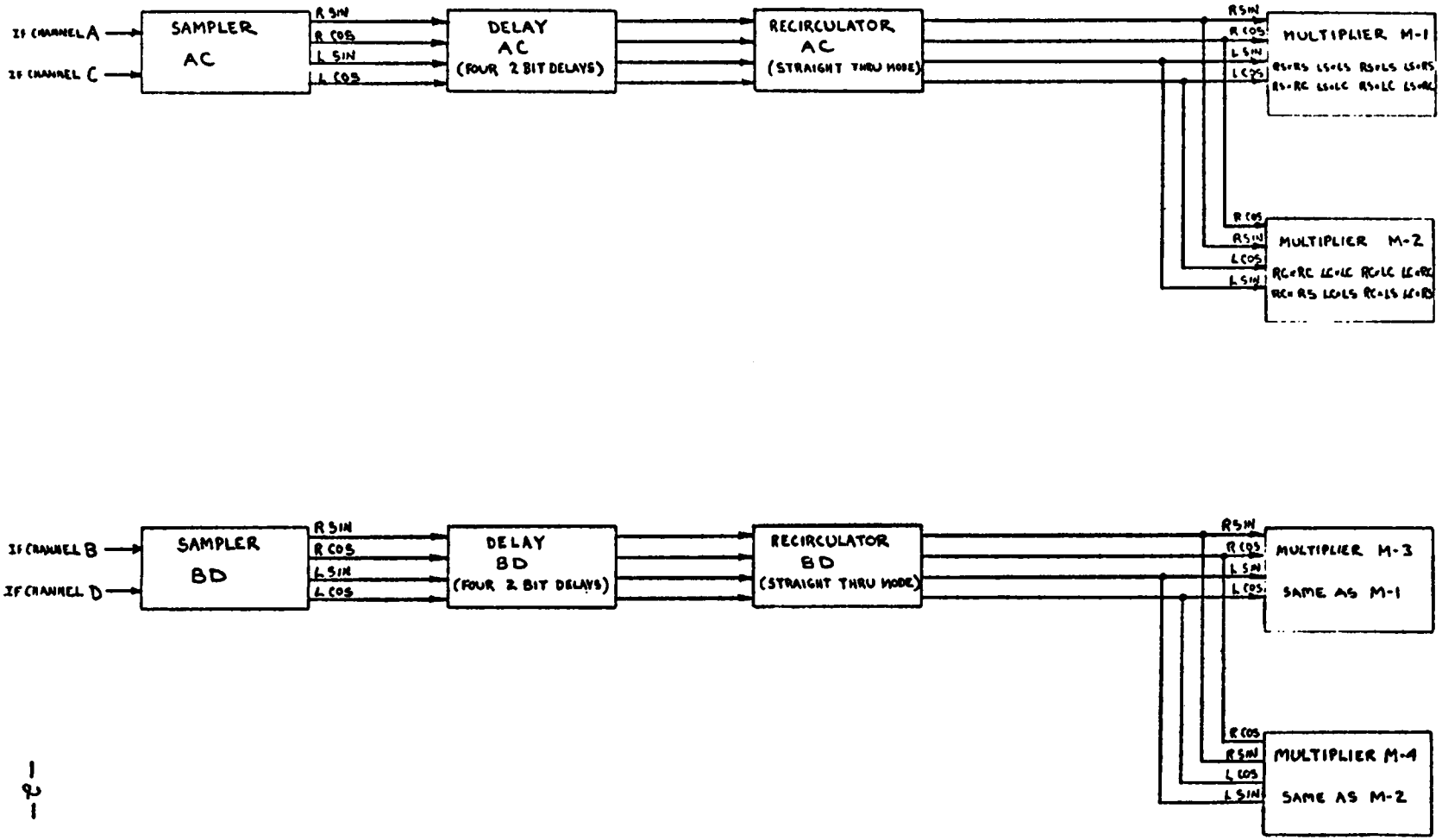
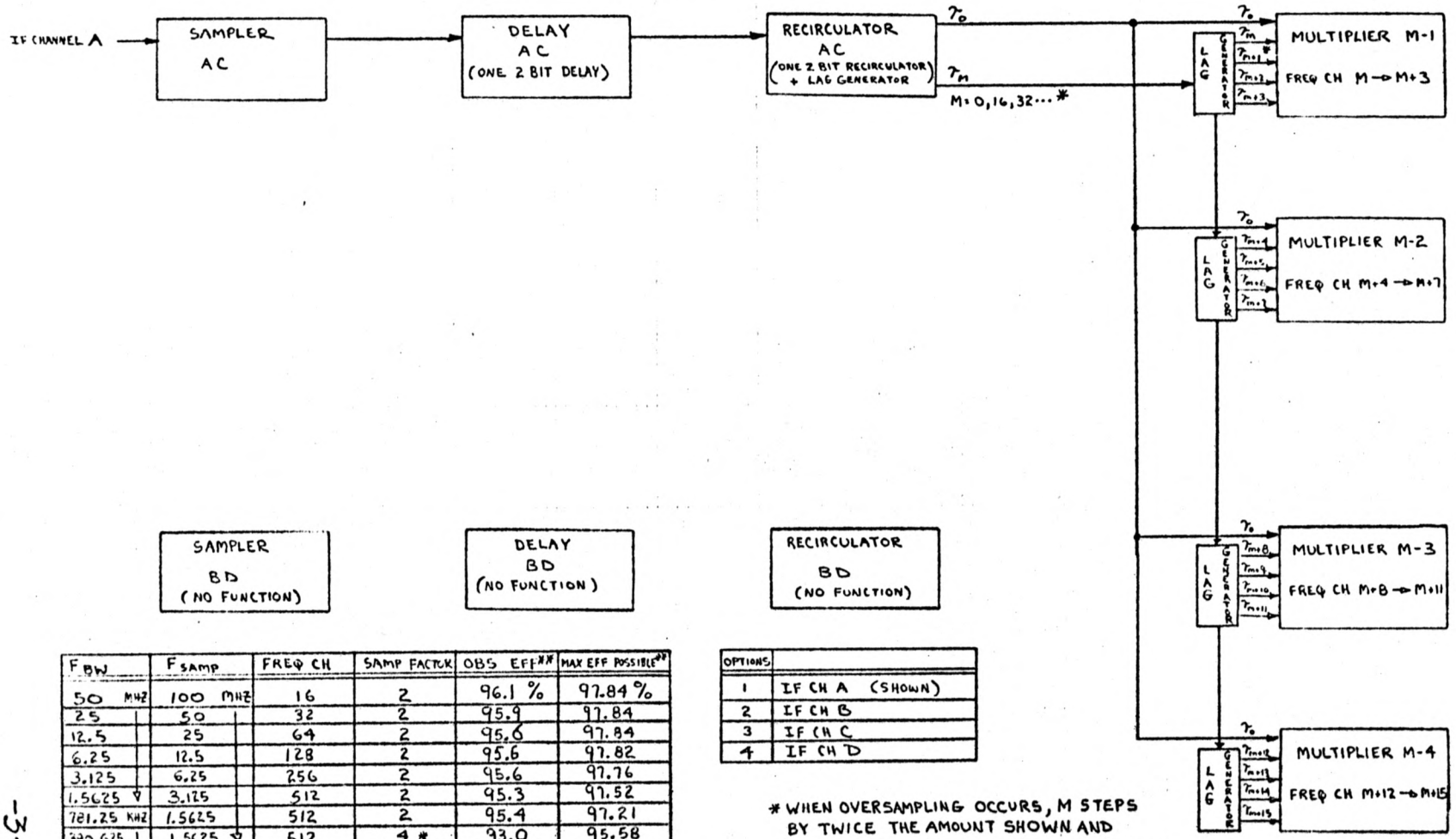


FIGURE 2 SINGLE BAND SPECTRAL LINE MODE



SAMPLER
BD
(NO FUNCTION)

DELAY
BD
(NO FUNCTION)

RECIRCULATOR
BD
(NO FUNCTION)

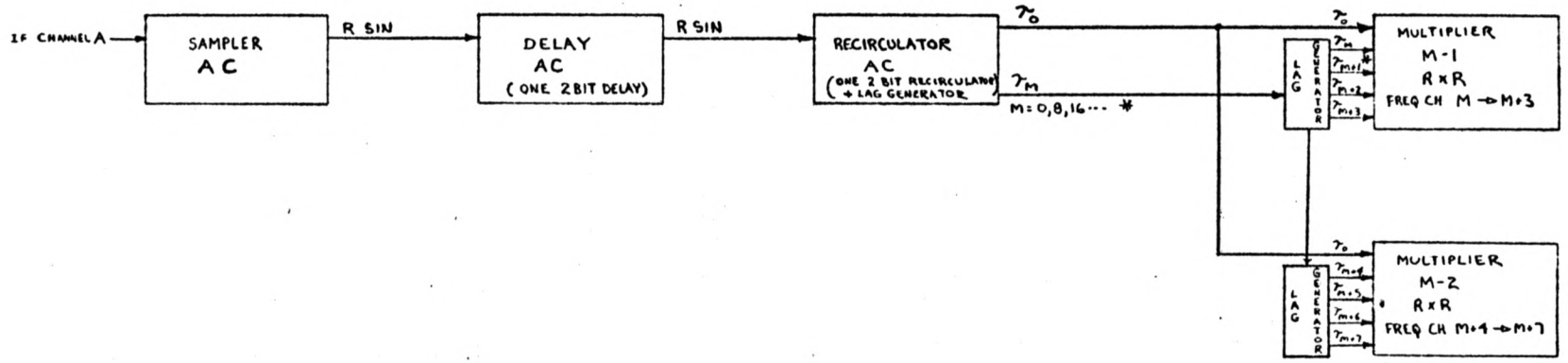
F_{BW}	F_{SAMP}	FREQ CH	SAMP FACTOR	OBS EFF**	MAX EFF POSSIBLE**
50 MHZ	100 MHZ	16	2	96.1 %	97.84 %
25	50	32	2	95.9	97.84
12.5	25	64	2	95.6	97.84
6.25	12.5	128	2	95.6	97.82
3.125	6.25	256	2	95.6	97.76
1.5625 ↓	3.125	512	2	95.3	97.52
781.25 KHZ	1.5625	512	2	95.4	97.21
390.625	1.5625 ↓	512	4 *	93.0	95.58
195.3125	781.25 KHZ	512	4 *	90.1	95.32
97.65625 ↓	390.625 ↓	512	4 *	90.1	92.80

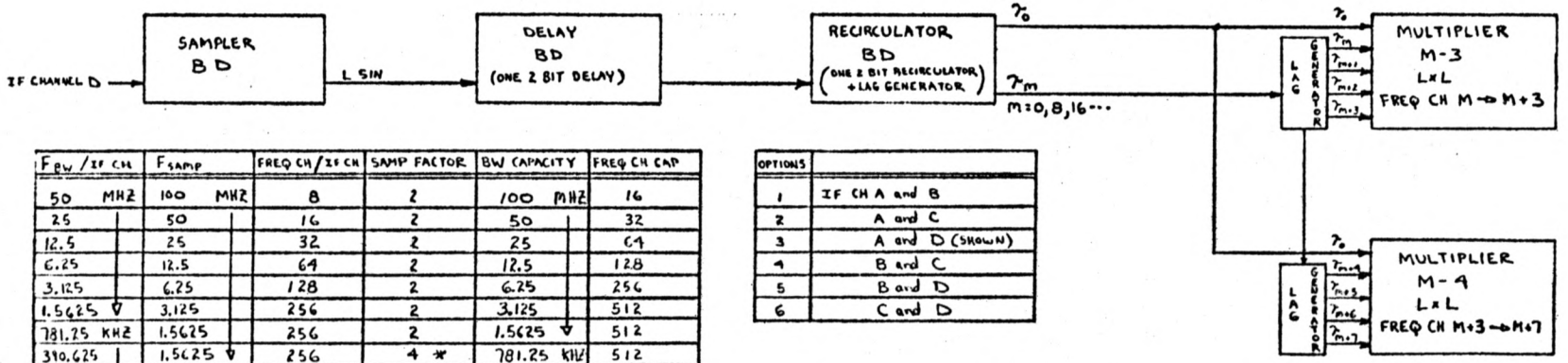
OPTIONS	
1	IF CH A (SHOWN)
2	IF CH B
3	IF CH C
4	IF CH D

* WHEN OVERSAMPLING OCCURS, M STEPS BY TWICE THE AMOUNT SHOWN AND τ_{M+N} INTO MULTIPLIERS BECOMES τ_{M+2N}.

** APPLIES TO FIG 2 THRU 5.

FIGURE 3 DUAL BAND SPECTRAL LINE MODE



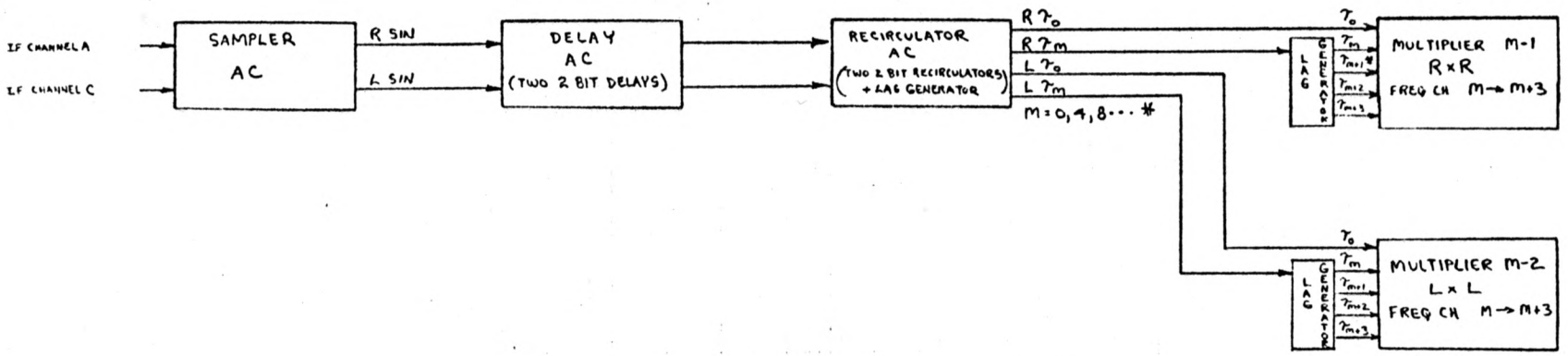


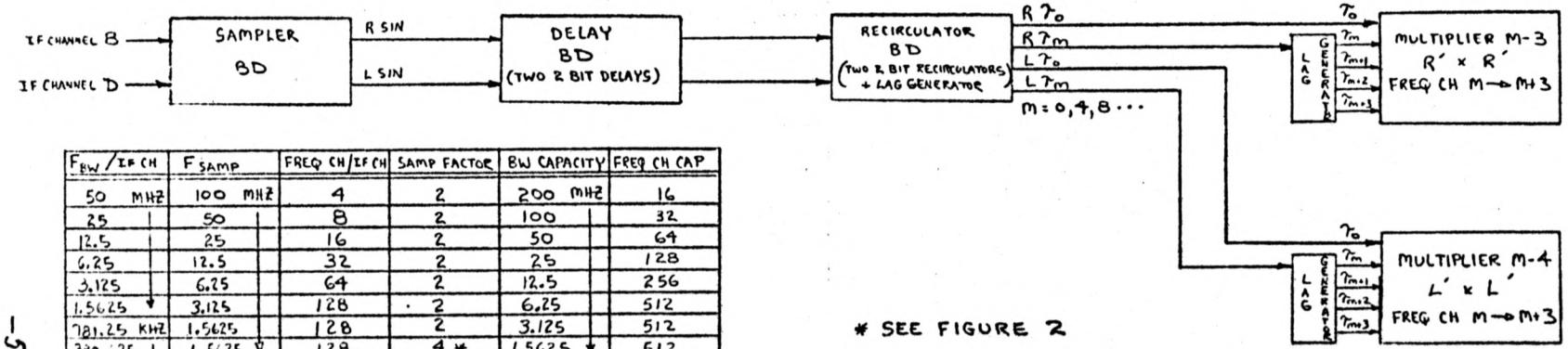
F_{BW} / IF CH	F_{SAMP}	FREQ CH/IF CH	SAMP FACTOR	BW CAPACITY	FREQ CH CAP
50 MHZ	100 MHZ	8	2	100 MHZ	16
25	50	16	2	50	32
12.5	25	32	2	25	64
6.25	12.5	64	2	12.5	128
3.125	6.25	128	2	6.25	256
1.5625	3.125	256	2	3.125	512
781.25 KHZ	1.5625	256	2	1.5625	512
390.625	1.5625	256	4 *	781.25 KHZ	512
195.3125	781.25 KHZ	256	4 *	390.625	512
97.65625	390.625	256	4 *	195.3125	512
[redacted]					

OPTIONS	
1	IF CH A and B
2	A and C
3	A and D (SHOWN)
4	B and C
5	B and D
6	C and D

* SEE FIGURE 2

FIGURE 4 FOUR BAND SPECTRAL LINE MODE



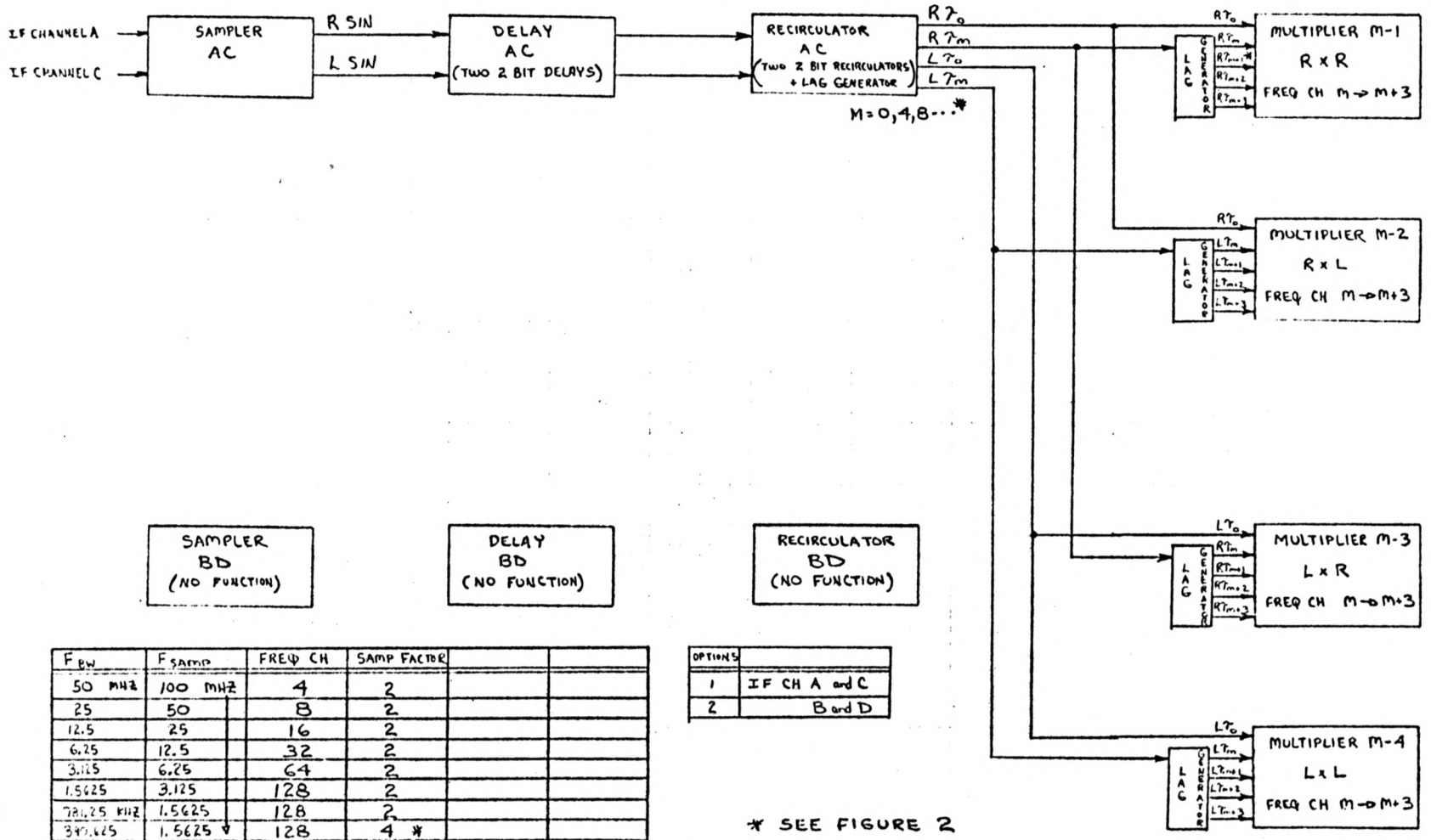


F_{BW} / IF CH	F_{SAMP}	FREQ CH/IF CH	SAMP FACTOR	BW CAPACITY	FREQ CH CAP
50 MHZ	100 MHZ	4	2	200 MHZ	16
25	50	8	2	100	32
12.5	25	16	2	50	64
6.25	12.5	32	2	25	128
3.125	6.25	64	2	12.5	256
1.5625	3.125	128	2	6.25	512
781.25 KHZ	1.5625	128	2	3.125	512
390.625	1.5625	128	4 *	1.5625	512
195.3125	781.25 KHZ	128	4 *	781.25 KHZ	512
97.65625	390.625	128	4 *	390.625	512

* SEE FIGURE 2

FIGURE 5

POLARIZATION SPECTRAL LINE MODE

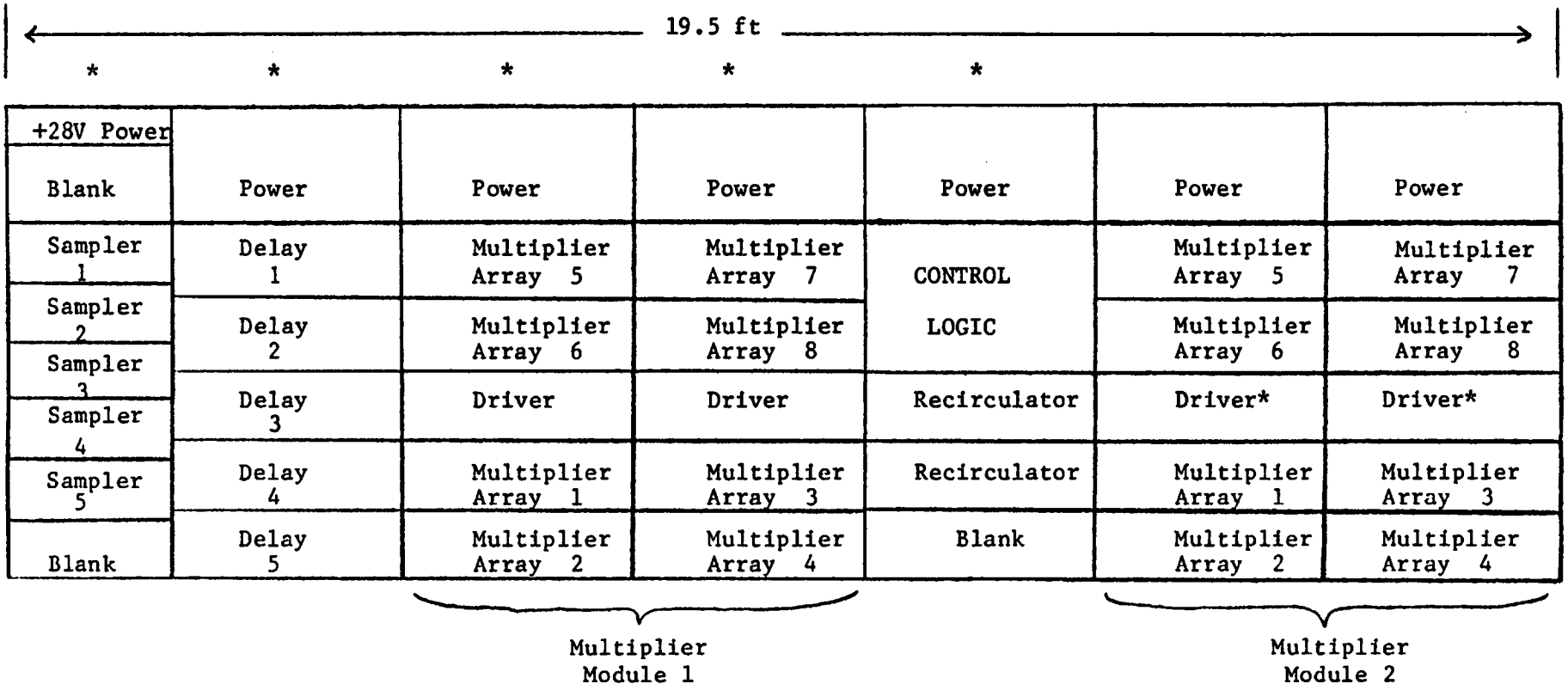


SAMPLER BD (NO FUNCTION)	DELAY BD (NO FUNCTION)	RECIRCULATOR BD (NO FUNCTION)

F_{BW}	F_{samp}	FREQ CH	SAMP FACTOR		
50 MHZ	100 MHZ	4	2		
25	50	8	2		
12.5	25	16	2		
6.25	12.5	32	2		
3.125	6.25	64	2		
1.5625	3.125	128	2		
781.25 KHZ	1.5625	128	2		
390.625	1.5625 ↓	128	4 *		
195.3125	781.25 KHZ	128	4 *		
97.65625	390.625 ↓	128	4 *		

OPTIONS	
1	IF CH A and C
2	B and D

* SEE FIGURE 2



Sampler: 1 Rack, 5 Bins, 54 Modules

Delay: 1 Rack, 5 Mother Boards, 108 Cards

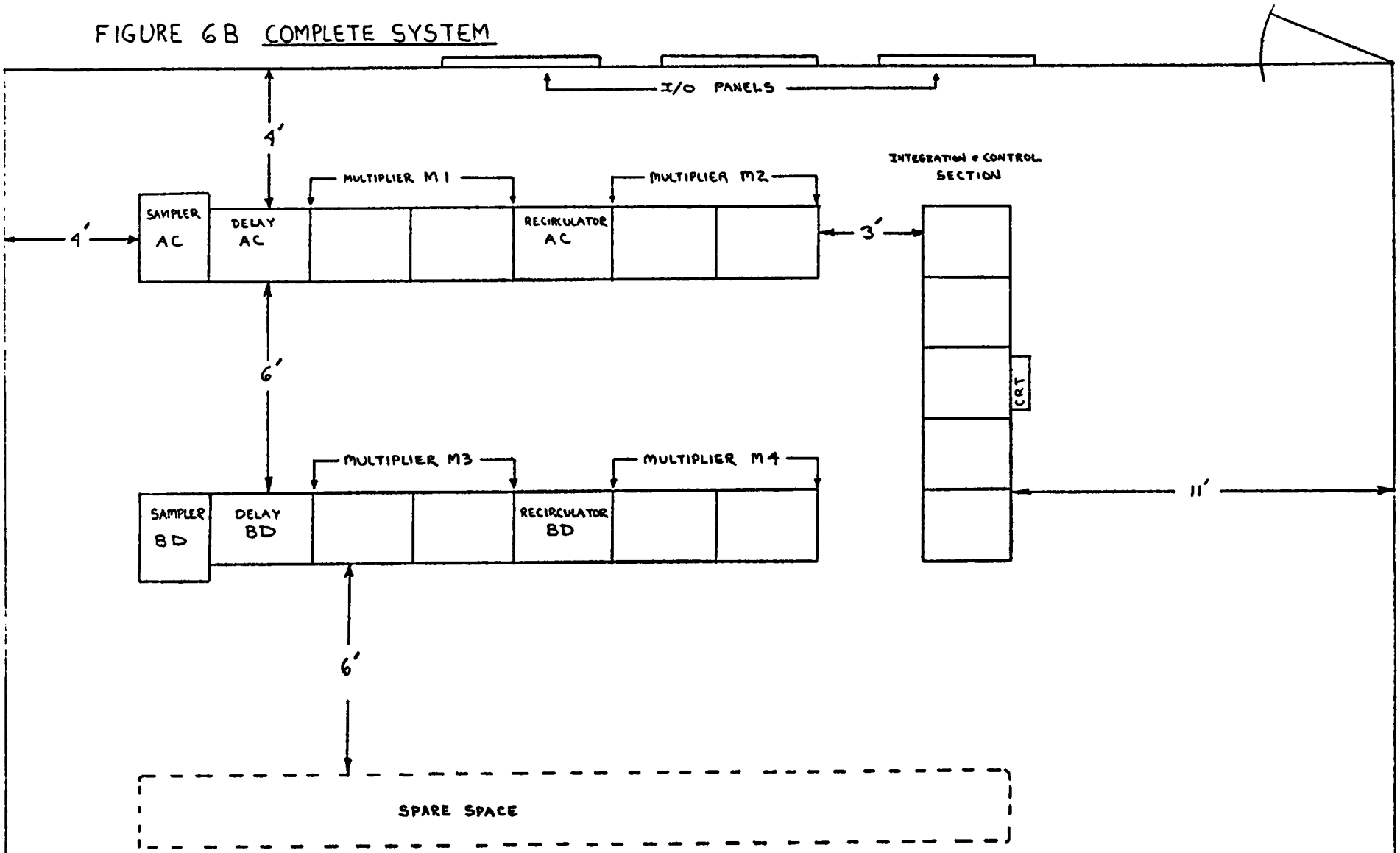
Recirculator: 1 Rack, 2 Mother Boards, 54 Cards

Multiplier: (Per Module) 2 Racks, 8 Mult M.B., 216 Cards
2 Driver M.B., 28 Cards

*Needed in the 1 Multiplier Module Prototype System

Figure 6A One-Half of Combined System

FIGURE 6B COMPLETE SYSTEM



+28V POWER	POWER	POWER	POWER	POWER	POWER	POWER
Sampler	MULT	MULT	CONTROL	CONTROL	MULT	MULT
Sampler	MULT	MULT	DELAY	DELAY	MULT	MULT
Sampler	DRIVER	DRIVER	RECL	RECL	DRIVER	DRIVER
Sampler	MULT	MULT	DELAY	DELAY	MULT	MULT
Sampler	MULT	MULT	DELAY	DELAY	MULT	MULT
Blank	MULT	MULT	BLANK	BLANK	MULT	MULT

Sampler Module: 1 Rack, 54 Modules in 5 Bins

Delay Module: 2 Racks, 108 Delay Cards, 4 M.B.,
54 Recl. Cards, 2 M.B.

Mult Module: 2 Racks, 216 Mult Cards, 8 M.B.,
28 Driver Cards, 2 M.B.

6C: Alternate Station Configuration Not Discussed in Text.

Mode I Continuum (Figure 1)

The operation of the system in continuum mode differs from the present system in that twice as many multipliers are now available. Thus the new design will produce, for any two antennas, the products:

R*R
R*L
L*R
L*L
} for each combination S*S, S*C

in multiplier module 1 and

R*R
R*L
L*R
L*L
} for each combination C*C, C*S

in multiplier module 2.

Where R refers to a right polarized signal, L a left polarized signal, and C and S the sine and cosine quadrature componants developed in the sampler.

Mode II Single Band Spectral Line (Figure 2)

Four operational options in this mode, corresponding to the four signals developed by each antenna, exist and are noted on Figure 2. This mode requires cabling between system AC and system BD to utilize all four multiplier modules to process a single IF signal and this cable interface is implemented at the recirculator output. Earlier proposals had this interface at both the sampler and delay inputs. The system of Figure 2, however, reduces the logic in operation at one time to only that necessary and hence improves reliability. In addition both the delay and recirculator modules will provide low power standby modes whereby unused logic can be disabled, saving, in spectral line operational modes, several hundred amperes of power supply current.

In this, as in all spectral line modes, only the sine quadrature components are correlated; all cosine logic will be in low power stand-by.

Mode III Dual Band Spectral Line

This mode and its various signal and bandwidth options is illustrated in Figure 3. The bandwidth capacity and frequency channel capacity columns refer to effective bandwidth and frequency channels obtained for options whereby the two processed bands are adjacent in frequency (with a small overlap), in Figure 4 four adjacent bands are possible.

As seen, any two of the four IF channels per antenna can be simultaneously correlated (no cross products) in the multipliers with each signal correlated in two multiplier modules. Cables interconnecting the two systems are used in options 2 and 5 of Figure 3.

Mode IV Four Band Spectral Line

This mode of operation is an extension of Mode III whereby all four IF signals are simultaneously correlated, one per multiplier module.

Mode V Polarization Spectral Line

In this mode cross products between two IF channels are obtained. As in Figure 5, the products

R*R
R*L
L*R
L*L

are produced, one in each multiplier module. In Modes III and IV polarization work can be done but no cross products are available.

III. THE SAMPLER SYSTEM

The sampler system specifications are:

Bandwidth: 49 MHz (1 to 50 MHz)

Quantization: 2 bit, 3 level

Delay Resolution: 625 ps

Delay Range: 10 ns

Outputs: 4 digital (2 each for sin and cos quadurature components)

Input: + 16·5 dBm into 50 Ω (with ALC signal to IF receiver)

Modules: 54 (in one 19" rack)

No change over the sampler system in the continuum system is required; hence little discussion of this module is required in this paper.

IV. THE DELAY SYSTEM

The delay system specifications are:

Clock Rate: 100 MHz

Delay Resolution: 10 ns

Delay Range: 163·84 μs

Delay Per P.C. Card: 2 bits

Delay Program Update Rate: 19·2 Hz

P.C. Cards Per Module: 108 (in 5 mother boards, one 30" rack)

The delay system does not need to change from the continuum system and the earlier proposals on the combined system assumed using the present design as is and building one delay module of two 30" racks with 216 delay cards (one bit per card) and 54 control cards. Several considerations, however, indicate that re-packaging the present design (somewhat modified) to be desirable. Five justifications for re-working the delay system are:

1. Lower cost: even considering the scrapage of present built and tested cards (saving the IC's) a 2 bit delay card system will save about $50,000 by changing the card requirements (for a 100 MHz system) from 540 (432 delay and 108 delay control cards) to 216 2 bit delay cards of the same physical size.

2. Ease in extending the self test - self healing capacity to include both the delay and recirculator systems. In addition, a drastic reduction in the cabling of the self test function, saving both money and 100 MHz interfaces, will occur.

3. Adding input multiplexer to the delay line input: this feature extends the present multiplier test (where a pseudo random digital signal replaces the delay line output at the multiplier system input) to a system test since the pseudo random signal can be applied at the delay line input. Also, additional options include a 13-antenna array interconnection in which a trade off of antennas for frequency channels can be made. This feature will be useful since in the prototype system, where only one multiplier module will be built and only about thirteen antennas are available in any case, full capacity to produce 256 frequency channels at 3·125 MHz bandwidth will be available since in going from 27 to 13 antennas a 4-to-1 increase in channels result.

4. Increase reliability: the present system illustrates that interface at 100 MHz clock rates to be the most critical item in the design. A dual delay line, with control and programming logic on the delay line card, will eliminate the present complex delay line - control card interface.

5. Reduce the number of racks in the system: this reduction will shorten the signal cable lengths of both the sampler - delay, and delay - recirculator interface.

The new delay line is shown in block diagram form in Figure 7. The input to one delay function (one half of a delay card) can be selected from one of four sources: the sampler output, a pseudo-random data source, a second sampler output (13 antenna array option), or a spare input. As in the present continuum delay line, the 100 MHz digital input is broken down into sixteen parallel 6·25 MHz paths in order to provide bulk delay via inexpensive MOS logic.

The first delay logic provides a discrete 0 or 512 bit, at 6·25 MHz data rate, delay programmed by the MSB of the digital delay program word. Thus of a 16384 bit delay range this stage provides 8192 bits.

The second delay logic provides dual paths of 512 MOS shift registers for each of the sixteen parallel paths. By varying the path duty cycle and clock rates each of the sixteen paths through this stage can be made 513 to 1024 bits long and can be varied in 1-bit steps at the 6·25 MHz clock rate. Thus this stage, programmed by 9 bits of the digital program word, provides 8176 bits of delay. The first two stages thus provide 0 to 16368 bits of delay range with 160 n second resolution.

The next stage is a parallel to serial stage which yields four 25 MHz data paths from the sixteen 6·25 MHz lines. The parallel to serial transfer is timed, being accomplished at one of four discrete times of 40 n second separation. Two additional bits of the delay program word are decoded in timing this transfer yielding 40 n second resolution at this interface. The last stages produce a single 100 MHz data output from the four 25 MHz signals with the transfer timed to occur in any of four discrete time slots separated by 10 n seconds. Thus the final output of the delay line provides 0 - 16383 bits of delay variation with 10 n second resolution.

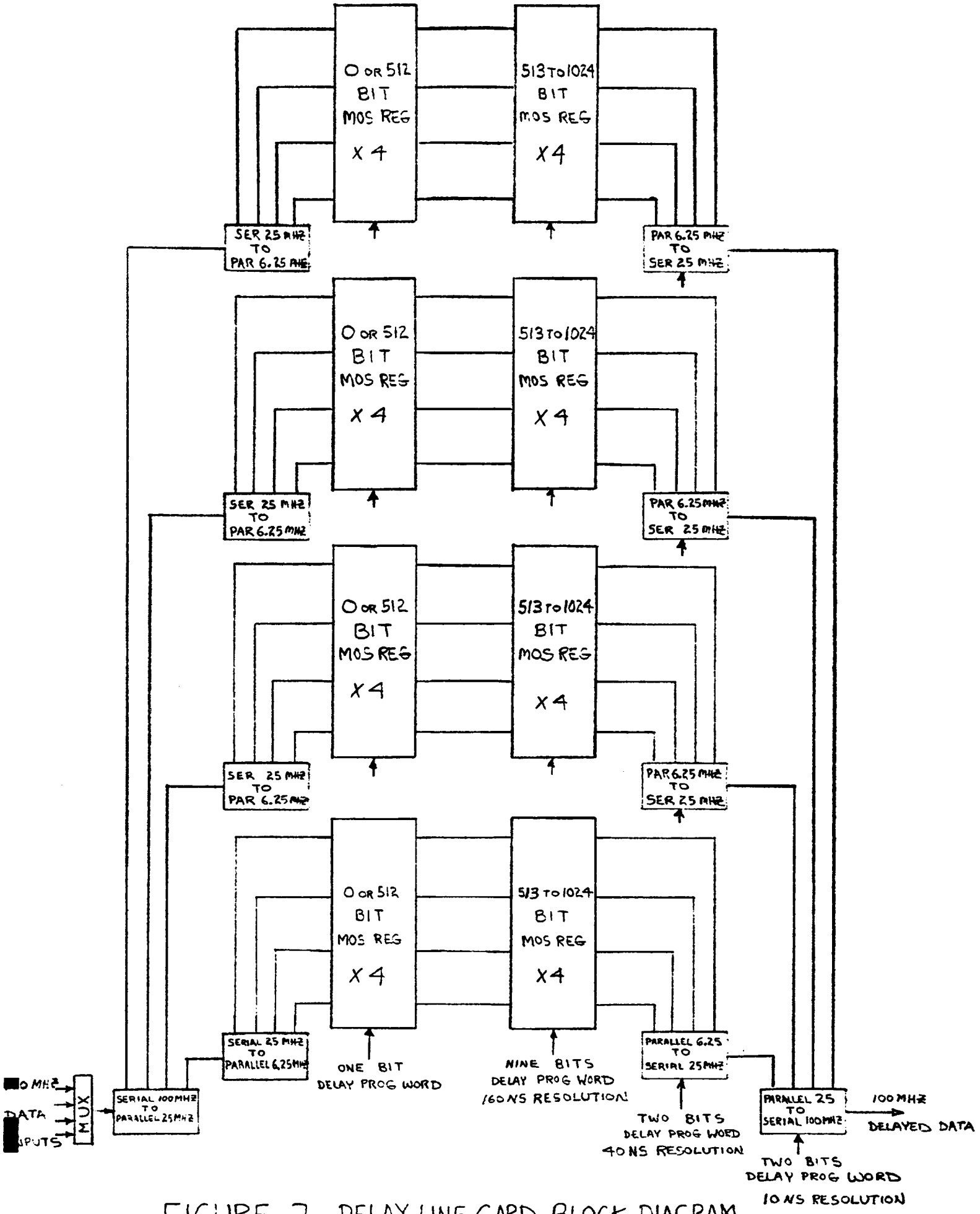


FIGURE 7 DELAY LINE CARD BLOCK DIAGRAM

One bit in the delay program word will disable both 25 and 6·25 MHz TTL clocks and the 6·25 MHz MOS clock yielding a 40% reduction in card dissipation.

An analog summation of the delay line outputs will be performed on each delay line mother board. Six antennas per mother board, individually excludable, will be summed (one right polarization and one left polarization analog sum per mother board with independent excludability) on each mother board. External summation of individual mother board analog outputs will produce an equivilant single antenna 130 meters in diameter. By selecting components and matching cable lengths coincidence of summed digital signals to 100 ps, or better, may be achievable.

V. THE RECIRCULATOR SYSTEM

The recirculator systems specifications are:

Input Clock Rate: 390.625 KHz to 100 MHz in octave steps

Output Clock Rate: 100 MHz

Recirculator Size: 10240 bits

Lag Range: 0 to 2048 bits

Functions per P.C. Card: 4 maximum (4 through functions or 2 recirculation functions)

P.C. Cards per Module: 54 (in 2 mother boards, one 30" rack)

Each recirculator P.C. card will input four 100 MHz digital inputs and provide four 100 MHz digital outputs. In continuum the four inputs correspond to the + and - samples of the sin and cos components of an IF signal, and in continuum the card provides a straight through function with the four card outputs being unmodified version of the inputs (delayed several bits). In spectral line work only the + and - sine inputs to the recirculator P.C. card are used and munipulated to provide + and - τ_o (undelayed) and + and - τ_m (step delayed by lag time M) outputs.

A block diagram of the recirculator is seen in Figure 8, and Figure 9 provides a simplified flow diagram that illustrates its function in spectral line mode.

The best way to visualize the operation of the recirculator in spectral line mode is to think of 10240 bits of RAM made with 40 parallel input and 40 parallel output lines. To produce a 100 MHz data rate the memory must be read in 400 n second cycles. In each 400 n second cycle define one potential write and two read operations. Each N TH potential write cycle (N = 100 MHz/ sample rate) 40 bits of delay line data are written into the RAM. The two read operations produce the τ_o and τ_m 100 MHz data signals separated by lag time M. For M = 0 two 100 MHz data streams, 8192 bits long and one delayed by M = 0 bits from the other, are produced and applied to the correlators. Next M will be set equal to L_s, the lag step (4, 8, 16 or 32 depending on mode), and again two 8192 bit 100 MHz signals are produced, one delayed by M = L_s bits from the other. This operation continues with M increasing by L_s N times and restarts when the maximum lag time $N \cdot L_s$ is produced.

One subtle effect produced with the above recirculator operation is that the first $L_s(N-1)$ and last $L_s(N-1)$ frequency channel integrations computed each 52 m second data valid cycle are calculated using some bits that are not used in any other integration results. For example, at a sample rate of 25 MHz N = 4 and L_s = 16 for Mode II, figure 2. Each time the recirculator unloads 8192 bits into the multipliers 16 frequency channel integrations are performed. At the start of a 19·2 Hz data valid cycle 8192 + 64 bits, at the 25 MHz sample rate, are written into the RAM's, enough to produce 8192 bits of integration with a maximum lag time of 64 bits. Of the first 8192 RAM bits used to compute the first 16 frequency channel integrations $\frac{1}{N}$ (8192) = 2048 bits will be written over by the time the next 16 frequency channel integration is made and thus will appear only in these first 16 integrations. Another 2048 bits that were used

in computation of the first two sets of 16 frequency channels are written over in the data used in the third integration and so on. In all $^{N-1}/N$ (8192) bits on each end of the data valid cycle fail to be used in computing all N (L_s) frequency channel integrations.

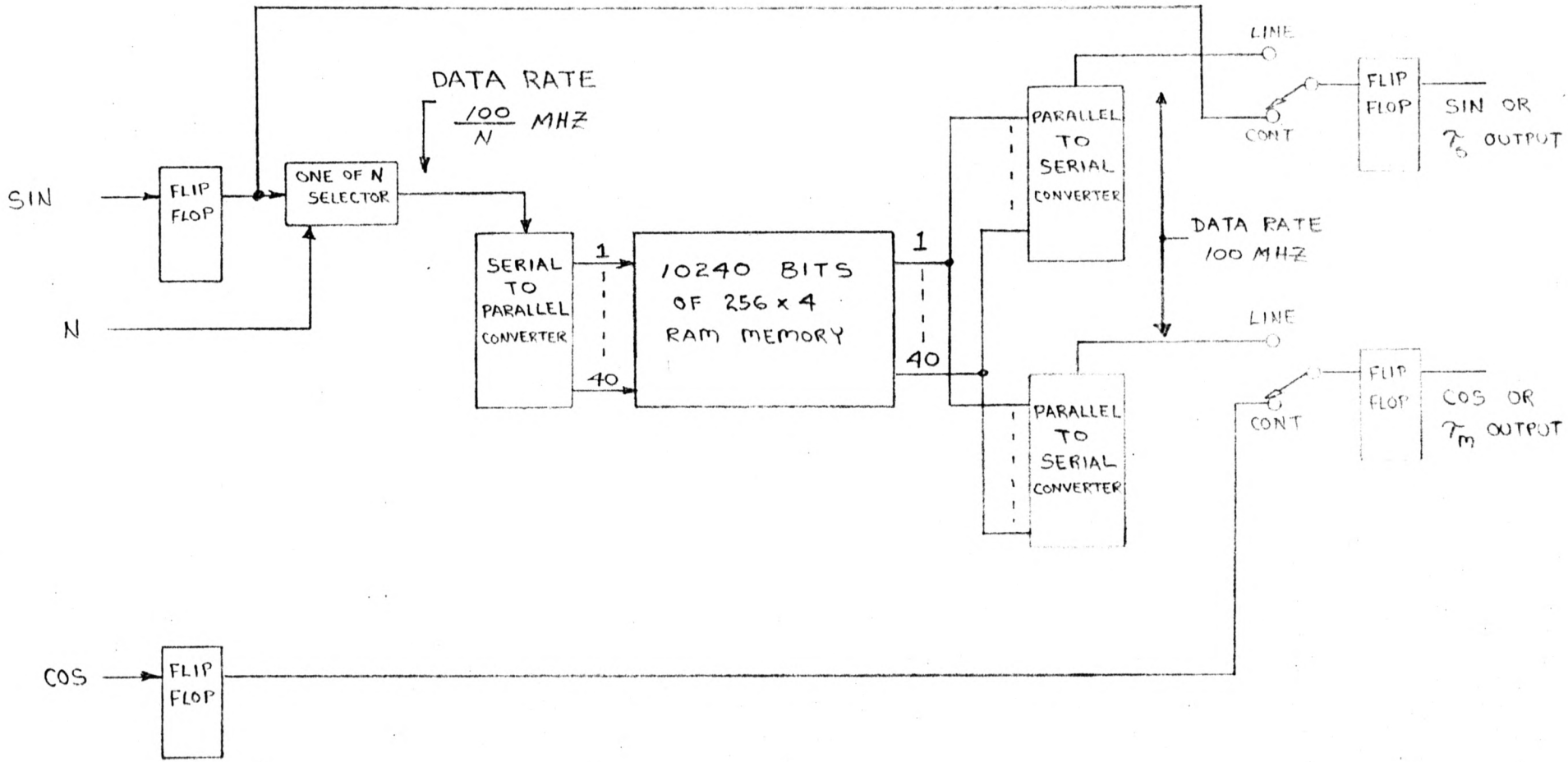


FIGURE 8 RECIRCULATOR BLOCK DIAGRAM
ONE BIT SHOWN

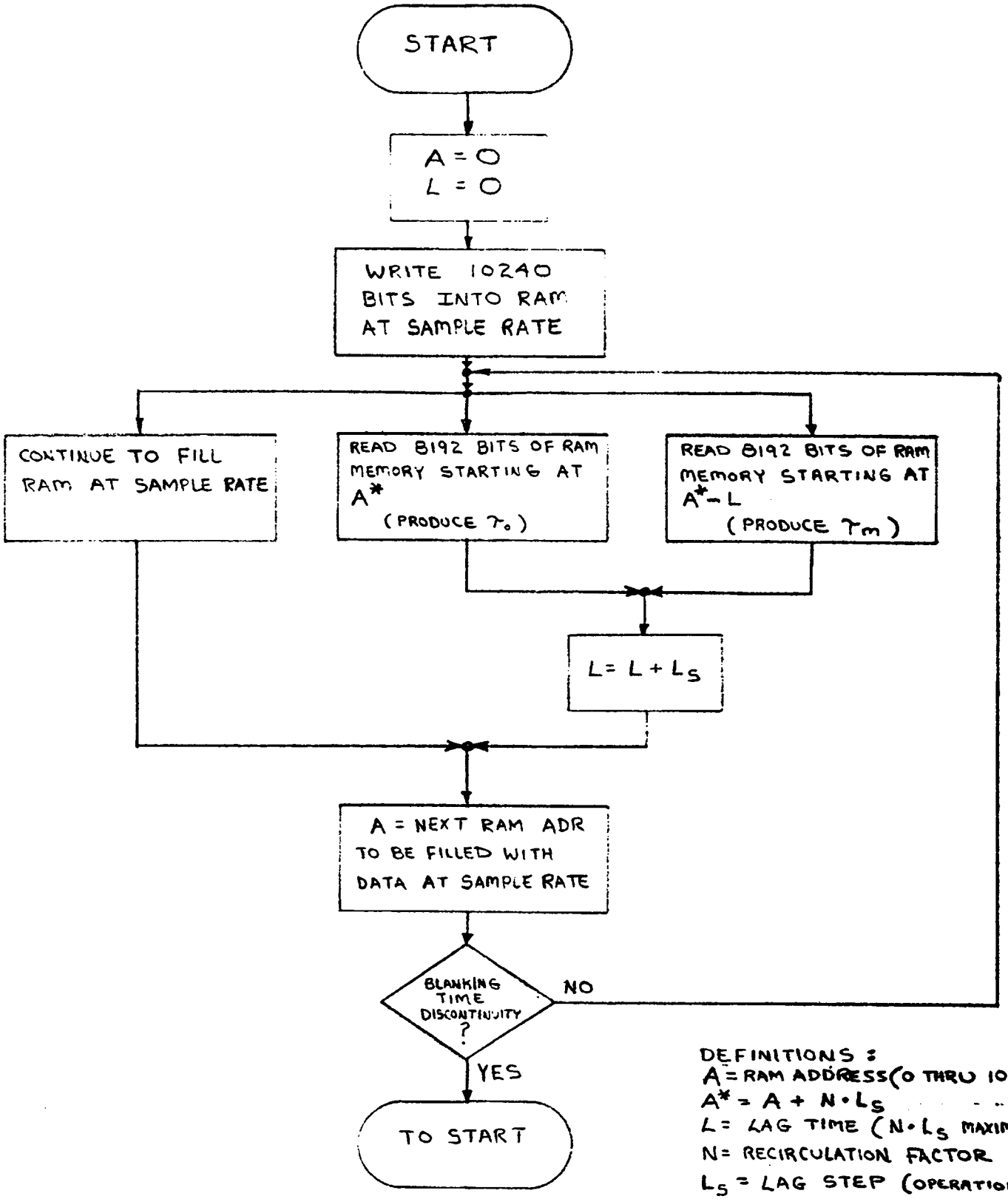


FIGURE 9 RECIRCULATOR FLOW CHART

VI. THE MULTIPLIER SYSTEM

The multiplier specification is:

CONTINUUM:

Multipliers, for any two antennas (A and B), the following multiplications are performed for each of the two 50 MHz bandwidths:

Array 1	RSA*RSB	RCA*RCB
Array 2	LSA*LSB	LCA*LCB
Array 3	RSA*LSB	RCA*LCB
Array 4	LSA*RSB	LCA*RCB
Array 5	RSA*RCB	RCA*RSB
Array 6	LSA*LCB	LCA*LSB
Array 7	RSA*LCB	RCA*LSB
Array 8	LSA*RCB	LCA*RSB
	Module 1	Module 2

Total cross multipliers = (32) (351) = 11232

Total self multipliers per two modules: selectable as follows

(A) 216 self mult. (108 redundant)

(B) 162 self mult. (54 redundant) plus 54 sin*cos multipliers

(c) 108 self Mult. plus 108 sine*cos mult. (54 redundant)

SPECTRAL LINE:

Frequency channels per module: 4

Auto multipliers per module: 27 x 4 = 108

The multiplier modules in the combined system differ from that used in the continuum system in four main ways:

1. On card integration has been incorporated to allow 8192 bits of integration (producing a 14 bit integration result) with secondary storage to allow integration result readout without stopping observation.

2. Driver stages have been added (on separate cards and mother boards) to reduce cabling requirements by considerably reducing cable lengths to the multiplier mother boards.

3. The self multipliers have been removed from the multiplier card and self multiplier/sin*cos multiplier/auto multipliers have been added to the driver board.

4. Blanking is accomplished synchronously in the driver stage instead of asynchronously using the multiplier flip-flop direct resets. Thus the 8192 bit integration period (V_S = 8192) can be made precise instead of ± 2 counts as in the present continuum system.

A 14 bit integration result will be produced during 8192 bits of observation. Of these bits the two least significant are truncated since they contain only noise and after letting the last carry ripple through, the remaining twelve bits are set into secondary storage to be shifted out during the next 8192 bit integration. This short integration time will be used in both continuum and line work. In line work separate storage is available for the various lag channels produced by a given multiplier whereas in continuum observations all twelve bit integration results of a given multiplier are summed together to obtain a final result.

Two points may be brought out at this time. First, 8192 bits of integration, counting by 2 each time, actually overflows the 14 bit integration capacity by one count. However, since counting by two every time is not possible in practice, the integration capacity is adequate. Second, increasing the 8192 bit per recirculator readout integration to 9216 bits (further

aggrevating the situation above) will make the achievement of the observational efficiencies of Figures 2 - 5 easier. For example, at a sample rate of 390·625 KHz the recirculator (8192 bits + 1024 maximum lag of it) can be filled 2·28 times per 19·2 Hz data valid cycle. Thus only two complete recirculations can be made through the lag channels producing an observational efficiency of 80·5%. It is possible to do one of three things to raise this figure.

1. Produce three complete recirculations, two with 8192 bits of previously unprocessed data and a third recirculation using 2048 bits of new data and 6144 bits of contiguous data previously processed in the second recirculation.

2. Produce three complete recirculations, two as before and a third with V_s = 2048 and the remaining 6144 bits blanked out.

3. Produce two complete recirculations, each on the basis of 9216 bits (V_s = 9216).

In each case the observational efficiency goes to 90·1% (against 92·8% maximum possible). Which option to use has not been decided at this time. The advantage of using 8192 bit integrations is that using a binary number eliminates the necessity of V_s subtraction, or at least makes it much easier.

VII. SELF TEST - SELF HEALING

The self test feature of the present continuum system will be changed considerably to make it more complete and automatic. The self healing feature will be expanded to enclose the recirculator function.

It is proposed that self test be performed during the data invalid period by using the pseudo random input port to the delay line. Four complete 8192 bit integrations could be performed during the 1·6 m second data invalid period and the multiplier integration outputs checked to limits. Each integration would be performed at different delay values and recirculator set-up with all possible delays and recirculator functions covered every few 19·2 Hz cycles. Thus every 52 m second a 95% complete checkout of the entire system would occur, being extended to 100% every 128 52 M second cycles (6·6 seconds). Fault isolation will be performed by tabulating errors into several tables, thus a single error would indicate a single multiplier error, 351 errors that contain a common delay line output will indicate a bad delay line or recirculator, 13 errors associated with a single multiplier board will indicate a bad multiplier board (a component common to all multipliers failed).

Once a failure is found and isolated to a delay line or recirculator the redundant delay and recirculator cards (two extra delay cards and one extra recirculator per system) will assume the function of the failed path until the defective card can be replaced.

Several advantages result from the above technique:

1. Complete, automatic, non-interfering checkout of the full system every 52 m seconds.

2. Even after a failure and healing event occurs the self test continues. In the present system once self healing has occurred self test capacity is lost.

3. Success of the self healing attempt can be evaluated.

Failed self multipliers or sin*cos multipliers in continuum work can be worked around by selecting the mix of self or sin * cos multipliers. A total of 54 multipliers per two multiplier modules are available to back up the 108 self and 54 sin*cos multipliers.

The redundant recirculator will provide four integrators that can be used to calculate the duty cycle, and hence the sample level, of any of the four sampler digital outputs. This function can be programmed to any sampler output. This integration, and its respective V_s, will be on the basis of 52 m seconds of data, not 8192 bits.

VIII. CONTROL LOGIC

It is desirable for delay line control, recirculator control, self test, and multiplier systems configuration control be, as completely as possible, self contained. Data exchange with the System Controller can be limited to supplying observational mode information and System configuration, delay values, and receiving multiplier results, self test results, self healing actions, various programming playbacks, and system monitor information.

The control logic required to accomplish this aim will be relative simple by the present continuum System Controller standard and will make the design and initial checkout of the system much easier seeing that design of the delay/multiplier system and design of the new System Controller will be performed 2,000 miles apart.

XI. THE ONE MULTIPLIER MODULE PROTOTYPE

A prototype delay/multiplier system will be constructed consisting of one each sampler, delay, recirculator and multiplier modules. This hardware will handle one 50 MHz system (two 50 MHz front end bands) and will be

used to evaluate the system before full construction is attempted. The 13 antenna option will, however, permit computation of the full number of frequency channels obtainable from the full system thus far described. Otherwise the 27 antenna configuration will provide one-fourth the frequency channel capacity, for a given bandwidth, specified in Figures 2 through 5.

In order to provide all self multipliers in continuum for the prototype, four driver mother boards must be present. Figure 6 defines the configuration of the prototype system.

Expansion of the prototype system to a full 50 MHz system will require simple addition of eight mother boards and 216 multiplier cards and associated cables and power supplies.

XL. SCHEDULING AND COST ESTIMATE

Table I and Table II are schedule and cost estimates. Prices for these cost estimates are based on development of the continuum system and component prices experienced in the six antenna system build.

Table III gives the 1976 estimate for development and non-recurring costs. The total 1976 budget requirements depend on what portion of the prototype system parts are ordered in 1976. It is possible to shift a large portion of the cost of the prototype system to either the 1976 or 1977 budgets. If parts and boards for the multilayer cards are ordered in late 1976 (and received in 1976) up to $200K must be added to the 1976 budget. Otherwise the 1976 budget requirements are illustrated in Table III.

TABLE I

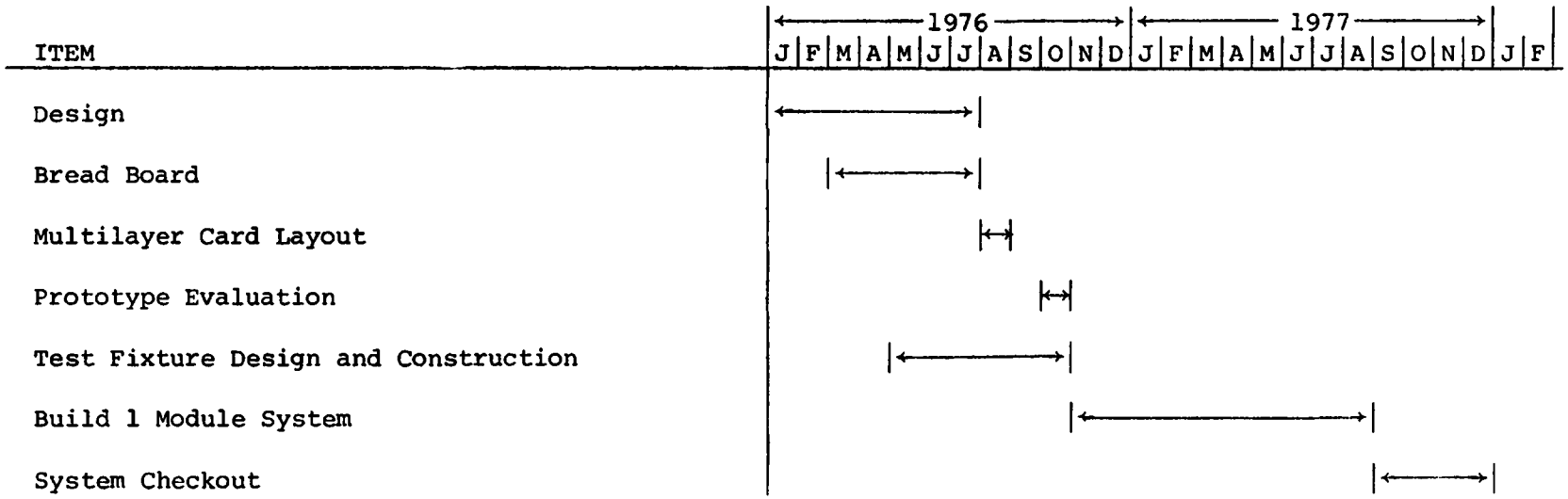

ITEM
1976
1977
J F M A M J J A S O N D J F M A M J J A S O N D J F
Design
Bread Board
Multilayer Card Layout
Prototype Evaluation
Test Fixture Design and Construction
Build 1 Module System
System Checkout

TABLE II

ITEM	TWO BAND SYSTEM WITH ONE MULTIPLIER MODULE		FULL FOUR BAND SYSTEM WITH FOUR MULTIPLIER MODULES	
SAMPLER SYSTEM				
Modules	54 @ $700	$	108	$ 75.6K
Bins	5 @ 100	0.5K	10	1.0K
Racks	1 @ 630	0.63K	2	1.26K
Cables	216 @ 5	1.08K	432	2.16K
DELAY SYSTEM				
Cards	108 @ 550	59.4K	216	118.8K
Mother Boards	5 @ 500	2.5K	10	5.0K
Racks	1 @ 460	.46K	2	.92K
Cables	40 @ 40	1.6K	80	3.2K
RECIRCULATOR SYSTEM				
Cards	54 @ 715	38.61K	108	77.22K
Mother Boards	2 @ 500	1.0K	4	2.0K
Racks	1 @ 460	.46K	2	.92K
Cables	20 @ 40	.8K	40	1.6K
MULTIPLIER SYSTEM				
Multiplier Cards	216 @ 350	75.6K	864	302.4K
Driver Cards	28 @ 250	7.0K	112	28.0K
Mother Boards	10 @ 500	5.0K	40	20.0K
Racks	2 @ 460	.92K	8	3.68K
Cables	216 @ 25	5.4K	864	21.6K
SELF TEST				
Cards	5 @ 500	2.5K	10	5.0K
Cables	20 @ 35	.7K	40	1.4K
CONTROL		20.0K		50.0K
POWER		22.0K		75.0K
MISCELLANEOUS		50.0K		125.0K
TOTAL		$334K		$922K

TABLE III

ACTIVITY	ITEM	ESTIMATED 1976 COST
Development and Non-recurring	BREADBOARDING:	
	Delay Card	$200
	Recirculator Card	700
	Driver Card	100
	CIRCUIT CARD LAYOUT:	
	Delay Card	$2K
	Recirculator Card	2K
	Multiplier Card	1.5K
	Driver Card	2K
	MOTHER BOARD LAYOUT:	
	Delay M.B.	$3K
	Recirculator M.B.	3K
	Multiplier M.B.	1.5K
	Driver M.B.	3K
	CONTROL LOGIC:	$5K
	PROTOTYPING:	
	Delay Card	$200
	Recirculator Card	300
	Multiplier Card	250
	Driver Card	150
	Mother Boards	3K
	TEST FIXTURES:	$5K
	MISCELLANEOUS:	$10K
	TOTAL:	$42.9K