NATIONAL RADIO ASTRONOMY OBSERVATORY
VERY LARGE ARRAY PROJECT
SOCORRO, NEW MEXICO

VLA ELECTRONICS MEMORANDA #140

December 1976

DIGITAL CORRELATOR AND INTEGRATOR CUSTOM INTEGRATED CIRCUITS

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Two custom integrated circuits, to be used in the VLA combined continuum/spectral line correlator system, are being developed for NRAO by Silicon Systems Inc. of Irvine, California. The purpose of this report is to publish the operational specifications of these circuits in the event that other applications, such as other correlator receivers being planned or designed, exist.

The first IC, the VLA-1 (NRAO Specification A13800N1), is a dual 2 bit, 3 level by 2 bit, 3 level ECL correlator designed to work at data rates up to 100 MHz. This chip will interface with standard ECL 10 K logic operating on a -5.2 V supply at its input and with standard 7400 TTL logic operating on a +5.0 V supply at its output. The IC Specification A13800N1, attached, can be referred to for more detailed information.

The second IC, the VLA-2 (NRAO Specification A13800N2), is a 12 stage integrator with 12 bits of secondary storage designed to interface with the VLA-1. The 12 stage counter can integrate the results of up to 8192 correlation products (or any number if cascaded) while the secondary storage shift register is providing access to the 12 bits of a previous integration. The VLA-2 is of low power Schottky technology and has standard 7400 TTL input and output logic levels and operates from a single +5.0 V power supply. The VLA-2 is in an 8 pin dual-in-line package allowing two integrator functions per 16 pin socket to be achieved.

The IC Specification A13800N2, attached, can be referred to for more detailed information.

To give some idea of the potential advantages of these

integrated circuits a short review of their impact on the VLA correlator system may be of interest. Below is listed several items illustrating the improvement realized in the VLA combined continuum/spectral line system (correlator portion only). This system is a recirculating correlator that provides, at one time, 16 frequency channels on 351 baselines (or has 11,232 hardware correlators).

A) Cable/100 MHz data interface reduction

1) Discrete component design

864 multisignal cables carrying 6912 100 MHz data interfaces.

2) Custom IC design

192 multisignal cables carrying 1726 100 MHz data interfaces.

B) Power reduction

1) Discrete component design

26.4 KW

2) Custom IC design

8.9 KW

C) Cost reduction

$100,000 estimate (about 25%)

D) Size reduction

1) Discrete component design

8 racks

2) Custom IC design

2 racks

E) Chip count reduction (and hence reliability increase)

1) Discrete component design

72,900 IC's

2) Custom IC design

17,500 IC's

Some specs will probably change from those indicated in the specifications attached but no major changes are anticipated. The

power level of the VLA-1 will hopefully be reduced to around 500 mW nominal.

Silicon System has stated that they can accept smaller orders of IC's at the same quantity prices NRAO will get. These prices are in the $7.80 to $6.20 range each for VLA-1 (depending on NRAO's final order quantity) and $6.20 to $5.20 each for the VLA-2. If there is any interest in these circuits, more information can be obtained from the author at 505-772-4283. The final order will be placed around March of 1977.

NATIONAL RADIO ASTRONOMY OBSERVATORY
Post Office Box "O"
Socorro, New Mexico 87801

SPECIFICATION NO. A13800N1 DATE: September 1, 1976

NAME: VLA-1 CUSTOM INTEGRATED CIRCUIT

PREPARED BY: APPROVED BY:

I. INTRODUCTION

This specification defines the operational characteristics of the VLA-1 custom integrated circuit. This chip is to perform in a dual digital correlator application at a 100 MHz clock rate with ECL inputs and TTL outputs and will be used in the NRAO Very Large Array Radio Telescope. Pin assignments and a functional block diagram are shown in Appendix 1.

II. PACKAGE

The VLA-1 integrated circuit package will be a 16-pin ceramic dual-in-line package. The specific package will be a subject of discussion between the supplier and NRAO and a mutually acceptable decision will be made on the results of this discussion. The package will have standard 0.3 inch pin spacing with pins on 0.1 inch centers. The package will be permanently marked on top with the designation VLA-1.

III. ENVIRONMENTAL CONDITIONS

The VLA-1 will meet all operational specifications under the following conditions:

1. Temperature: 0 to 70 C moving air blowing at 500 LFPM perpendicular to the dip longitudinal axis.

2. Voltage:

   ECL Portion -5.2V±5%

   TTL Portion +5.0V±5%

3. Power:

   P_{DISS} = 960 mW Max at nominal voltages

The VLA-1 will not be permanently damaged under the following conditions:

1. Temperature:
   A. Storage for 24 hours at -55 to +125 C still air.
   B. Thermal cycle: 5 cycles, 60 seconds at OC, 60 seconds at 100 C, 10 seconds transfer time air-to-air. (Power not applied.)

2. Voltage:
   A. ECL Portion -5.2V
      TTL Portion 0V (indefinitely)
   B. ECL Portion 0V (indefinitely)
      TTL Portion +5.0V
   C. ECL Portion -6.5 (30 sec transient)
      TTL Portion +5.0
   D. ECL Portion -5.2
      TTL Portion +6.0 (30 sec transient)

3. Vibration and Shock:
   A. Vibration: 20 Hz to 2 KHz at 20G for 60 seconds.
   B. Shock: 1000G shock in any axis.

IV. LOGIC INPUT SPECIFICATIONS

All ECL inputs will be compatible with ECL 10,000 series standards. Thus over the operational temperature and supply voltages of Section III:

input logic 0 (V_{IL}) is defined as $-5.2V \leq V_{IL} \leq -1.63V$

input logic 1 (V_{IH}) is defined as $-0.98V \leq V_{IH} < -0.6V$

Loading will be less than 200 µADC and no more than 3 PF per input.

These specifications cover the data inputs, the clock input, and the reset input pins.

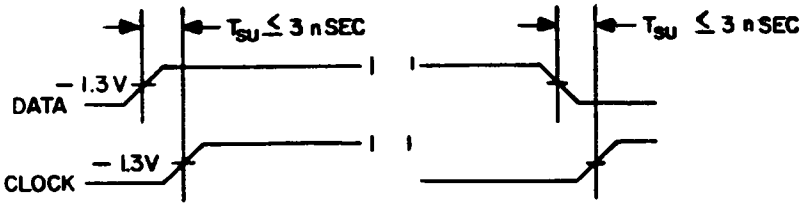
V. OUTPUT DRIVE

V out $\leq$ 0.5V sinking 10 MADC at logic zero

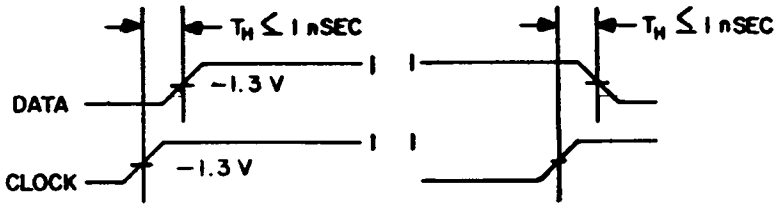
V out $\geq$ 2.5V sourcing 100 µADC at logic one

VI. ACTIVE CHARACTERISTICS

A) SETUP TIME (T_{SU})

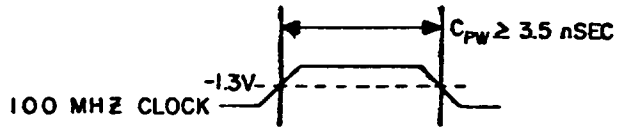


B) HOLD TIME (T_H)

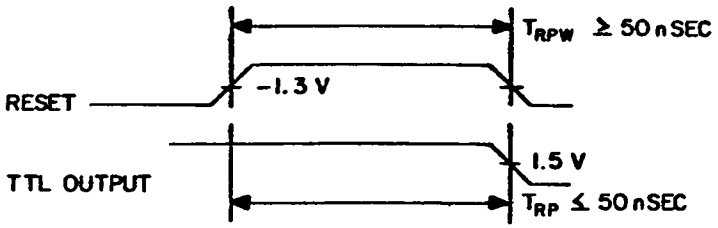


In either case clock reliably captures the data present at a data input pin at least T_{su} prior to and held at least T_H after the clock rising transition.

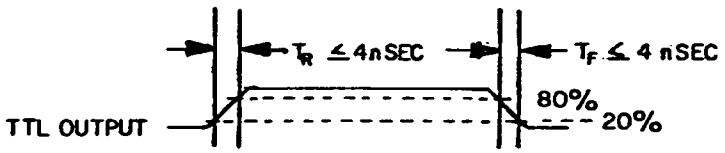
C) CLOCK PULSE WIDTH (C_{PW})



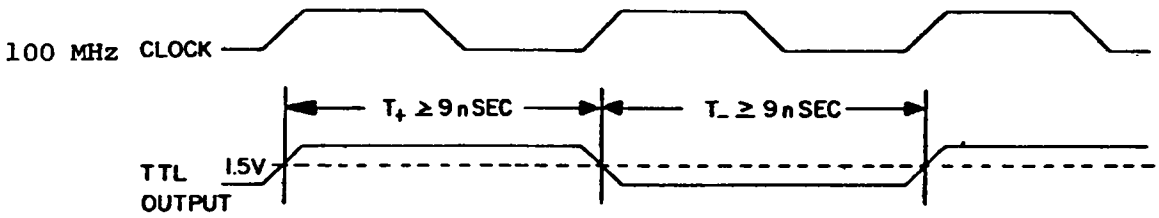
D) RESET PULSE WIDTH AND RESET TIME (T_{RPW} & T_{RP})



E) OUTPUT RISE AND FALL TIME (TTL LOAD) (T_R & T_F) SEE SECTION VIII FOR TTL LOAD REQUIRED



F) OUTPUT PULSE WIDTH (T_+ & T_-) SEE SECTION VIII FOR TTL LOAD REQUIRED



G) TOGGLE RATE OF FLIP/FLOPS (F_{TOG})

F_{TOG} = 0 TO 125 MHZ, $V_E = -5.20$ V, TEMP = 25° C

F_{TOG} = 0 TO 110 MHZ OVER SECTION III RANGE

VII. FUNCTION TABLE (See Appendix 1 for identification of Q_A, Q_B, Q_C, Q_D and +A, -A, +B, -B, +C, -C).

The chip shall perform a dual 3-level x 3-level digital correlator function as defined in the following table:

Q_{AO} = before clock positive transition

Q_A = after clock positive transition

+A	-A	+B	-B	Reset	Clock	Q_A	Q_B	Remarks
X	X	X	X	1	X	LOW	LOW	Reset
0	0	X	X	0	⎍	$\overline{Q}_{AO}$	$\overline{Q}_{BO}\cdot Q_{AO} + Q_{BO}\cdot\overline{Q}_{AO}$	Increment counter by 1
X	X	0	0	0	⎍	$\overline{Q}_{AO}$	$\overline{Q}_{BO}\cdot Q_{AO} + Q_{BO}\cdot\overline{Q}_{AO}$	Increment counter by 1
0	1	0	1	0	⎍	Q_{AO}	$\overline{Q}_{BO}$	Increment counter by 2
1	0	1	0	0	⎍	Q_{AO}	$\overline{Q}_{BO}$	Increment counter by 2
0	1	1	0	0	⎍	Q_{AO}	Q_{BO}	No change
1	0	0	1	0	⎍	Q_{AO}	Q_{BO}	No change
1	1	X	X	0	⎍	X	X	Don't care
X	X	1	1	0	⎍	X	X	Don't care

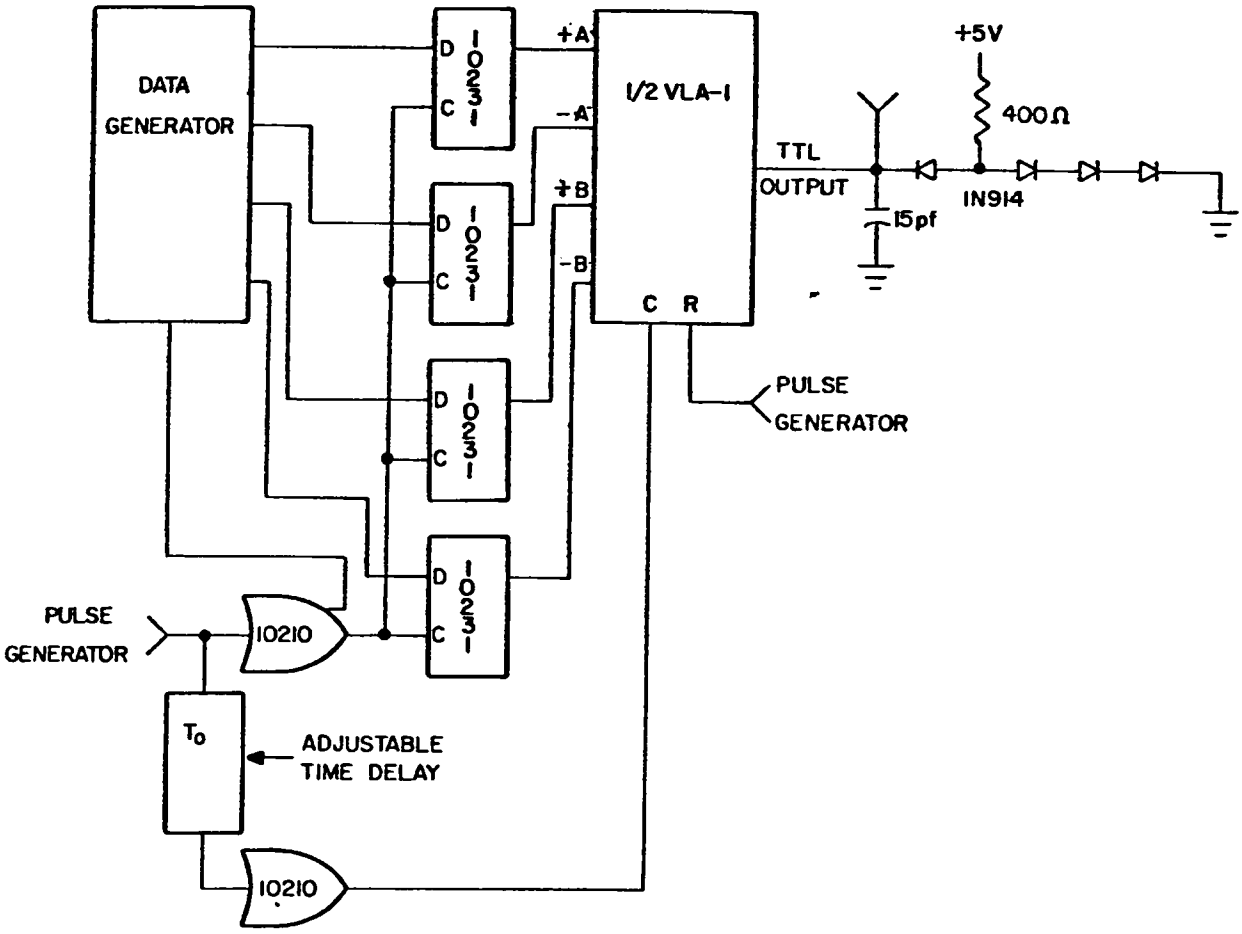
The same table would define the function performed using inputs +B, -B +C, -C and flip-flops Q_C and Q_D.

In the remarks column, flip-flops Q_A and Q_B (or Q_C and Q_D) are treated as two stages of a binary counter.

VIII. TESTING

NRAO will provide a gang test dynamic test fixture to the supplier. The exact form of this fixture will be determined in discussion between NRAO and the supplier.

In general, a fixture as shown will be used in IC dynamic testing.



APPENDIX 1

EQUATIONS AND DESIGN: 3-LEVEL X 3-LEVEL DIGITAL CORRELATOR

Given the 3-level quantization of a wideband analog signal specified by two digital bits +A and -A such that:

(+A) (-A) = 10 indicates sampled analog > V_o

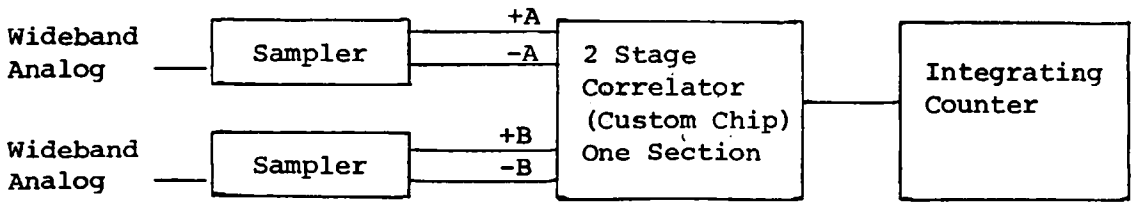
(+A) (-A) = 01 indicates sampled analog < $-V_o$

(+A) (-A) = 00 indicates $-V_o \leq$ sampled analog $\leq V_o$

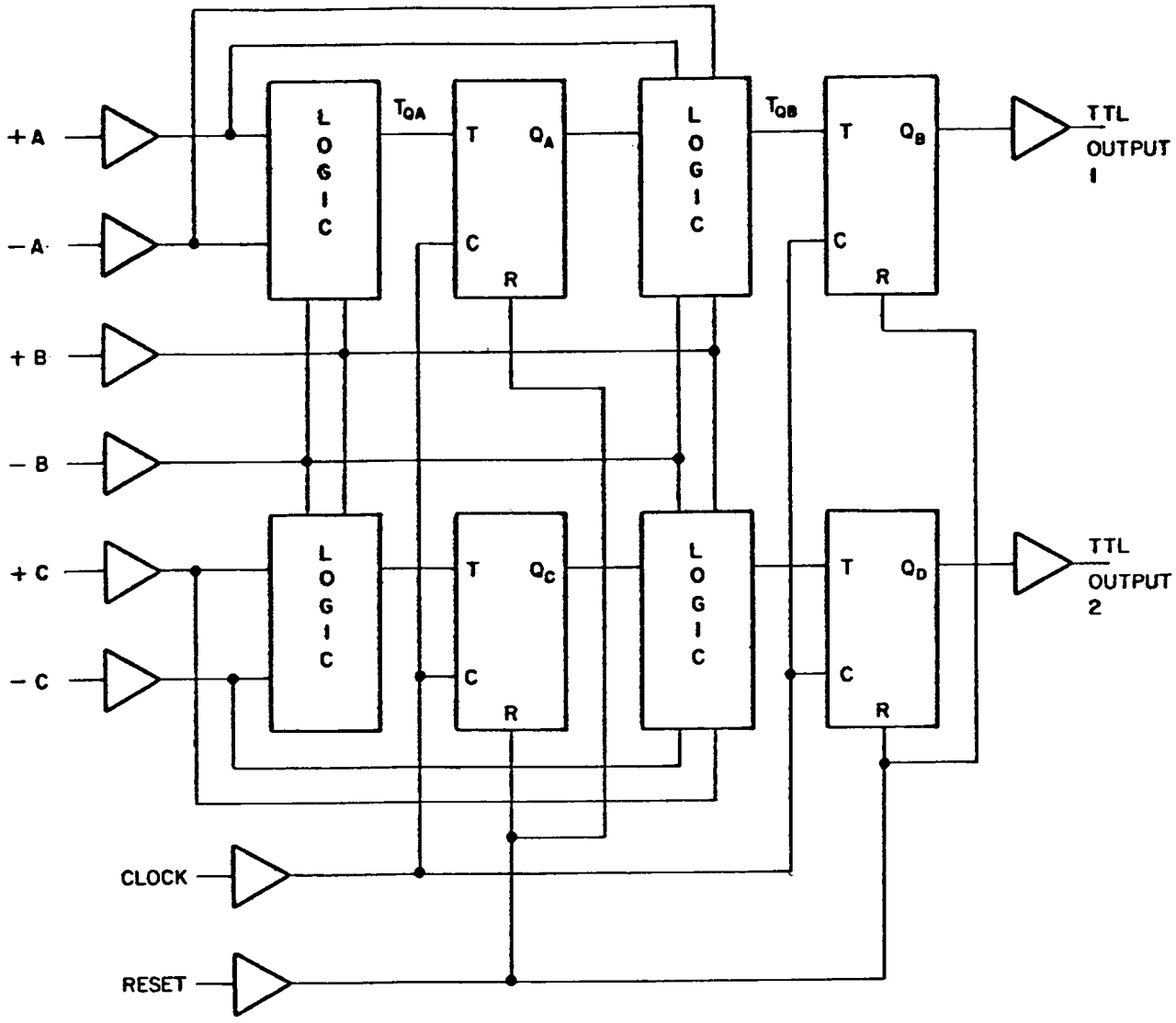
A table giving the quantity to be added to an integration register can be defined for all combinations of correlation between samples of two analog signals:

(+A) (-A) \ (+B) (-B)	01	00	10
01	2	1	0
00	1	1	1
10	0	1	2

This is an offset table that allows unidirectional integration counters to be used. The circuit can be implemented as shown below:



A block diagram of the dual correlator chip is illustrated in Figure 1.



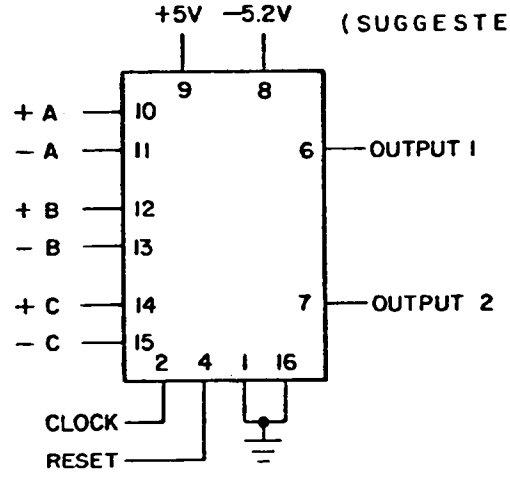


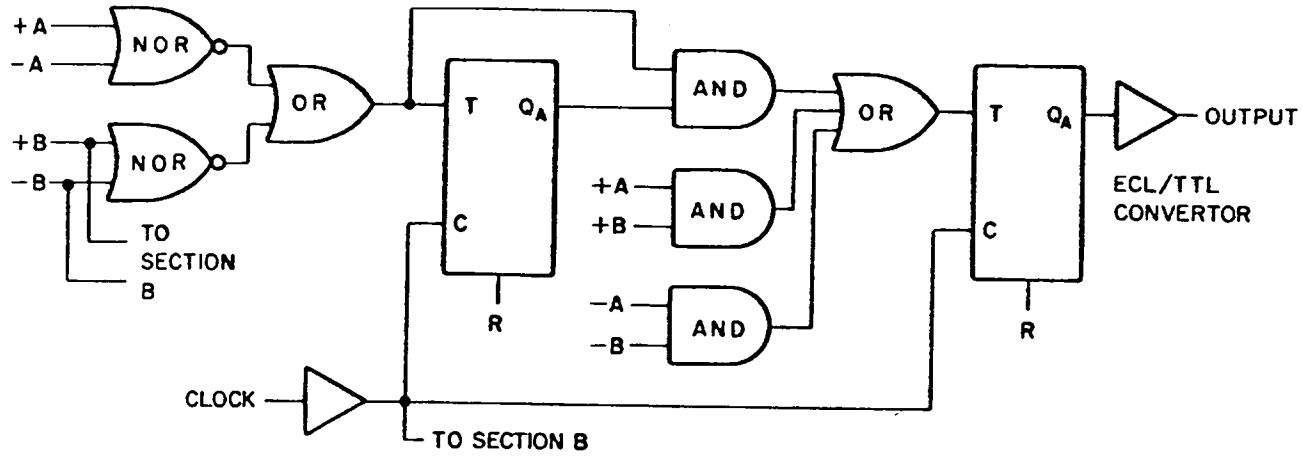
FIGURE 1: VLA-1 DUAL CORRELATOR 1-C

If a T flip-flop is used to implement the function table of Section VI the input equations are:

$$T_{QA} = \overline{(+A) + (-A)} + \overline{(+B) + (-B)}$$

$$T_{QB} = Q_A . T_{QA} + (+A).(+B) + (-A).(-B)$$

Thus one implementation of the desired function is seen in the attached logic diagram. Since a TTL counter is to be used for integration, an ECL to TTL converter has been included.



NATIONAL RADIO ASTRONOMY OBSERVATORY
Post Office Box "O"
Socorro, New Mexico 87801

SPECIFICATION NO. A13800N2 DATE: September 1, 1976

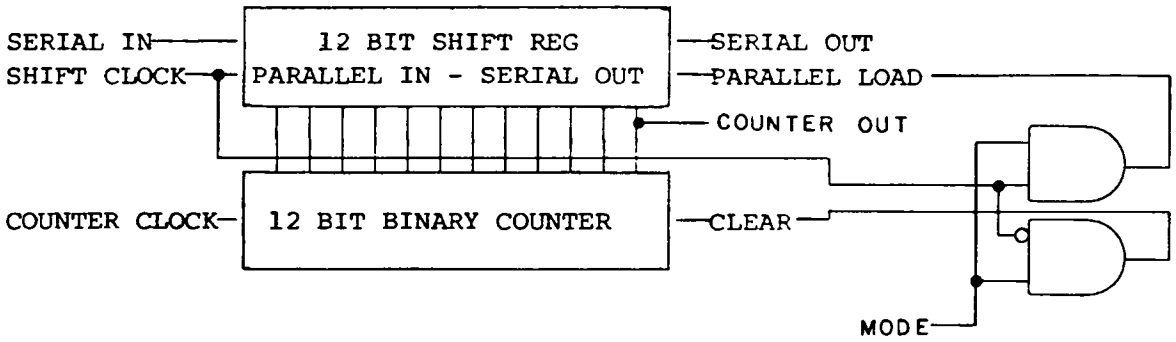
NAME: VLA-2 CUSTOM INTEGRATED CIRCUIT

PREPARED BY: APPROVED BY:

I. INTRODUCTION

This specification defines the operational characteristics of the VLA-2 custom integrated circuit. This chip is to perform in a digital integration application at a 50 MHz clock rate with TTL inputs and TTL output and will be used in the NRAO Very Large Array Radio Telescope.

II. FUNCTIONAL DESCRIPTION



Binary Counter:

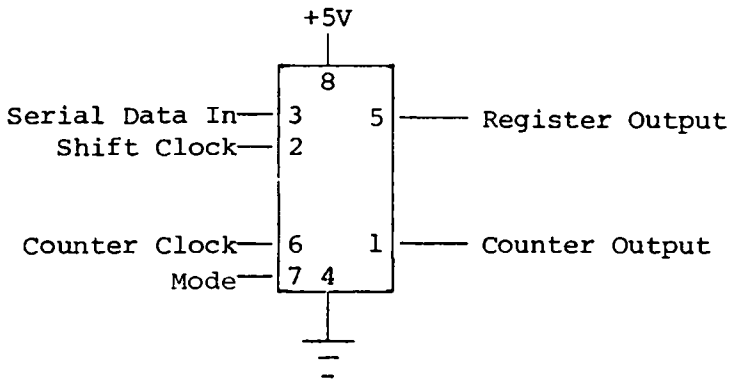
Twelve stages of binary counter are provided whose logic states reflect the binary number of negative transitions applied to the counter clock input since the last clear pulse. Counter overflow occurs at $2^{12} = 4096$. A logic one on the mode input with a logic zero on the shift clock input will reset all stages of this counter to logic zero.

Shift Register:

Twelve stages of shift register are provided by which the logic state of each of the twelve counter flip-flops can be serially accessed. From a known state in the shift register (all logic one's or all logic zero's) the logic states of the twelve binary counter flip-flops can

be parallel loaded into the shift register by application of a logic one on both the mode and shift clock inputs. The positive edges of the shift clock can then unload this binary counter state serially in order, most significant bit first, while the counter is free to perform an independent function. A serial input line permits several VLA-2 IC's to be serially interconnected.

SUGGESTED PIN ASSIGNMENTS



III. PACKAGE

The VLA-2 integrated circuit package will be an 8-pin plastic dual-in-line package. The specific package will be a subject of discussion between the supplier and NRAO and a mutually acceptable decision will be made on the basis of this discussion. The package will have standard 0.3 inch pin spacing with pins on 0.1 inch centers and body length will be such that two units will fit in a standard 16-pin IC socket. The package will be permanently marked on top with the disignation VLA-2.

IV. ENVIRONMENTAL CONDITIONS

The VLA-2 will meet all operational specifications under the following conditions:

1. Temperature: 0 to 70 C moving air blowing at 500 LFPM perpendicular to the dip longitudinal axis.

2. Voltage: +5.0V±5%

3. Power: P_{DISS} = 400 mW MAX at nominal voltage.

The VLA-2 will not be permanently damaged under the following conditions:

1. Temperature:

   A. Storage for 24 hours at -55 to +125 C still air.

   B. Thermal shock: 5 cycles, 60 seconds at OC, 60 seconds at 100 C, 10 seconds transfer time. (Power not applied.)

2. Voltage:

   +6.0V (30 sec transient)

3. Vibration and Shock:

   A. Vibration: 20 Hz to 2 KHz at 20G for 60 seconds.

   B. Shock: 1000G shock in any axis.

V. LOGIC INPUT SPECIFICATIONS

All TTL inputs will be compatible with TTL 74LS series standards. Thus over the operational temperature and supply voltages of Section IV:

LOGIC LEVELS:

$0 \leq$ Logic Zero ≤ 0.8 V

$2.0 \leq$ Logic One ≤ 4 V

INPUT LOADS

I sink ≤ 0.4 MA at $V_{in} = 0.5$ V

I source ≤ 20 µA at $V_{in} = 2$ V

VI. OUTPUT DRIVE

V out ≤ 0.5 V sinking 2 MADC at logic zero

V out ≥ 2.5 V sourcing 100 µADC at logic one

VII. ACTIVE CHARACTERISTICS

A. Toggle Frequency of input counter flip-flop

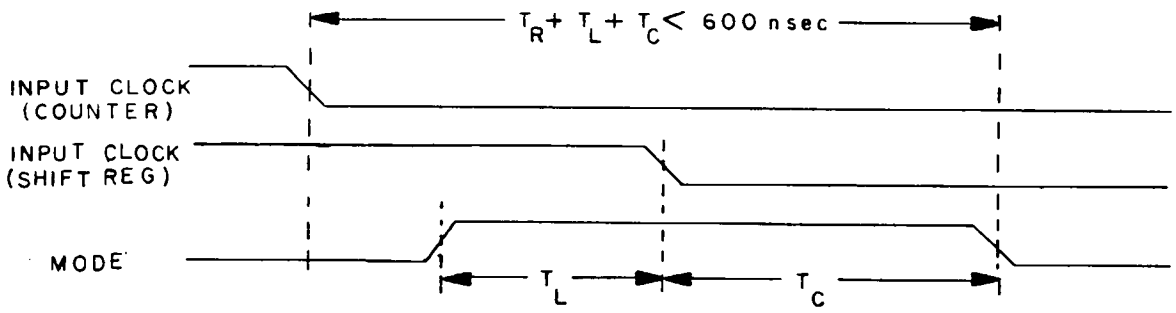
$F_{TOG} = 0$ to 60 MHz, $V_{CC} = 5.00$ V, $T = 25^{o}C$

$F_{TOG} = 0$ to 55 MHz, over section IV range

B. Shift rate of shift register flip-flops

$F_{s} = 0$ to 5 MHz

C. Clear and parallel load pulse width



Where:

T_R = Ripple through time of 12-stage binary counter

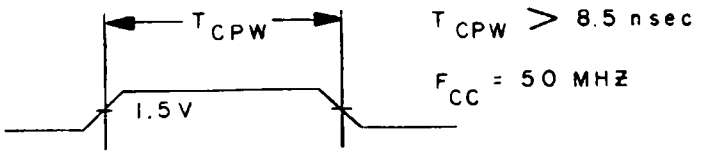
T_L = Load time of shift register

T_C = Clear time of binary counter

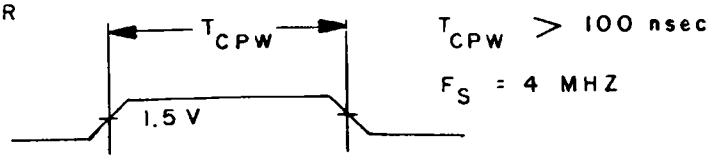
This specification specifies that from the final binary counter clock (negative edge) until the shift register is loaded and the counter reset, less than 600 nsec is required.

D. Clock pulse width

1) COUNTER



2) REGISTER



E. Propagation delay, set-up time, and hold time. (See Section VIII for the load required.)

Define: T_{SU} = minimum required set-up time for data at the serial input to the shift register

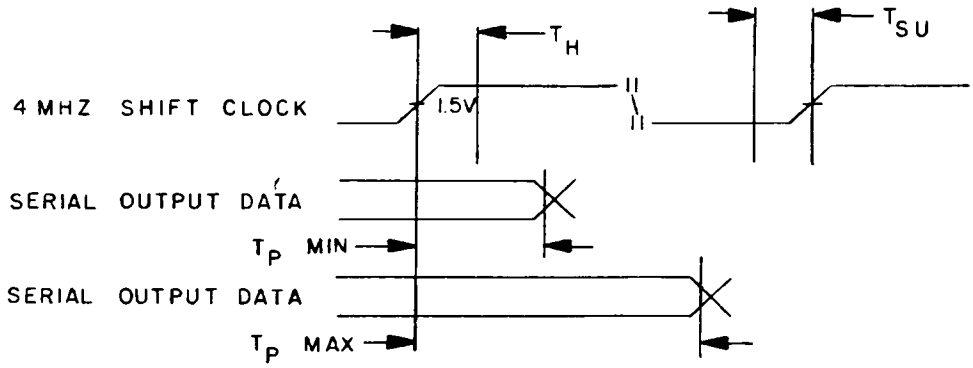
T_H = maximum required hold time for data at the serial input to the shift register

T_P = propagation time from positive edge of shift clock to the serial data output (shift clock = 4 MHz)

Then the following realtions must hold between the defined parameters:

$$T_{P_{min}} > T_H + 5 \text{ nsec}$$

$$T_{P_{max}} < 250 \text{ ns} - T_{SU} - 20 \text{ nsec}$$



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In general, a fixture as shown will be used in IC dynamic testing.