COMBINING THE VLA CONTINUUM AND SPECTRAL LINE CORRELATORS

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I. SCOPE

This paper describes the modifications needed to fit the present continuum delay/multiplier system to accomplish spectral line observations. Two design options are discussed: the first defines the instrument obtained if a minimum of changes are made to the continuum system; the second will discuss increasing the number of multipliers to obtain greater frequency resolution from the spectral line system.

In the discussion that follows system specifications, a design plan, and cost and manning estimates will be presented.

II. SPECIFICATIONS

Some changes to the present continuum system specifications will result in the modifications required for line work. Since a recirculation scheme is proposed to accomplish line observation, a trade-off between recirculator size and dump time frequency is encountered. The proposed recirculator size, programmable from 65536 to 131072 bits, will require dump times between 0.655 and 1.31 msec, thus requiring approximately 80 to 40 dumps per 19.2 Hz cycle. At 25 μsec per dump the observational efficiency, in continuum, will be 93% to 95% as opposed to the present 97%.

The degradation in observational efficiency above is offset in allowing dump time to be synchronized with rapid time varying sources. The dump time being variable, in 10 nsec increments, from .655 to 1.31 msec, will allow recording data in time channels that are fractional portions of a variables period. The 512 hardware channels (256 frequency channels) of memory provided

for spectral line operation will allow division of the variables period into 32 time channels over a 100 MHz bandwidth or 64 at a 50 MHz bandwidth.

Some changes in equipment details will also occur. The complete redundancy of self-multiplier, in continuum, will be eliminated so that half of the self-multipliers can be used as V_s counters.

In addition, self-test and sin x cos multiplication will change such that 12 antenna loops will replace the present 27 antenna loops in the time multiplexing self-test and sin x cos functions. No sin x cos multiply redundancy will be provided. Also the pseudo-random data generator now used in the multiplier test function will be applied into the system at the delay line front end making this test a more system-wide test and also making the delay line test functional even if active sampler data is not available.

The spectral line specifications are given with two options reflecting the present amount of hardware in the delay/multiplier design or an add-on of two additional racks of multipliers to increase the number of frequency channels.

The various factors that will affect the operational specifications of spectral line operation are given below:

1. RECIRCULATION FACTOR, N:

    Design A:

    Bandwidth = 50/N MHz

    Frequency Channel = 8 N

    Design B:

    Bandwidth = 50/N MHz

    Frequency Channel = 13 N

    Where N = any integer

2. POLARIZATION FACTOR, K:

Bandwith = 50/N MHz

Frequency Channel $= \frac{8N}{K}$ or $\frac{13N}{K}$

Where K = 4 for all multiplies

R x R

R x L

L x R

L x L

Or K = 2 for all multiplies

R x R

L x L

By a very simple recabling of delay line inputs the above option could yield sin - cosine separation.

3. ARRAY FACTOR, L:

Bandwidth = 50/N MHz

Frequency Channel = 8LN or 13LN

Where L = 1 for a 27 antenna array

L = 4 for a 13 antenna array

4. EFFICIENCY FACTOR, M:

Bandwidth = 50/N

Frequency Channel = 8 (N+M) or 13 (N+M)

Where the observational efficiency is $95 \frac{N}{N+M}$ %.

Thus:

Bandwidth = 50/N

Frequency Channel = $\frac{8(N+M)(L)}{K}$ or $\frac{13(N+M)(L)}{K}$

Where

N = Recirculation Factor = any integer

M = Efficiency Factor = any integer (efficiency = $95 \frac{N}{N+M}$ %)

L = Array Factor = 1 for 27 antenna array

 = 4 for 13 antenna array

K = Polarization Factor = 1 for no polarization

 = 2 for SxS or RxR

 CxC   LxL

 = 4 for SxS or RxR

 SxC   RxL

 CxS   LxR

 CxC   LxL

In any case frequency channel = 256 maximum and

where $\frac{8(N+M)(L)}{K}$ > 256 oversampling occurs.

III. DESIGN PLAN

In concept, the recirculation approach to the spectral line correlator system will use the delay/multiplier continuum system by time sharing the high speed multipliers to perform multiple correlations on low speed data. Thus the 5616 hardware channels implemented in the continuum system will provide 8 frequency channels each time data stored in the recirculator is run past the multipliers. A block diagram of one approach to a recirculation system is given in Figure 1.

```
┌─────────────────┐              ┌─────────────────┐              ┌─────────────────┐
│   100 MHZ       │  100 MHZ     │   100 MHZ       │ 100 MHZ DATA │  SELECT EACH    │  100/N MHZ
│   SAMPLERS      │──DATA───────▶│   DELAY LINE    │─────────────▶│  Nᵗʰ BIT        │   DATA
│                 │              │                 │         N ──▶│                 │
└─────────────────┘              └─────────────────┘              └─────────────────┘
```

```
            ┌─────────────────────┐
            │  K BIT MEMORY       │
       ○    │  LOADED AT          │
       ○    │  100/N   MHZ        │              ┌─────────────────┐
            └─────────────────────┘         ○    │   100 MHZ       │        TO
                                                 │   MULTIPLIER    │────▶  COMPUTER
       ○    ┌─────────────────────┐    ○         │                 │
       ○    │  K BIT MEMORY       │              └─────────────────┘
            │  READ N TIMES       │
            │  AT 100 MHZ         │
            └─────────────────────┘
```

MULTIPLIER SYSTEM PRODUCES
8 FREQUENCY CHANNELS FOR
EACH PASS THRU THE MEMORY
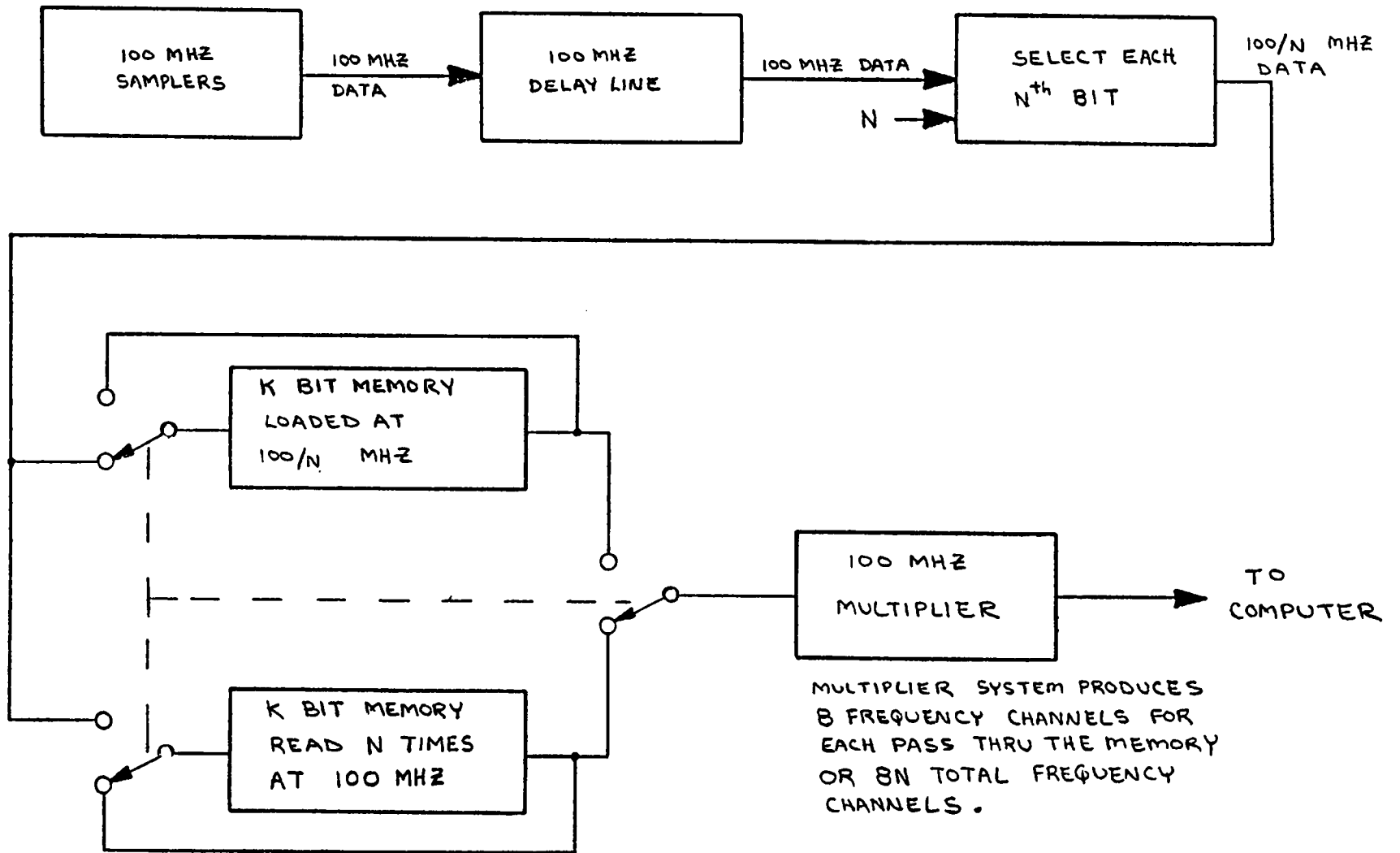OR 8N TOTAL FREQUENCY
CHANNELS.

FIGURE 1 : BASIC RECIRCULATOR SYSTEM

The configuration of the present continuum multiplier system divides each 50 MHz section into eight mother boards of 27 P.C. cards each. Each mother board implements $\frac{27 \times 26}{2}$ multiply channels in an array illustrated in Figure 2A.

```
 1 x
 2 x x
 3 x x x
 4 x x x x
 5 x x x x x
 6 x x x x x x
 7 x x x x x x x
 8 x x x x x x x x
 9 x x x x x x x x x
10 x x x x x x x x x x
11 x x x x x x x x x x x
12 x x x x x x x x x x x x
13 x x x x x x x x x x x x x
14 x x x x x x x x x x x x x x
15 x x x x x x x x x x x x x x x
16 x x x x x x x x x x x x x x x x
17 x x x x x x x x x x x x x x x x x
18 x x x x x x x x x x x x x x x x x x
19 x x x x x x x x x x x x x x x x x x x
20 x x x x x x x x x x x x x x x x x x x x
21 x x x x x x x x x x x x x x x x x x x x x
22 x x x x x x x x x x x x x x x x x x x x x x
23 x x x x x x x x x x x x x x x x x x x x x x x
24 x x x x x x x x x x x x x x x x x x x x x x x x
25 x x x x x x x x x x x x x x x x x x x x x x x x x
26 x x x x x x x x x x x x x x x x x x x x x x x x x x
27 x x x x x x x x x x x x x x x x x x x x x x x x x x x
```

Antenna → ▲ 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2
x outputs   0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7
from delay
lines *

Antenna
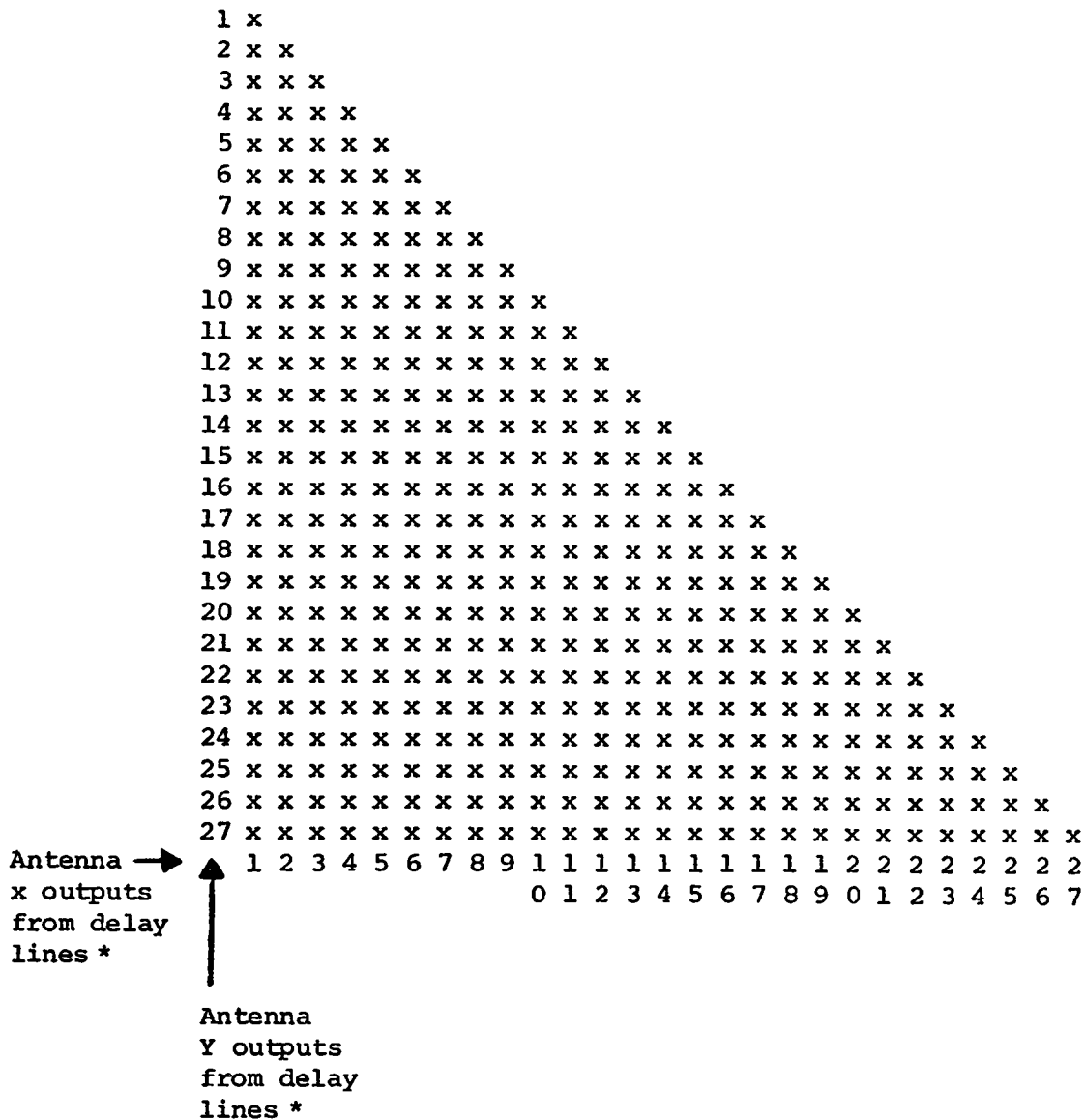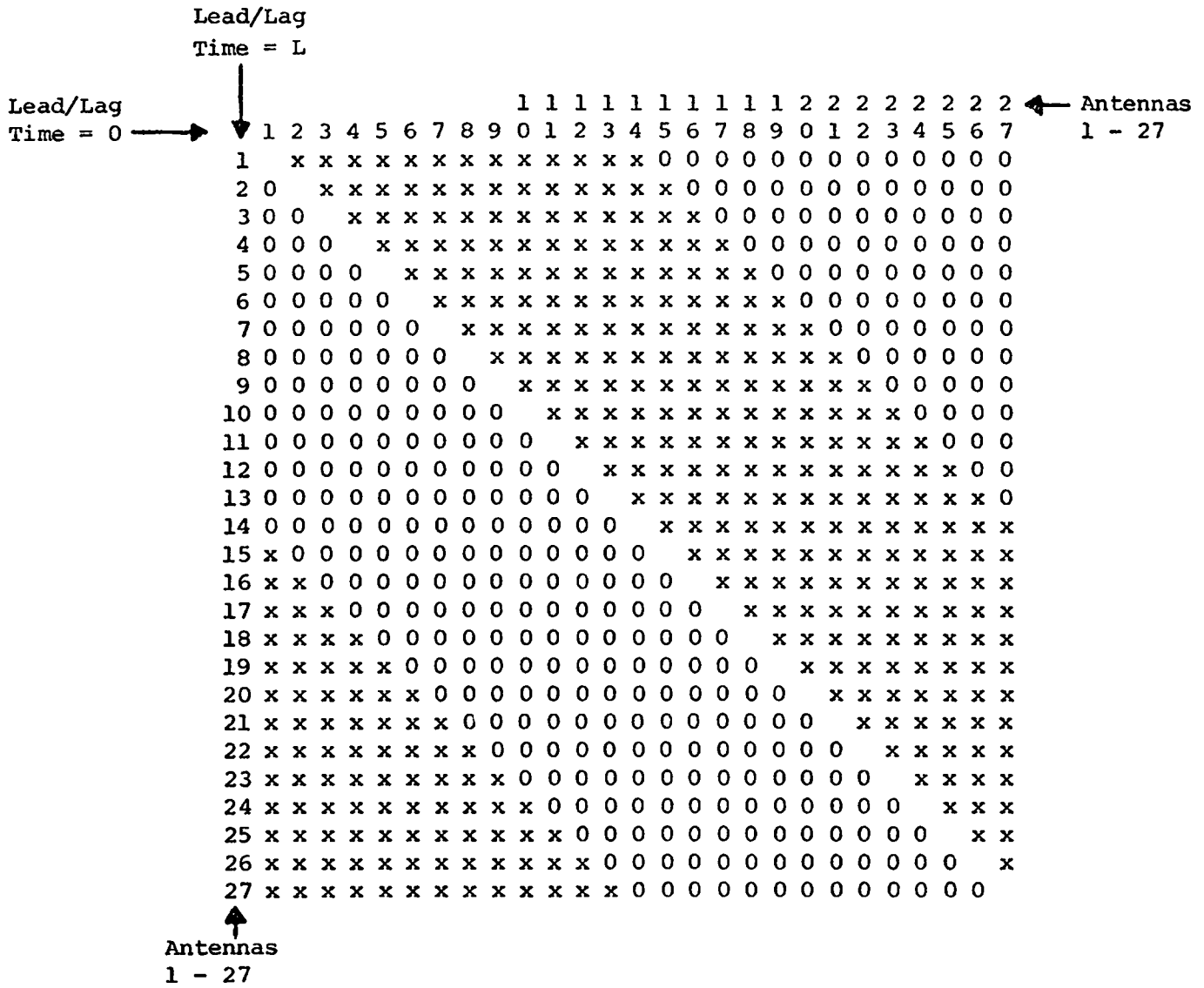Y outputs
from delay
lines *

Figure 2A

* See Figure 3B

An orthogonal implementation of this half matrix was maintained throughout

multiplier, delay and cabling interconnect systems. Thus Figure 2B displays

a complete array of correlators obtained for one lead, or lag channel by

combining two mother boards to produce a full 26x27 point matrix. Hardware

is available in the continuum system to produce eight such arrays, thus

performing eight lead or lag channels at a time, and for a recirculation factor

of $N = 20$: 160 frequency channels are produced at a 2.5 MHz bandwidth. With

the addition of ten more mother boards, associated delay line fan-out and cables

$N = 20$ would result in 260 frequency channels at 2.5 MHz bandwidth. Both of

these options are priced out in the last portion of this paper.

```
                              1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2      Antennas
                   1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7   1 - 27
            1    x x x x x x x x x x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0
            2  0   x x x x x x x x x x x x x 0 0 0 0 0 0 0 0 0 0 0 0
            3  0 0   x x x x x x x x x x x x x 0 0 0 0 0 0 0 0 0 0 0
            4  0 0 0   x x x x x x x x x x x x x 0 0 0 0 0 0 0 0 0 0
            5  0 0 0 0   x x x x x x x x x x x x x 0 0 0 0 0 0 0 0 0
            6  0 0 0 0 0   x x x x x x x x x x x x x 0 0 0 0 0 0 0 0
            7  0 0 0 0 0 0   x x x x x x x x x x x x x 0 0 0 0 0 0 0
            8  0 0 0 0 0 0 0   x x x x x x x x x x x x x 0 0 0 0 0 0
            9  0 0 0 0 0 0 0 0   x x x x x x x x x x x x x 0 0 0 0 0
           10  0 0 0 0 0 0 0 0 0   x x x x x x x x x x x x x 0 0 0 0
           11  0 0 0 0 0 0 0 0 0 0   x x x x x x x x x x x x x 0 0 0
           12  0 0 0 0 0 0 0 0 0 0 0   x x x x x x x x x x x x x 0 0
           13  0 0 0 0 0 0 0 0 0 0 0 0   x x x x x x x x x x x x x 0
           14  0 0 0 0 0 0 0 0 0 0 0 0 0   x x x x x x x x x x x x x
           15  x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x x x x x x x x x x x
           16  x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x x x x x x x x x x
           17  x x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x x x x x x x x x
           18  x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x x x x x x x x
           19  x x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x x x x x x x
           20  x x x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x x x x x x
           21  x x x x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x x x x x
           22  x x x x x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x x x x
           23  x x x x x x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x x x
           24  x x x x x x x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x x
           25  x x x x x x x x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x x
           26  x x x x x x x x x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0   x
           27  x x x x x x x x x x x x x 0 0 0 0 0 0 0 0 0 0 0 0 0
```

Antennas
1 - 27

Where L = 0 thru 7   or 8 thru 15   or 16 thru 23   - - -

0 indicates multiplications done in System A

x indicates multiplications done in System B

Figure 2B

Figure 3A is a per-antenna breakdown of the continuum delay system.
Each antenna supplies digital inputs, at a 100 MHz bit rate, to eight delay
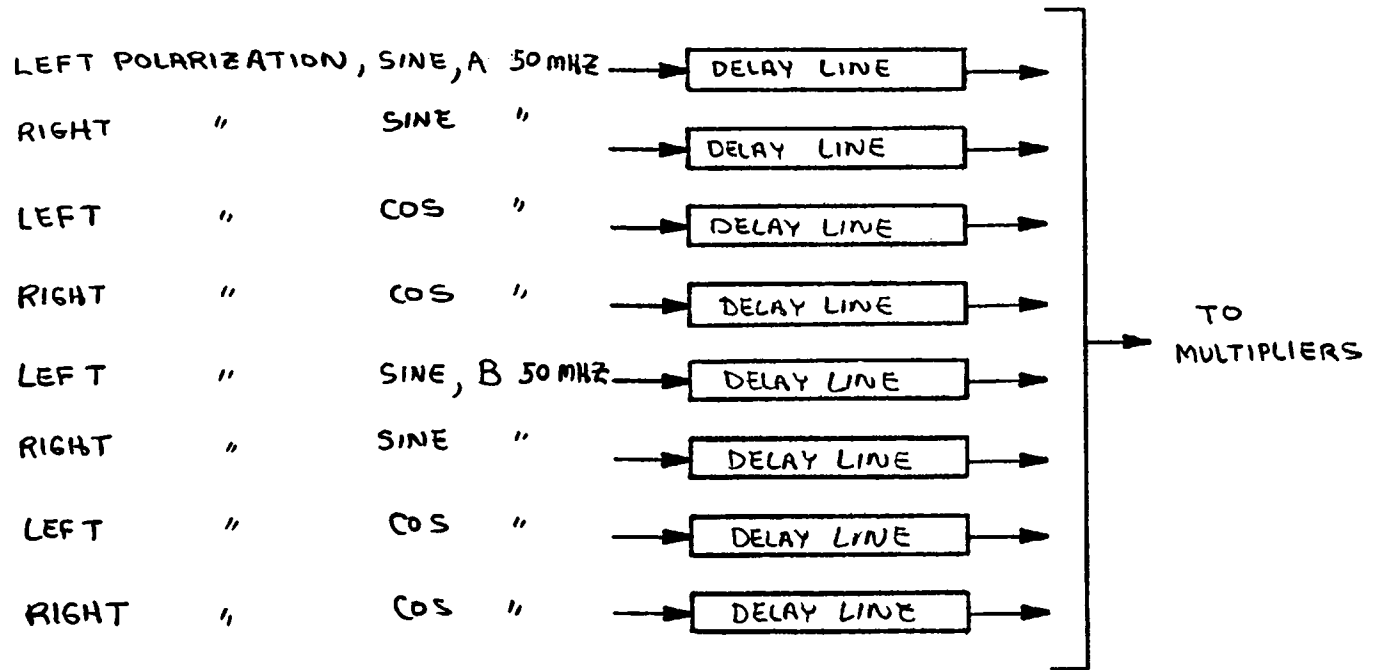lines (four in each 50 MHz system).

LEFT POLARIZATION, SINE, A 50 MHz → DELAY LINE →

RIGHT   "   SINE   " → DELAY LINE →

LEFT   "   COS   " → DELAY LINE →

RIGHT   "   COS   " → DELAY LINE →

LEFT   "   SINE, B 50 MHz → DELAY LINE →

RIGHT   "   SINE   " → DELAY LINE →

LEFT   "   COS   " → DELAY LINE →

RIGHT   "   COS   " → DELAY LINE →

TO MULTIPLIERS

FIGURE 3A : CONTINUUM DELAY SYSTEM PER ANTENNA

Figure 3B gives a breakdown of a delay line card into an input stage, delay memory, and an output stage. The present delay line consists of 16 stages of discrete 512 bit delay, 16 stages of discrete 256 bit delay, and 16 stages of 512 bit storage with a 257 to 512 bit variable thru-put time. For a combined line-continuum system it is proposed that a new delay line with 16 stages of 2048 bit storage with a 1025 to 2048 bit variable thru-put time be designed. This modification will make a more expensive but more compact delay line with a total potential storage of 32768 bits.
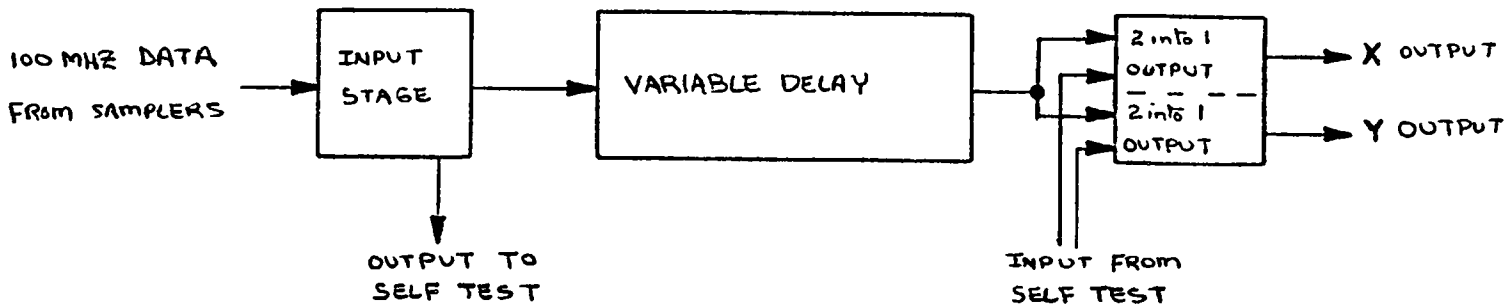
FIGURE 3B: DELAY LINE CARD BREAKDOWN

In the proposed spectral line delay/correlator system each antenna will supply digital data to only one delay line. Thus the storage capacity of seven delay lines per antenna is available to supply recirculator memory. Figure 4 displays how eight delay lines are interconnected to form a recirculator. Each of the delay line memory blocks labeled "recirculator memory" had previously been filled in turn at the 100/N MHz rate. When the block presently being loaded at 100/N MHz is full, the five delay lines that constitute the recirculator will be reconfigured such that the delay line with the oldest data will start being loaded at the 100/N MHz rate and the delay line shown being loaded will be inserted into the four delay line recirculator loop. All switching is done electronically at a speed such that the four seriesed recirculator delay lines contain a continuous record of 131,000 bits of antenna data.
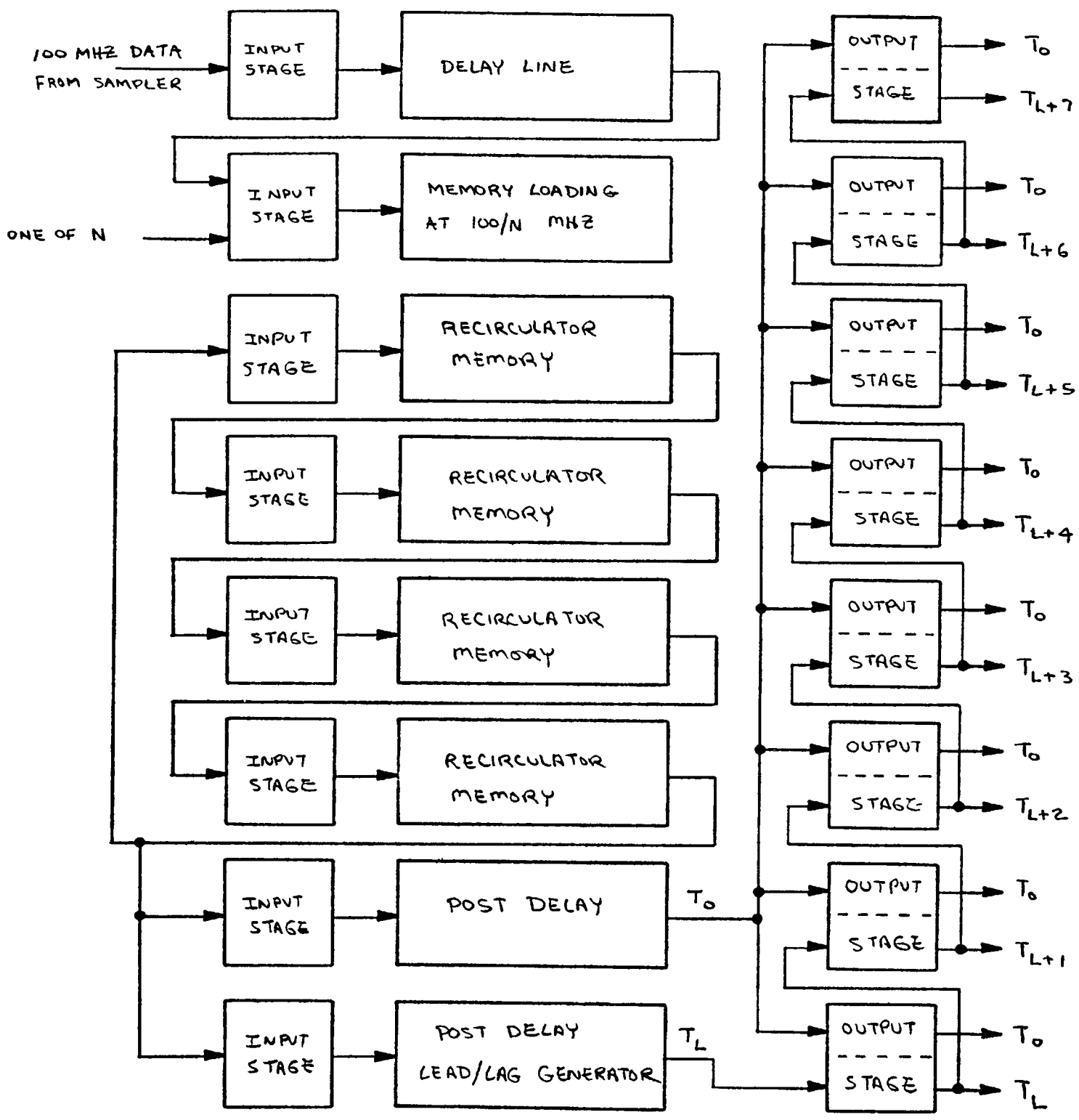
FIGURE 4: BASIC 8 DELAY LINE RECIRCULATOR

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Figure 4 is in error in one respect. That is that each delay line output stage has outputs to two multiplier mother boards. Thus a more accurate representation, complete with continuum designations on the delay lines is given in Figure 5. The post delay function yields the lead-lag delays times. Since these hardware paths are delay lines, the differential delays in the T_O and T_L paths will be changed by eight (or 13) each time the recirculator data is run through. Note that the delay line can feed data into any of the five recirculator memory blocks and that each recirculator block can feed data into the other four blocks. The post delay blocks in turn can accept data from any of the five recirculator blocks. Hence any interconnection is possible. The configuration will always be under the system controller's control.
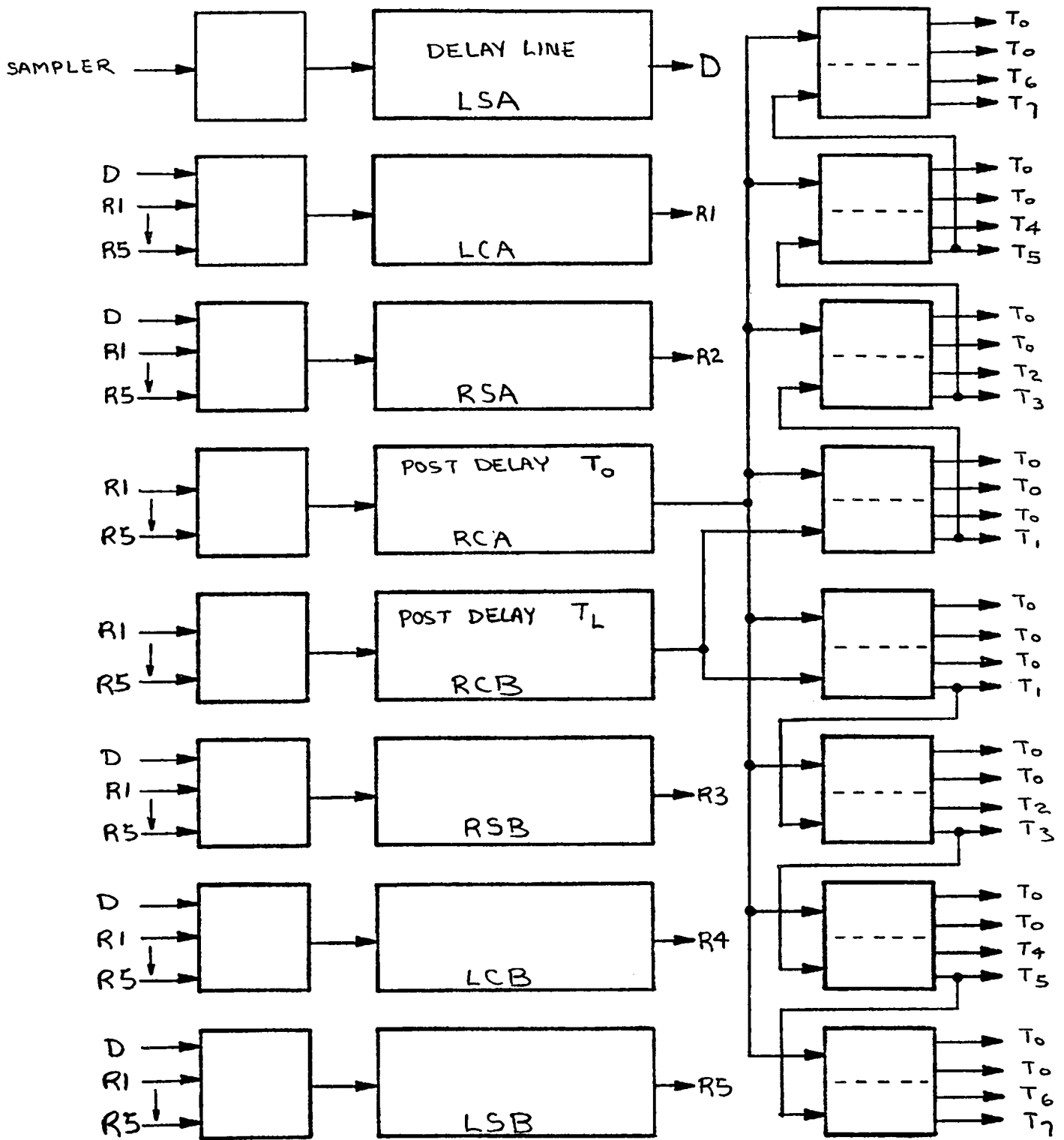
FIGURE 5 : EIGHT DELAY LINE RECIRCULATOR

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Figure 6 displays one of the left-right polarization options (RxR and LxL). In this configuration, since only one delay line is available for the post delay function, 1/N of the time must be spent in filling the post delay memory with current data. Thus the observational efficiency goes down by the factor $\frac{N-1}{N}$.
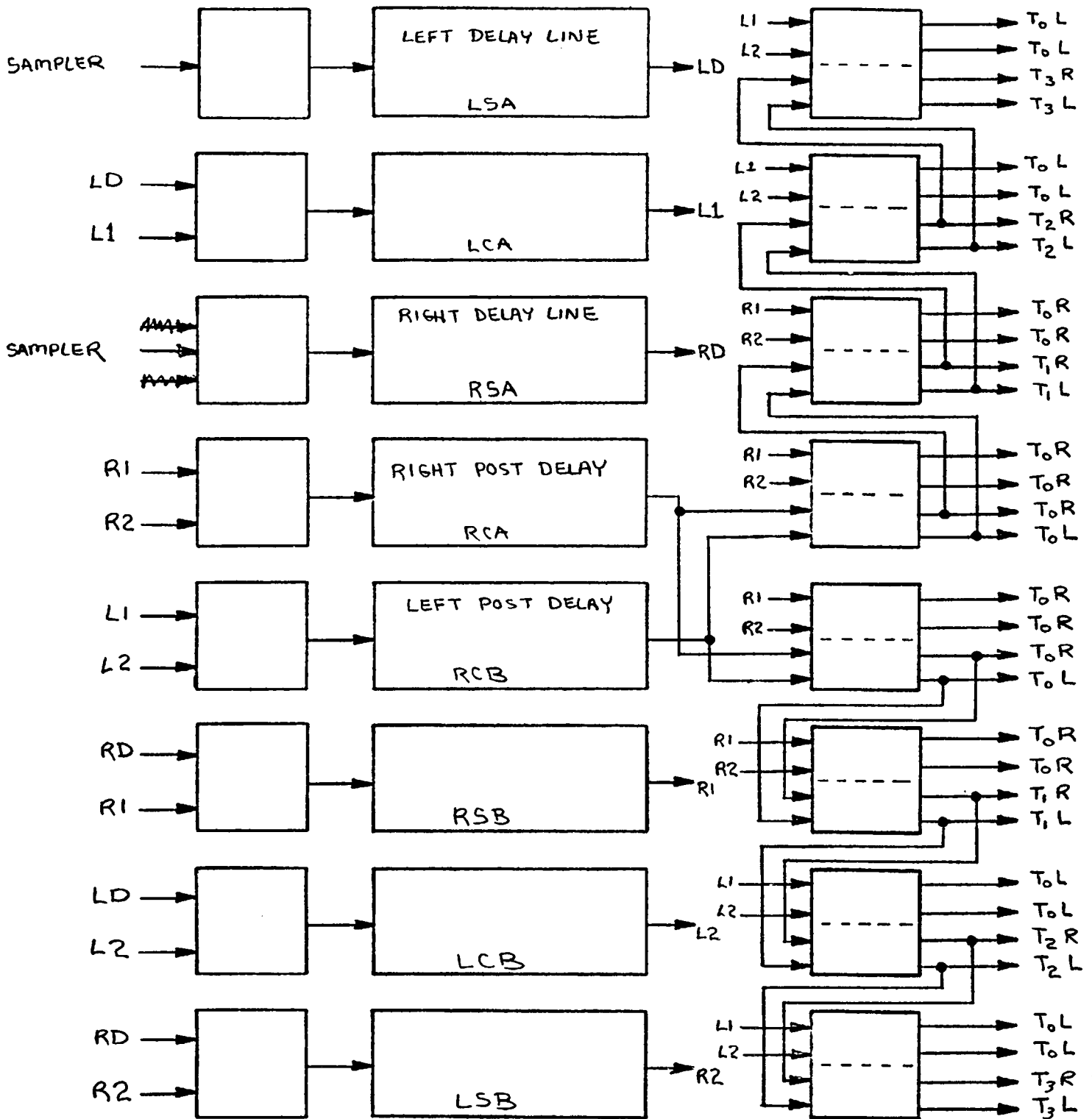
Figure 6

RxR and LxL Polarization Option Example

Figures 7 and 8 display the input and output functions required to accomplish all options denoted in the Specifications Section.
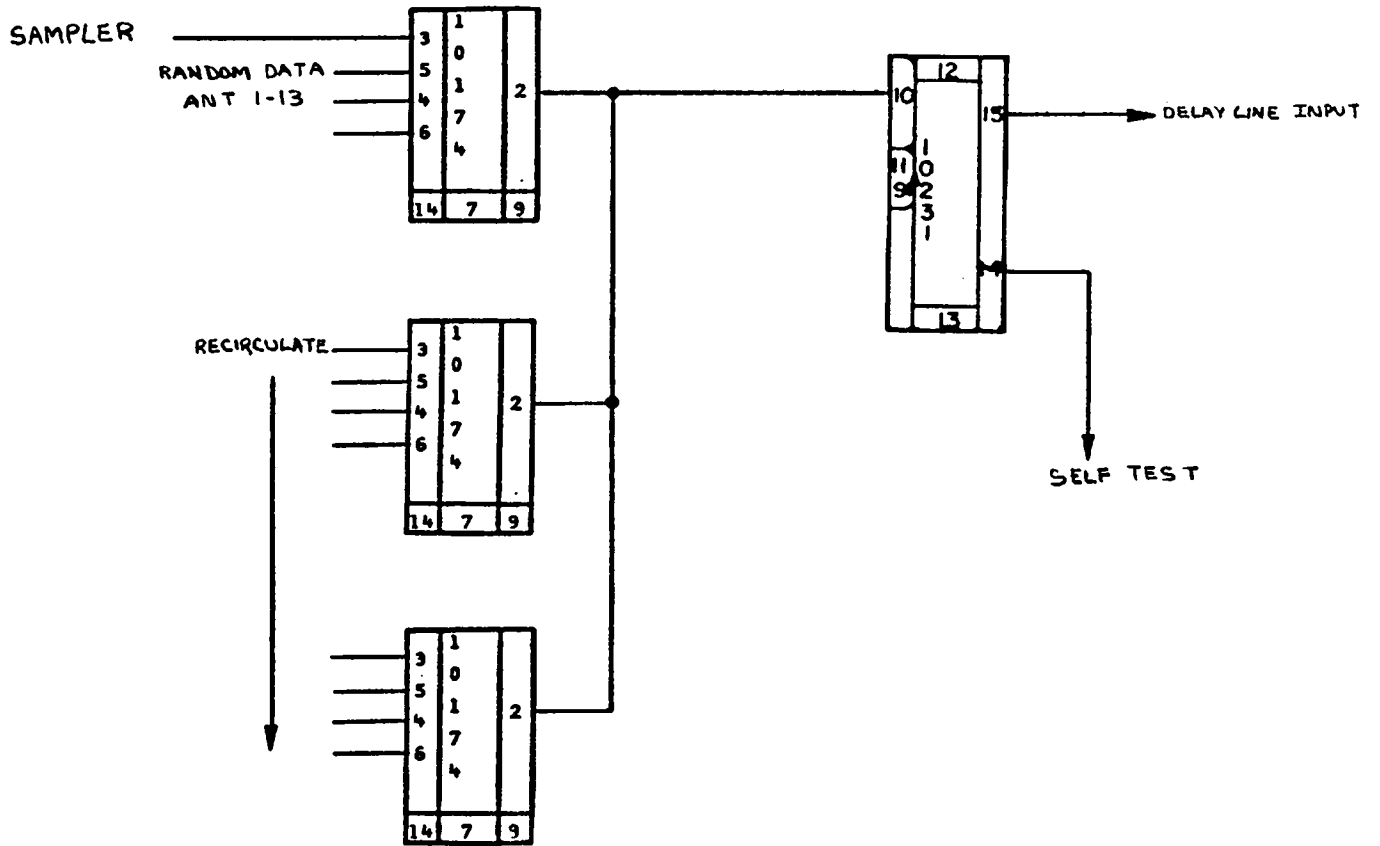
Figure 7

DELAY LINE INPUT STAGE
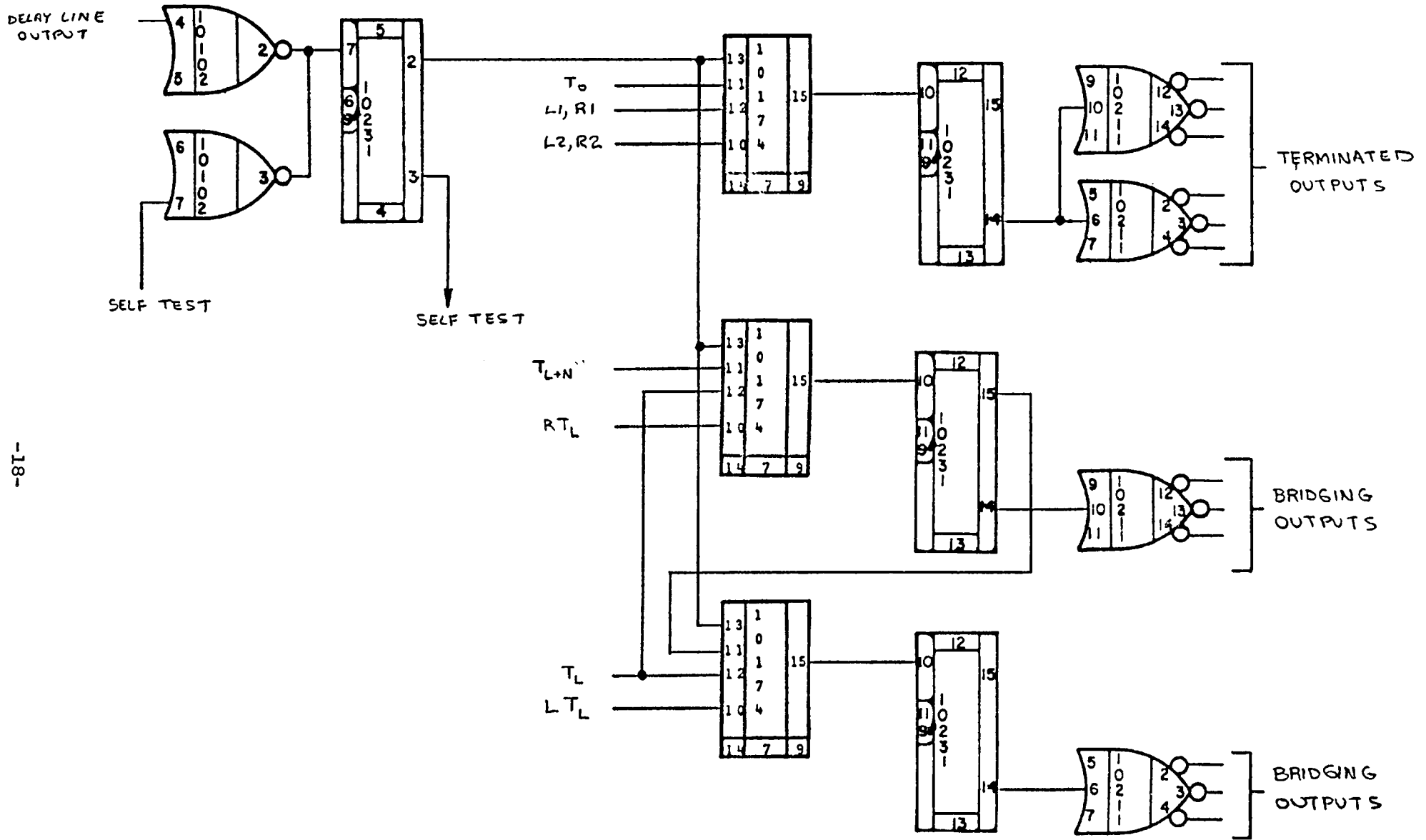
FIGURE 8 : DELAY LINE OUTPUT STAGE

To accomplish the switching required for implementation of the system described thus far, it is important that all eight delay lines associated with any given antenna be located on the same mother board. This is possible within the present system if a 1 for 2 reduction in delay line cards can be made by doubling the logic to fit two delay lines on each multilayer card. In addition, incorporating the control card logic on these new cards will be attempted to reduce the mother board interconnects. Thus new delay line cards and delay mother boards will be required, but with only a minimal redesign from the present proven design. Multi-layer, micro-strip card and mother board design will be retained in these new cards.

The multiplier system will require only minimum modifications. A recirculator size of 131,000 bits will permit a bit round-off in the integration result given by:

$$2^{N+3} = \overline{)FT} - \overline{) \text{ No. Bits in Recirculator}}$$

Where: N = # Bits of integration thrown away

F = Sample frequency

T = Integration time

Thus for a 131,000 bit memory:

N = 5.5

In order to accomplish this requirement two more bits must be brought off of the present multiplier card.

When utilizing right and left polarization data the recirculator size goes to 32,768 bits and 4.5 bits must be retained. Thus if only two additional bits are brought off the multiplier card, one half bit will be lost.

The self-test, self-healing function of the new delay system will be accomplished by using a standard delay mother board (hand modified) and two standard delay lines to monitor/replace the delay lines of each mother board. The input and output multiplex functions displayed in Figures 7 and 8 will accomplish the function of the present input-output MUX cards. Thus a 12-delay line loop in self test and sin x cos functions will replace the present 27-delay line loop.

Due to the short dump time the present Low Speed Integration logic will not be needed. All integration between dumps into Temporary Storage will be performed by the High Speed Integrator cards. Thus extensive changes, but mostly simplifications, will be required to be made to the integration and integration control logic. The addition of ten more multiplier mother boards will require additional High Speed Integration logic which probably will not fit easily into the present scheme. These cards will probably be interconnected in an independent integration system.
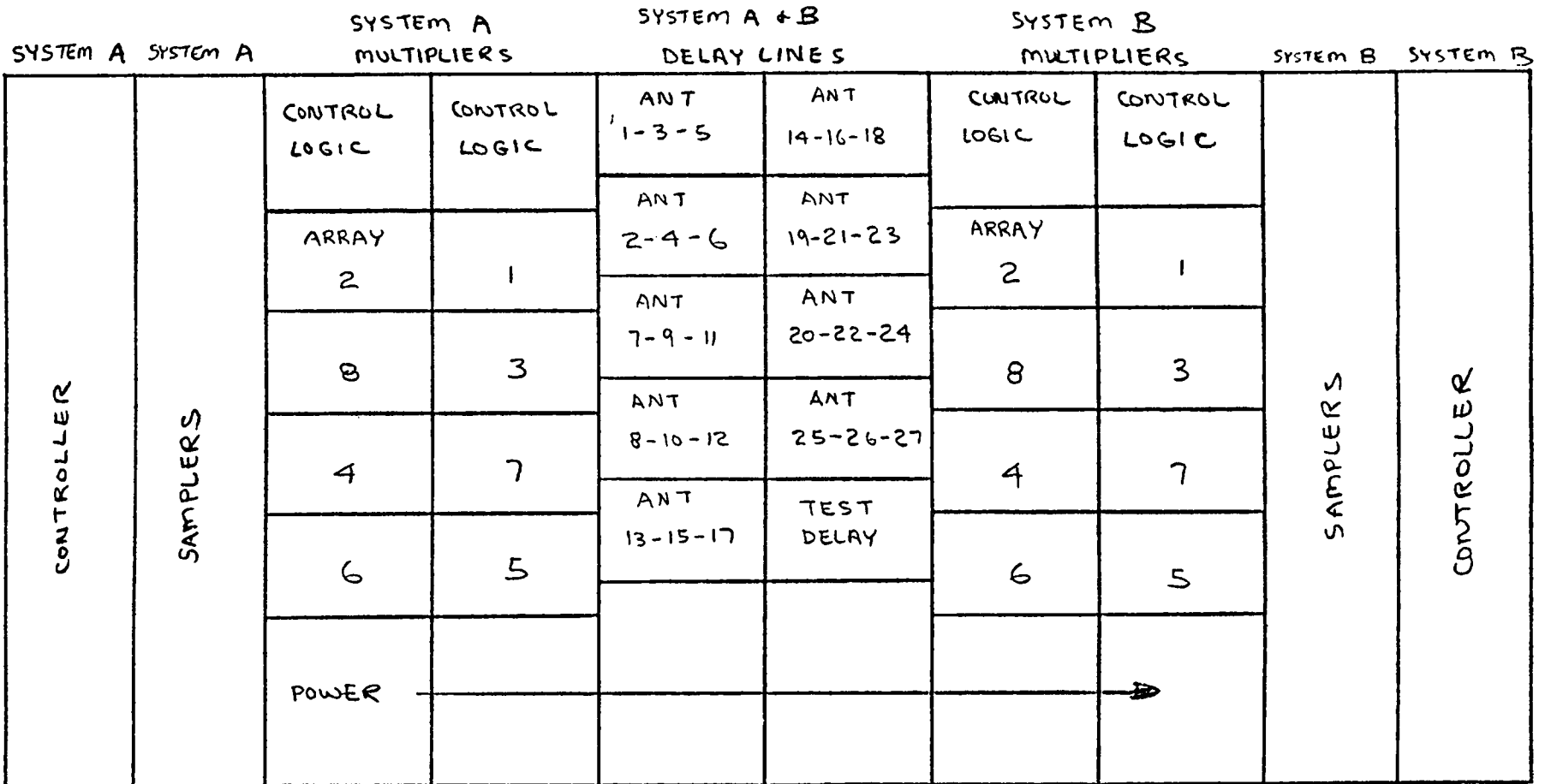
A new functional requirement for the new system, both in continuum and line, will be to store ten seconds of observational data between data dumps into the computer.. This integration will take place in the System Controller from the data output of the Temporary Storage. Since 256 frequency or 512 hardware channels must be stored, the correlators will produce 256/8 dumps of 6066 words. A full ten seconds of integration will produce up to a 25 bit word (actually much less on the average), thus requiring integration/storage of approximately 200,000 25 bit words. As only 6066 words are applied each 1.31 msec dump (3033 for each 50 MHz system), present 16 K RAM memory would be fast enough for this application requiring a memory of just over 300 16 K RAM's. The design of this memory seems fairly straightforward, although dump into the computer might require a 50 msec period each ten seconds that would

be lost for observation. The addition of the ten extra multiplier mother boards will of course expand the figures above by the appropriate factor.

The System Controller for this new system would require a complete redesign. New responsibilities, such as recirculator configuration control, have been added which probably strongly indicate a mini computer would be required in the System Controller. Either a single System Controller or two (corresponding to the present 50 MHz division of the present 100 MHz continuum system) communicating controllers could be used. The new System Controller(s) require by far the most new design effort in applying the continuum system design to line work.

It would be possible, but with some effort to maintain the complete independence of all functions including power supplies of the two 50 MHz halves of the 100 MHz continuum system. Although delay line cards from the two systems will be present on the same mother boards, separate power distribution can still be maintained.

Figure 9 illustrates the proposed system layout. Two System Controllers are shown although one could be designed to do both functions.

SYSTEM A	SYSTEM A	SYSTEM A MULTIPLIERS		SYSTEM A & B DELAY LINES		SYSTEM B MULTIPLIERS		SYSTEM B	SYSTEM B
CONTROLLER	SAMPLERS	CONTROL LOGIC	CONTROL LOGIC	ANT 1-3-5	ANT 14-16-18	CONTROL LOGIC	CONTROL LOGIC	SAMPLERS	CONTROLLER
		ARRAY 2	1	ANT 2-4-6	ANT 19-21-23	ARRAY 2	1		
		8	3	ANT 7-9-11	ANT 20-22-24	8	3		
		4	7	ANT 8-10-12	ANT 25-26-27	4	7		
		6	5	ANT 13-15-17	TEST DELAY	6	5		
		POWER ⟶					⟶		

MULT
MULT
MULT
MULT
MULT
POWER

POSSIBLE ADD ON MULTIPLIER RACKS

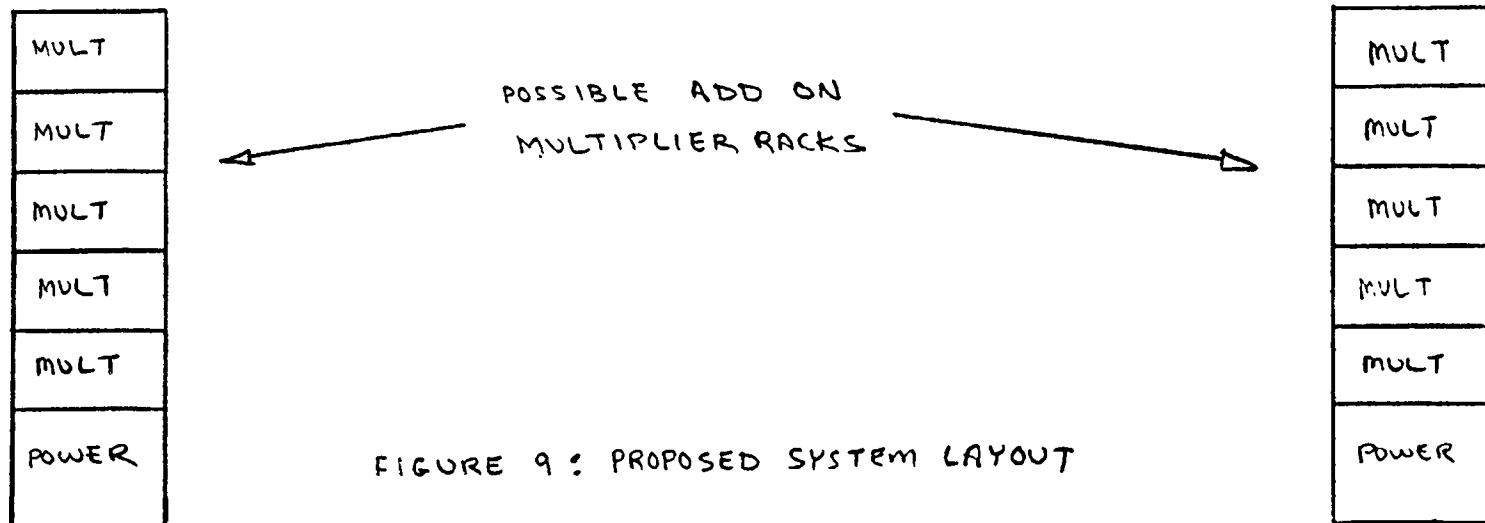| MULT |
|---|
| MULT |
| MULT |
| MULT |
| MULT |
| POWER |

FIGURE 9 : PROPOSED SYSTEM LAYOUT

IV. COST AND DESIGN TIME EFFORT

The estimate in Table I is based on the 1975 cost estimate of the continuum system. Component prices come mainly from component prices encountered in ordering for the six-antenna delay/multiplier system.

Table II gives the add-on cost of ten additional multiplier mother boards to accomplish 256 frequency channels at 2.5 MHz bandwidth.

Table III is a design time estimate.

Unit			Present	Spectral Line	Already Expended On Six Ant. Sys.
SAMPLER:			$ 84K	$ 84K	$ 9.3K
DELAY SYSTEM:	Delay Cards	432 @ $85	36.7K		
		216 @ $100		21.6K	–
	Parts	432 @ $145	62.6K		
		216 @ $375		81K	4K
	Assy. & Test	432 @ $62	26.8K		
		216 @ $100		21.6K	–
	Control Cards	56 @ $285	16.0K	0	
	Mother Boards	20 @ $610	12.2K		–
		10 @ $800		8K	
	Cables		3.4K	3.4K	–
	Self Test				
	Cards	20 @ $290	5.8K		
		18 @ $575		10.35K	–
	Cables	216 @ $37.73	8.15K		
		50 @ $37.73		1.88K	–
	Miscellaneous		10.0K	20.0K	–
WIRING MATRIX:	Cables & Multiplier Mother Boards		35.71K	35.71K	15K
MULTIPLIER SYSTEM:	Multiplier Cards	432 @ $328	142K		
		432 @ $330		142K	15K
INTEGRATION LOGIC:	H.S.I. Cards	80 @ $350	28K		
		80 @ $350		28K	4K
	L.S.I. Cards	8 @ $805	6.44K		
		0		0	–
	Storage & Cont.		6.2K	6.2K	3K
SYSTEM POWER:			22.6K	22.6K	10K
SYSTEM CONTROLLER:			20K		
	10 Second Storage			40K	–
RACKS:	8 large @ $463		3.7K		
	4 small @ $630		2.5K		
	6 large @ $463			2.8K	1.8K
	4 small @ $630			2.5K	1.2K
MISCELLANEOUS			10K	50K	

TABLE II

ADDITIONAL TEN-MULTIPLIER MOTHER BOARDS

TO OBTAIN 256 FREQUENCY CHANNELS AT 2.5 MHz BANDWIDTH

Unit			Increase in Cost
DELAY SYSTEM:	More fan-out		2K
WIRING MATRIX:	Additional cables	405 @ $35	14.2K
MULTIPLIER SYSTEM:	Multiplier Cards	270 @ $328	88.65K
	Mother Boards	10 @ $550	5.5K
INTEGRATION LOGIC:	HSI	50 @ $350	17.5K
	Storage & Cont.		2K
SYSTEM POWER:	30% increase		7.0K
RACKS:	2 large @ $463		1.0K
SYSTEM CONT.	Additional 10 sec storage		10K
			147.85K

TABLE III

DEVELOPMENT OF NEW DELAY CARD

Board Layout	$2,500
Design Man Hours	160 hours
Mother Board Layout	$3,500
System Design Man Hours	160 hours

RE-DESIGN OF INTEGRATION LOGIC

Man Hours	320 hours

RE-DESIGN OF SYSTEM CONTROLLER

Man Hours	4,000 hours

PROTOTYPING AND TEST FIXTURES

Cost	$10,000
Design Time	200 hours

SYSTEM DESIGN

Man Hours	1,000 hours

V. TEN-ANTENNA INTERMEDIATE IMPLEMENTATION

The combined system as defined will expand, with antennas, just as the present delay/multiplier system expands. Both delay line and multiplier card requirements progress linearly with antennas. Thus for ten antennas approximately 40% of the samplers, delay cards, multiplier cards, cables, and power supplies (which account for about 80% of the total system cost) need to be implemented. If the option of multiplying frequency channels by four by using the thirteen-antenna interconnection, then 75% of the system must be implemented at the ten-antenna stage.