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PHASE LOCK LOOP PARAMETERS OF F2 AND F3 MODULES

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F2 and F3 are the modules that produce the first local oscillator signals for L-, U- and K-bands. F2 is the Upconverter Pump, and it contains a 3·2 GHz varactor-tuned oscillator that provides pump power for the L-band upconverters. F3 is the 17-20 GHz Local Oscillator that provides a conversion signal for the U- and K-band mixers. This oscillator is YIG-tuned and can be locked at intervals of 100 and 200 MHz to give the required coarse tuning for the two highest frequency bands. Each module incorporates a high-gain, second order, phase lock loop with an IF of 100 or 200 MHz. The modules also contain bias circuits for the upconverters and mixers.

During 1978 the enclosure for the phase detector was redesigned to eliminate leakage of harmonics of the reference signal, and at the same time the parameters of the phase lock loops were optimized. This memorandum describes the derivation of the revised loop parameters. Frequent reference will be made to Phaselock Techniques by F. M. Gardner, published by John Wiley and Sons, 1966, and also to Phase Lock Loops by A. Blanchard, John Wiley and Sons, 1976.

1.0 CHOICE OF NATURAL FREQUENCY OF THE LOOPS

The present application of phase lock loops calls for a high natural frequency. A high natural frequency maximizes the ability of the loop to follow phase variations in the reference frequency (see Gardner, p. 11, Figure 2-4). It also minimizes the result of frequency

modulation on the oscillator and allows a fast sweep to be used for lock acquisition. Too high a natural frequency makes the loop difficult to design and may result in instability. The precise value of the natural frequency is not highly critical, and a nominal value of 100 kHz is chosen for F2 and F3. Note that there are situations where a low natural frequency is required, for example where the loop is used as a cleanup filter for a noisy reference signal.

It is useful to calculate the effect of expected frequency modulation on the oscillators with the 100 kHz loop natural frequency. Frequency modulation resulting from power supply ripple, vibration, etc. is reduced to phase modulation by the integrating action of the loop. Consider the effect of a ripple of 0·1% at 120 Hz on the 15 V power supply. The oscillator in the F2, which has a pushing specification of 35 MHz/V, would exhibit a peak frequency deviation of 0·53 MHz when the loop is unlocked. The resulting phase modulation on the locked oscillator can be found from equations (4-12) and (4-15) on p. 31 of Gardner which, for the case of $\omega_m << \omega_n$, reduce to

$$\theta_e = \Delta\omega \cdot \omega_m/\omega_n^2 \qquad (1)$$

where θ_e = peak phase deviation, $\Delta\omega$ = peak frequency deviation of the unlocked oscillator, ω_m = modulation frequency and ω_n = loop natural frequency. For the F2, $\Delta\omega = 2\pi \times 5{\cdot}3 \times 10^5$ rad s^{-1}, $\omega_m = 2\pi \times 120$ rad s^{-1}, and $\omega_n = 2\pi \times 10^5$ rad s^{-1}, which results in $\theta_e = 0{\cdot}36^{\circ}$. In the F3, the maximum effect of the power supply ripple on the YIG-tuned oscillator would be to produce an equivalent fractional frequency deviation, i.e., 20 MHz at the 20 GHz center frequency. Thus $\Delta\omega = 2\pi \times 2 \times 10^7$ rad s^{-1} and with the same values of ω_m and ω_n used above, $\theta_e = 14^{\circ}$.

The phase modulation causes an equivalent varying error in the fringe visibility at the correlator outputs. This error is greatly reduced by the averaging circuitry which follows the correlators. There is, of course, a reduction in correlation by a factor approximately

equal to $\cos(\theta_e/\sqrt{2})$, which for F2 is negligibly different from unity, and for F3 is 0·985. Since the ripple is likely to remain fairly constant no serious error in visibility should result, and the loss in sensitivity is not intolerably large.

2.0 DAMPING FACTOR

Like the natural frequency, the loop damping factor, ζ, is not critically defined. The following aspects of loop performance lead to slightly different optimum values.

2.1 Transient Response

Low values (less than ~0.7) result in large overshoot, and high values (greater than ~2) in long settling times. Blanchard (pp. 82-85) shows that for a phase step response the fastest elimination of loop error occurs for $\zeta = 1$.

2.2 Noise Performance

For a given value of ω_n, the noise bandwidth is minimized with ζ = 0·5 (Gardner, p. 20, Figure 3-1). The noise bandwidth increases rapidly with decreasing ζ for values less than 0·25. Optimum filtering as defined by Weiner is, under certain conditions, obtained with $\zeta = 1/\sqrt{2}$ = 0·707. Gardner (p. 15) states that this is a commonly used value.

2.3 Lock Acquisitions with Linear Frequency Sweep

Gardner (pp. 47-48, Figure 4-11) indicates that acquisition probability increases with ζ, but can only state that the optimum value almost certainly lies between 0·5 and 2. Frazier and Page (IRE Trans. Space Electron. Telemetry, SET-8, 210, 1962), on whose work Gardner's comments are in part based, state that in the presence of noise the optimum damping factor lies in the range 0·5 to 0·85.

For the F2 and F3 the signal-to-noise ratio is high, and the transient response is not particularly critical since there are no deliberately induced phase or frequency steps. It is concluded that a range of about 0·7 to 1·5 for ζ should be a satisfactory choice.[1]

3.0 K_o, K_d AND DETERMINATION OF LOOP TIME CONSTANTS

The characteristic time constants of the loop integrator circuit, τ_1 and τ_2, are determined by resistors R_1 and R_2 and capacitor C in Figure 1. These are chosen to give the desired values of natural frequency and damping for the particular phase detector gain factor, K_d, and oscillator gain factor K_o. Values for each of these two factors must be assumed to vary by factors of 2 to 4 under realistic operating conditions, so the loop must be designed to keep the natural frequency and damping within acceptable ranges.

The phase detector gain factor is most easily measured by observing the peak-to-peak amplitude, V_{pp}, of the beats at the phase detector output when the loop is unlocked. Then $K_d = V_{pp}/2$ volts per radian. K_d is, of course, a function of the IF and reference signal levels, and should be measured under the appropriate operating conditions. Both F2 and F3 use the same phase detector circuit which is shown in Figure 2. Typical behavior of the gain constant is shown in Figure 3 for both 100 and 200 MHz.

The main cause of variation in K_d is variation of the IF level into the phase detector. The IF amplifiers have no a.l.c. applied and do not limit significantly since the 1 dB compression point occurs for output levels of >13 dBm for the F2 and >6.5 dBm for the F3. For F2, measurements show a typical range of K_d of 0·12 to 0·3 V rad^{-1}, the lower values resulting from reducing the 3·0 GHz and 200 MHz reference signals to the module to examine the range over which reliable locking would occur. The range of K_d and corresponding design parameters are given in Table 1. For F3 a range of values of 0·065 to 0·25 V rad^{-1}

[1] Observations of lock reliability during bench testing indicate deterioration of performance for low values of 5, so range is chosen towards the high side of optimum.

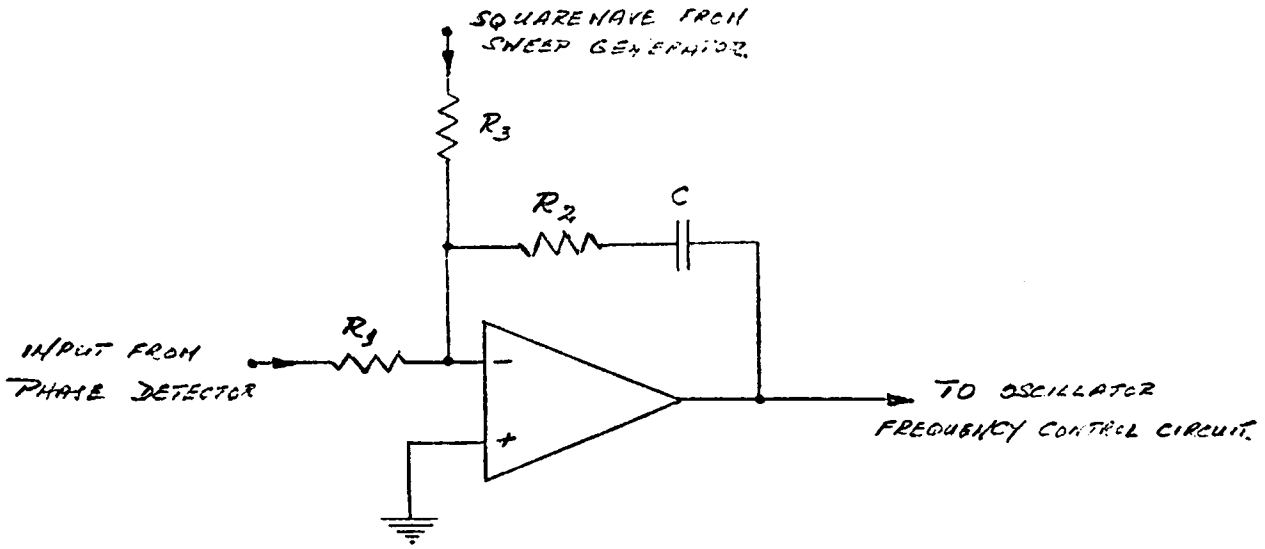

FIGURE 1: Loop amplifier circuit

Parameter	F2 Module			F3 Module			
	Min.	Nominal	Max.	Min.	Nominal	Max.	
Natural Frequency, $f_n = 2\pi\omega_n$	72	109	151	68	128	195	kHz
Loop Damping, ζ	0.68	1.03	1.42	0.61	1.17	1.78	
Phase Detector Gain, K_d	0.12	0.2	0.3	0.06	0.15	0.25	V rad^{-1}
Oscillator Gain, K_o	5.5	7.5	9.5	19	28	38	MHz V^{-1}
$K_o \times K_d$	$4{\cdot}1\times10^{6}$	$9{\cdot}4\times10^{6}$	1.8×10^{7}	$7{\cdot}2\times10^{6}$	$2{\cdot}6\times10^{7}$	$6{\cdot}0\times10^{7}$	s
$\tau_1 = R_1C$		$2{\cdot}0\times10^{-5}$			$4{\cdot}0\times10^{-5}$		s
$\tau_2 = R_2C$		$3{\cdot}0\times10^{-6}$			$2{\cdot}9\times10^{-6}$		s
Noise Bandwidth, B_L	237	436	757	218	556	1180	kHz

TABLE 1: LOOP PARAMETERS

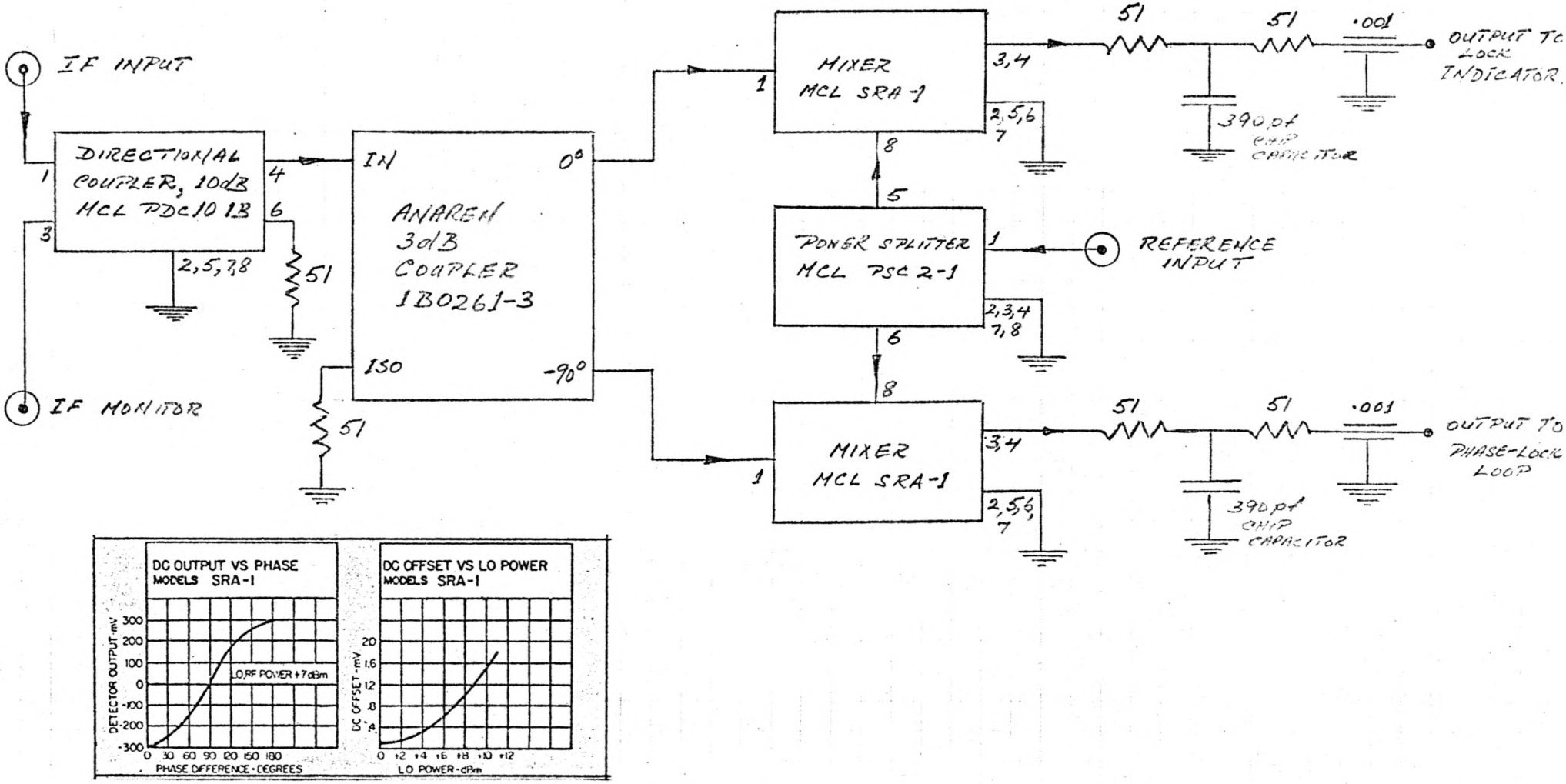

FIGURE 2: Phase detector for F2 and F3.
IF and reference frequencies are 100 or 200 MHz.
Input levels at mixer units are 3·5 dB below input to phase detector unit for reference and 4 dB below for IF. Nominal reference input to phase detector

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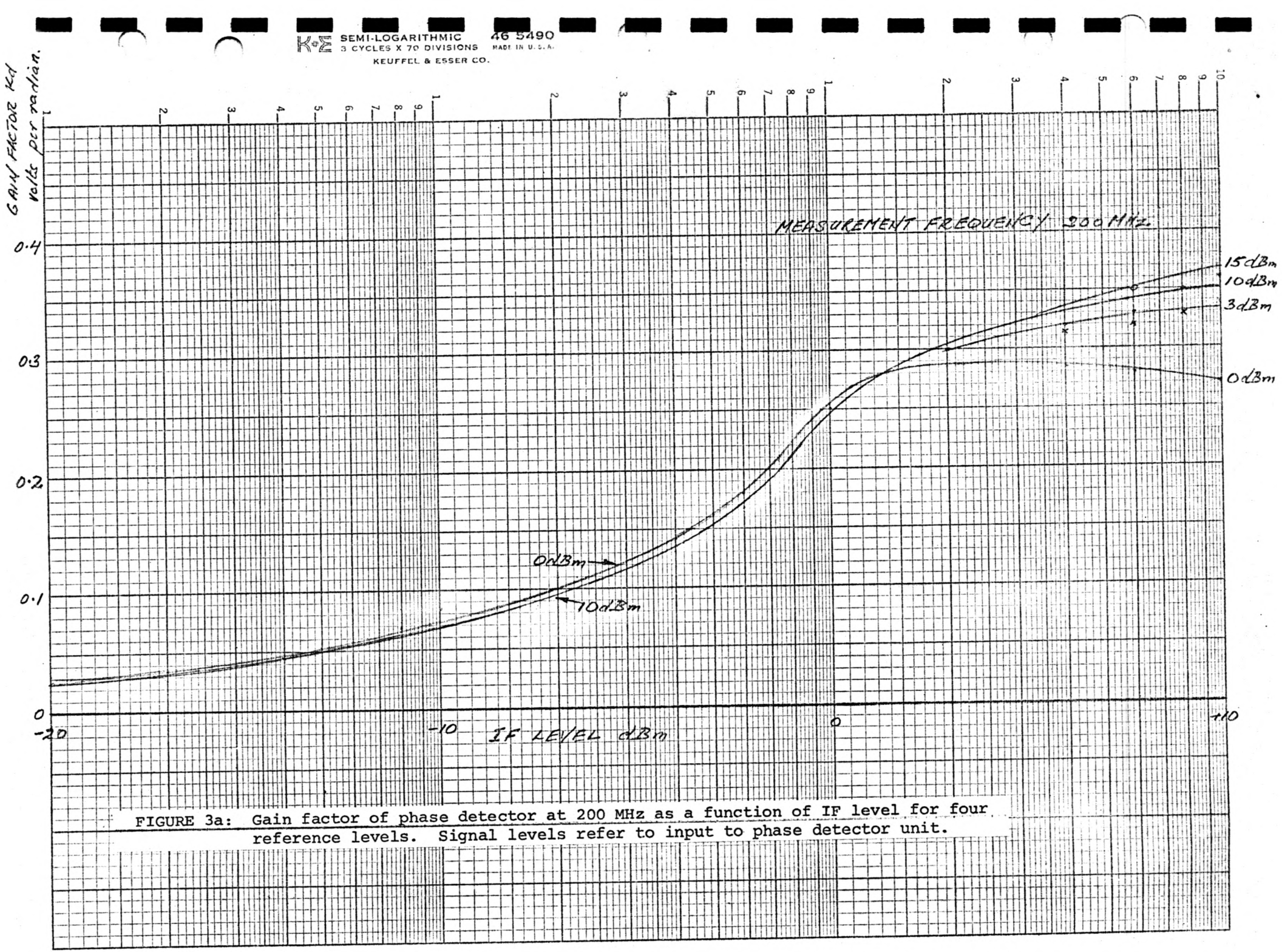

FIGURE 3a: Gain factor of phase detector at 200 MHz as a function of IF level for four reference levels. Signal levels refer to input to phase detector unit.

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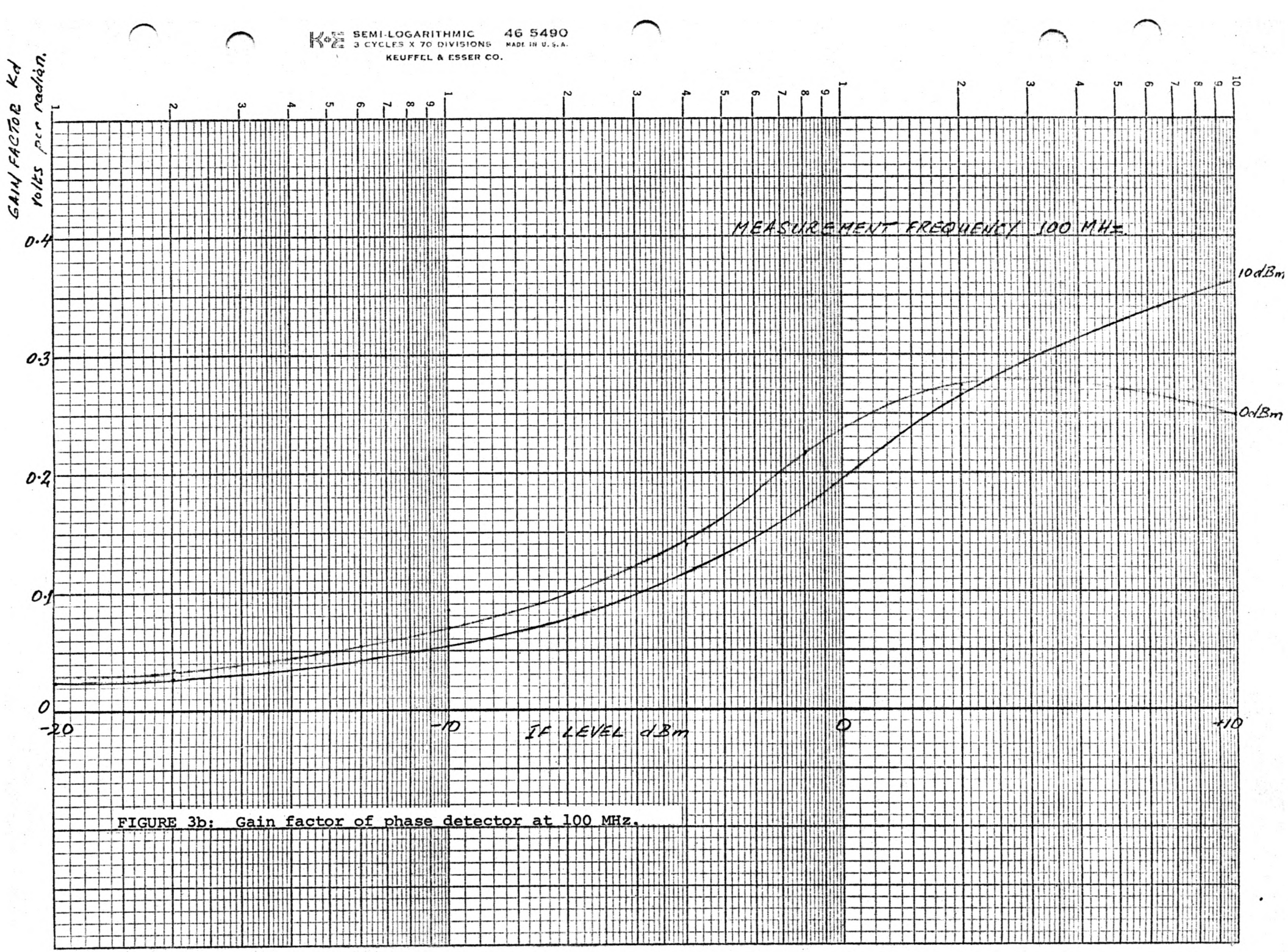

FIGURE 3b: Gain factor of phase detector at 100 MHz.

was measured between the various lock points while keeping the input signals to the module at their nominal values. The oscillator tunes over a frequency range of 3 GHz, and the variation in IF level results from the combined frequency response of the oscillator, a coupler and a harmonic mixer. The design range of 0·06 to 0·25 V rad^{-1} in Table 1 should compensate for 12 dB variation in IF level, and a further 6 dB of IF variation can be tolerated if K_o is close to the nominal value.

For the oscillators, a range of values of K_o is allowed to cover manufacturing tolerances. For the F2 the tuning sensitivity is specified as 7·5±2 MHz V^{-1} (VLA Specification A13150N1). For the YIG-tuned oscillator in F3 the f.m. coil sensitivity is specified as 120±40 kHz per m.a. (VLA Specificiation A13160N1) and the total resistance in the f.m. coil circuit is 4·25 ohms. Allowance for the variation of K_o in the design should enable oscillators to be replaced without circuit adjustments.

The required expressions for determination of τ_1 and τ_2 for a second order loop are given by Gardner (p. 9):

$$\omega_n = [K_o K_d/\tau_1]^{\frac{1}{2}} \qquad (2)$$

$$\zeta = \frac{\tau_2}{2} [K_o K_d/\tau_1]^{\frac{1}{2}} \qquad (3)$$

The chosen values for τ_1 and τ_2 and the corresponding ranges of ω_n and ζ are given in Table 1. Note that the power of ½ in the above expressions allows the fractional variation in K_o and K_d to be much larger than the tolerable range of ω_n and ζ.

4.0 IF SIGNAL-TO-NOISE RATIO

Phase fluctuations in the output resulting from noise in the loop are determined by the signal-to-noise ratio in the IF amplifier preceding the phase detector, and the noise bandwidth of the loop. The noise bandwidth, B_L is given by Gardner (p. 20):

$$B_L = \frac{\omega_n}{2}\left[\zeta + \frac{1}{4\zeta}\right] \qquad (4)$$

where B_L is in Hz and ω_n in rad s^{-1}. Values of B_L are given in Table 1. The mean square phase fluctuations on the locked oscillator are given by (Gardner, p. 21)

$$\overline{\theta}^2_{no} = W_i B_L / P_s \quad \text{(radians)} \qquad (5)$$

where W_i is the power spectral density of the noise in the IF amplifier and P_s is the signal power at the same point. To keep $\overline{\theta}_{no}$ at a tolerably low level[1], which we will take as 1^o, requires P_s to be greater by 35 dB than $W_i B_L$ which is the IF noise power in bandwidth B_L. This can easily be checked with a spectrum analyzer, using the maximum values of B_L in Table 1.

5.0 CHOICE OF INTEGRATING AMPLIFIER

The operational amplifier in the integrator circuit in Figure 1 must have sufficient gain up to the natural frequency of the loop to work effectively as an integrator. This calls for a gain of 40 dB or more at the natural frequency. In addition the DC gain must be sufficiently large to produce a negligible phase error for the largest correction voltage applied to the oscillator. If g_o is the DC gain and V_m the maximum correction voltage, the input voltage to maintain this output is V_m/g_o. The input voltage is produced by the phase detector, and corresponds to a phase difference of $V_m(g_o K_d)^{-1}$ radians. This phase error should not be greater than 10% of the 1^o per GHz phase stability goal, i.e., no greater than $0{\cdot}14^o$ for the F2 and 2^o for the F3. For the F2, V_m = 15 V and the minimum required value of g_o is $5{\cdot}1 \times 10^4$ (94 dB). For the F3, V_m = 4 V and the minimum required value of g_o is $1{\cdot}9 \times 10^3$ (66 dB). The amplifier chosen, LM318, has typical open loop gain of 110 dB for DC, and 50 dB at 200 kHz. It therefore satisfies the above requirements with ample margin.

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[1] In considering the tolerable level the same arguments used for the effect of ripple in Section 1.0 apply except that the noise-induced variations are faster and should average out more effectively.

6.0 LOCK ACQUISITION AND SWEEP RATE

The lock-in frequency is specified as the maximum frequency deviation of the oscillator for which lock will be acquired almost instantaneously when the loop is closed. Note that this is different from the pull-in frequency as defined by Gardner which applies to a wider deviation from which the loop will gradually move towards the lock condition. The lock-in frequency is roughly equal to the natural frequency of the loop and is given by Gardner (p. 43);

$$\Delta\omega_L \simeq 2\zeta\,\omega_n \tag{6}$$

Note that a necessary condition for lock-in, that a signal exists within the IF amplifier, is taken care of by the requirement that the IF amplifier bandwidth be several times the loop natural frequency.

Because the lock-in frequency is small compared with the likely open-loop frequency deviation of the oscillator, a sweep must be applied to ensure that the oscillator is brought into lock. The sweep rate must not be so great that the frequency moves through the lock-in range in a time shorter than the reaction time of the loop which can be assumed to be $\simeq \frac{2\pi}{\omega_n}$. This condition is expressed by Gardner (p. 36) as

$$\Delta\dot{\omega} < \omega_n^2$$

$\Delta\dot{\omega}$ being the sweep rate.

The sweep is implemented by applying a squarewave of amplitude ±2 V through resistor R3 in Figure 1 to the summing junction of the amplifier. The sweep rate at the amplifier output is then V_s/CR_3 V s^{-1} where V_s is the squarewave amplitude, ±2 V. The corresponding sweep rate of the oscillator is $K_o V_s/CR_3$. The condition that this be less than ω_n^2 becomes, using equation (2),

$$\frac{K_o V_s}{CR_3} < \frac{K_o K_d}{CR_1},$$

$$V_s/R_3 < K_d/R_1 \qquad (7)$$

Gardner (p. 47, Figure 4-10) presents evidence that for $\zeta = 0{\cdot}707$ a factor of at least 2 should be allowed in fulfilling the above inequality.

When lock is acquired the current from the lock detector should be able to hold the oscillator frequency constant to allow the lock indicator circuit to function and turn off the sweep. This requires that the current from the phase detector flowing through R_1 to the summing junction of the integrator should be able to exceed and cancel the sweep current flowing through R_3. The maximum output voltage from the phase detector is $(\pm)K_d$, and, not too surprisingly, the required condition turns out to be identical to (7) above.

In an early version of F2 and F3 a partially differentiated squarewave was injected through R_3 which resulted in a nonlinear sweep. This is clearly undesirable since it is difficult to fulfill the various conditions described above if the sweep rate is not constant, and the probability of acquiring lock is dependent upon the frequency offset to be corrected.

7.0 CHOICE OF RESISTANCE AND CAPACITANCE VALUES IN THE INTEGRATOR CIRCUIT

In choosing R_1, R_2, R_3 and C in Figure 1 the following conditions must be fulfilled:

1) $R_1C = \tau_1$, $R_2C = \tau_2$ (τ_1 and τ_2 given in Table 1)
2) $K_d/R_1 > 2\ V_s/R_3$
3) R_1 should be about 1 kilohm or more so as not to overload the phase detector.

Values meeting the above requirements are given in Table 2 for the two modules.

	F2 Module	F3 Module
τ_1	$2{\cdot}0\times10^{-5}$ s	$4{\cdot}0\times10^{-5}$ s
τ_2	$3{\cdot}0\times10^{-6}$ s	$2{\cdot}9\times10^{-6}$ s
C	0·002 μf	0.022 μf
R_1	10 kΩ	1.8 kΩ
R_2	1·5 kΩ	130 Ω
R_3	300 kΩ	360 kΩ
Sweep Ramp, V_s/CR_3	$3{\cdot}33\times10^{3}$ Vs^{-1}	253 Vs^{-1}
Sweep Squarewave Period	18 ms	37 ms
V_s/R_3	$6{\cdot}67\times10^{-6}$ A	$5{\cdot}6\times10^{-6}$ A
Min. K_d/R_1	$1{\cdot}2\times10^{-5}$ A	$3{\cdot}3\times10^{-5}$ A

TABLE 2: CIRCUIT VALUES

8.0 SWEEP RANGE

The voltage range through which the integrating amplifier sweeps should be sufficient to drive the oscillator over the desired frequency search range. In the F2, the voltage sweeps between -11 and +11 V causing the oscillator to sweep over 165 MHz. This range is a factor of two larger than necessary, but it is convenient to let the output voltage limits of the LM318 amplifier define the sweep range. In the F3, the voltage sweep is 0 to 4 V, and the corresponding frequency sweep at 112 MHz.

Finally, the period of the squarewave oscillator must be sufficient to allow the full sweep in one direction to occur during half a cycle. For the F2 the squarewave period is 18 ms and for the F3, 37 ms.

9.0 PHASE DETECTOR OFFSET

Imbalance in the diodes in the SRA-1 mixer units in the phase detector leads to a DC output generated by the reference input which is independent of the IF signal. According to the manufacturer's specifications for the SRA-1, the typical offset is 1 mV with 7 dBm input power. In one unit, however, offset voltages between 20 and 30 mV were measured. In this case the mixer units had been unsoldered from an early version circuit board and were probably damaged by the heat required. The excessive offset was sufficient to prevent the sweep from operating in an F3 module.

The effect of a steady offset can be cancelled by adjustment of the loop amplifier offset potentiometer. To make this adjustment the reference signal should be applied to the phase detector but no IF signal should be present, and the sweep should be disabled by removing the squarewave generator IC. The offset potentiometer should then be adjusted to be as close as possible to the point where the integrator output swings from one polarity to the other. An exact compensation for the offset voltage cannot, of course, be maintained with the 11±1·5 dB specification on input reference level to the modules. The maximum tolerable uncompensated voltage is $V_S R_1/R_3$ which results in a

current sufficient to overcome the sweep current. This voltage is 65 mV in the F2 and 10 mV in the F3.

Before retrofitting the new shielded phase detectors in the F2 and F3 modules, they should each be checked for offset voltage. A 200 MHz signal applied to the reference input should produce offsets of no more than 5 mV at the phase detector and lock indicator outputs for input power levels of 0, 10, and 15 dBm. The test should be repeated with the signal applied to the IF input. Tests on a few units have shown that the offsets do not vary greatly between 100 and 200 MHz.

10.0 LOCK INDICATOR THRESHOLD

The lock indicator functions by detecting the output voltage from second output of the phase detector unit. This output is produced by a mixer for which the IF signal is in phase quadrature to that going to the mixer producing the output to the loop amplifier. The two outputs have equal gain factors, K_d, and when the loop is in the normal lock condition the voltage to the lock indicator circuit is $\pm K_d$.

Detection of the in-lock condition is most critical at the instant that the loop locks and is holding the oscillator frequency against the action of the sweep voltage. The loop output of the phase detector unit is then equal to $V_s R_1/R_3$, and the corresponding phase error is $\sin^{-1}(V_s R_1/K_d R_3)$. The output to the lock indicator is $\pm K_d$ times the cosine of the phase error, i.e., $\pm K_d\sqrt{1-(V_s R_1/K_d R_3)^2}$. The lock indicator threshold should be set to respond to this voltage level, computed for the minimum value of K_d. It should not, of course, be set much lower since this would only invite problems from spurious responses and DC offsets. The lock indicator threshold is 0.1 V in the F2 and 0.05 V in the F3, and these values just fulfill the above requirement.

11.0 CONCLUDING REMARKS

The performance of the F2 with the parameters described here

appears to be satisfactory with regard to reliability of lock. The performance of the F3 is less satisfactory as a result of excessive variation of IF level with oscillator tuning, and further work on the harmonic mixer or addition of an a.l.c. loop appears to be required.

ACKNOWLEDGMENTS

S. Weinreb and G. Barrell produced the original design of the F2 and F3 modules, and some further work has been added by H. Richards. L. R. D'Addario contributed some useful ideas to the design review described in this memorandum.