NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO
VERY LARGE ARRAY PROGRAM

VLA ELECTRONICS MEMORANDUM NO. 182

CORRELATOR SYSTEM SELF TEST/SELF HEAL

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1.0 SCOPE

This memorandum will describe the self test/self heal capability of the continuum/spectral line correlator system.

2.0 DELAY/MULTIPLIER TEST

Figure 1 shows the configuration of test hardware used in self testing and self healing of the correlator system. Figure 1 represents one antenna IF (A, B, C, or D) and hence is one-fourth of the total test logic in the system. Operation is as follows:

1. During data invalid of each 19.2 Hz waveguide cycle the system controller steers all delay line inputs to a pseudo-random data generator.
2. The system controller loads one of four delays into all delay lines and one of four lags to all recirculators. This insures all delay lines and recirculators are identically programmed while the other three delay/lag values test the system in subsequent test cycles over a small but comprehensive subset of delays and lags possible in actual operation.
3. The results of one 92.16 μsec integration for one-fourth of one quadrant (one array) are stored in RAM's at the 14 MHz interface rate for later analysis.
4. All delay lines and recirculators are returned to operational status for use in the next data valid cycle with real antenna delays.
5. During the next data valid period the one array's worth

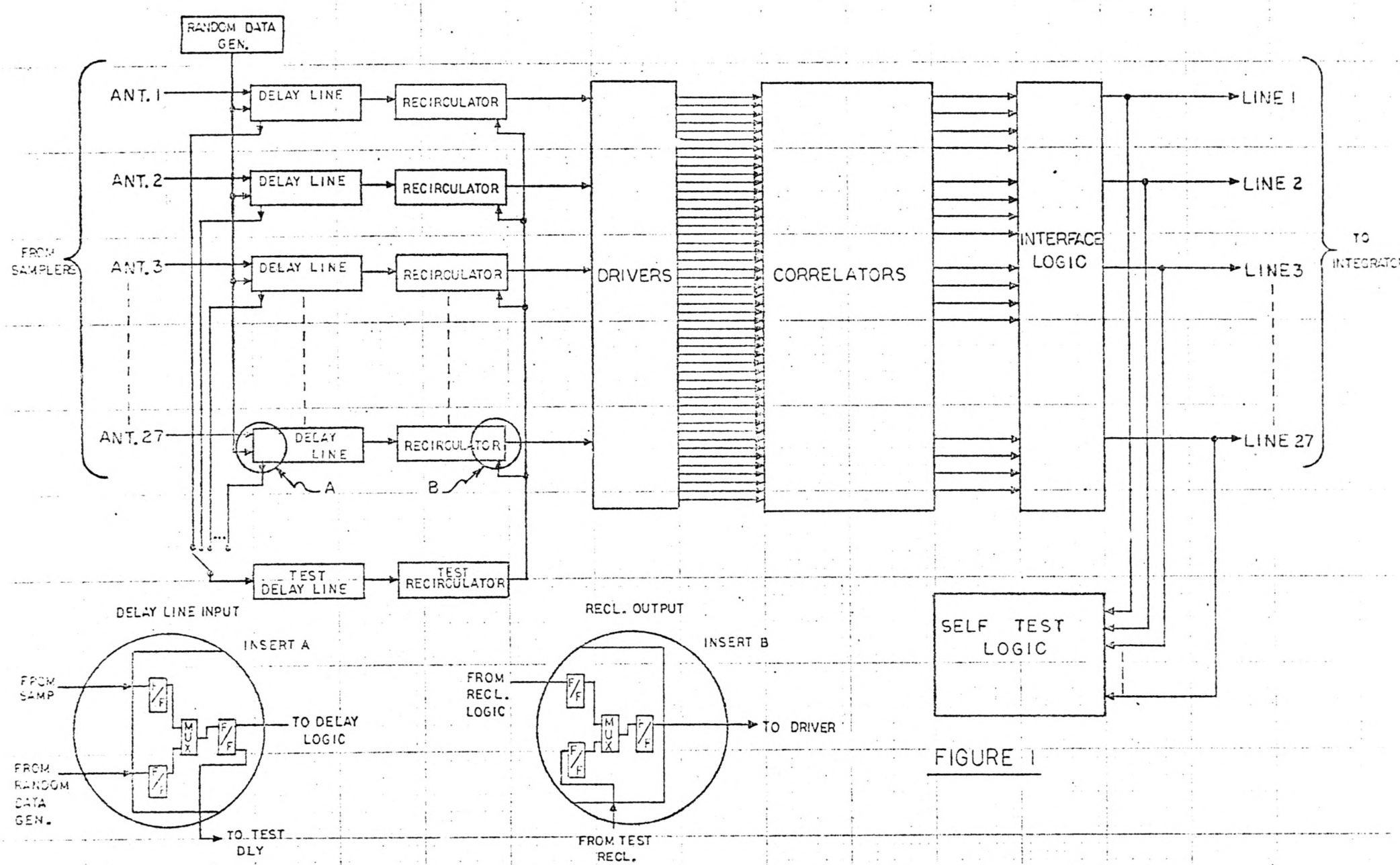
RANDOM DATA GEN.
ANT. 1
ANT. 2
ANT. 3
ANT. 27
FROM SAMPLERS
DELAY LINE
RECIRCULATOR
TEST DELAY LINE
TEST RECIRCULATOR
A
B
DRIVERS
CORRELATORS
INTERFACE LOGIC
LINE 1
LINE 2
LINE 3
LINE 27
TO INTEGRATOR
SELF TEST LOGIC
DELAY LINE INPUT
INSERT A
FROM SAMP
FROM RANDOM DATA GEN.
MUX
F/F
TO DELAY LOGIC
TO TEST DLY
RECL. OUTPUT
INSERT B
FROM RECL. LOGIC
TO DRIVER
FROM TEST RECL.

FIGURE 1

of 92.16 μsec correlator results (27 x 27 results) are transferred into the system controller.

6. Since the self test is run with whatever system configuration is being used in the observation in progress (continuum, one band line, 2 band line, 4 band line, legal mixed configurations, etc.) predicted values of each antenna pair are prepared reflecting: a) modes of two antennas for each result, b) array and quadrant being checked, c) which of 4 delay/lags used.
7. Predicted values are checked against actual results and no-go results flagged. Errors are displayed on the front panel and the Modcomp (SPECTRE) is notified.
8. After all 8 arrays of a quadrant pair (quad 1 and 2 or quad 3 and 4) have been tested (with the same delay/lag) these results are checked to see if a pattern of errors exist that would indicate a bad delay line or recirculator. Briefly this pattern would be recognized if all correlator results a given delay line or recirculator (which is bad cannot be determined) contributed to are bad.
9. If such a pattern is recognized one of several things may happen:
   a) A flag is set that will result in an exchange of the test delay/recl path for the suspected busted delay/recl path during the next data invalid period in an attempt to heal the system for the next and subsequent data valid cycles.
   b) Recognition that the test delay/recl path is not available (either since it is already used on another path or has been flagged to not exchange) will take place and no further action will be attempted (except as below).
   c) Recognition that that particular delay/recl path is

already bypassed will lead the system to assume that an early attempt to fix the same problem was unsuccessful and hence the test logic is itself bad. In this case the test path will be removed and flagged so as to attempt no future healing action.

d) The busted path may belong to an antenna that is not in use (no mode has been assigned it) in which case no action is taken so as to not waste the test path on an unused antenna.

A summary of test/heal features would be as follows:

1. The delay/recirculator/driver/correlator/interface portion of the system can, during inactive periods, test itself on a noninterfere basis requiring 16 waveguide cycles (times 4 for all four delay/lag words) for a complete test in the final four IF system.
2. Error filtering is obtained since a problem must be present for 4, 6, or 8 (depending on mode) consecutive waveguide cycles for the pattern of errors inducing a healing attempt to be recognized.
3. A busted path within the delay/recl subsystem can be healed using alternate test paths.
4. The effectiveness of such an attempt at healing can be observed in subsequent operation and abandoned if ineffective.
5. All errors encountered and subsequent actions taken are reported to SPECTRE. Appendix 1 gives the form of error reporting.
6. SPECTRE can modify at will any action taken by the system controller on its own. Appendix II gives the command format for such control.
7. If a delay line or recirculator card is changed (either while substituted for by the test path or otherwise) the test logic will quickly see this busted path and disqualify

itself from further healing attempts. Pressing the front panel reset switch will clear errors and again allow exchange of test logic for suspected busted cards. If the recirculator card is changed, the program word stored on that card will be lost and the observation must be restarted.

8. Substitution, and disabling substitution, occur on an IF basis, each of the four IF circuits acting independently.

Since a path through the test delay/recirculator must be via cables not needed in normal paths, extra delay to signals in this path must be compensated for by the test delay line. In continuum an extra 10 bits of delay are encountered and the system controller will load delays to this delay line that are 10 bits less than that to which BOSS specifies for the normal delay line it is paralleling. Thus a requirement for using the test path is that BOSS supply no delays less than 10 to any delay line in continuum. For spectral line a more complicated requirement exists where the minimum delay is (5N + 5) where the sample rate is 100/N MHz.

3.0 INTEGRATOR TEST

Figure 2 shows the configuration of test hardware used in self testing and self healing of the integrator system. This figure represents one quadrant and hence is one-fourth of the total test logic in the system. Operation is as follows:

1. The test memory path parallels one normal memory path each dump period (0.3 to 10 seconds). When the array processor reads information from the paralleled memory its contents are compared with that of the test memory and an error is flagged if noncomparison occurs.
2. Normally the test memory circulates around a loop of all used lines requiring KD seconds for a complete loop where K represents the number of antennas being observed with and D the dump period.

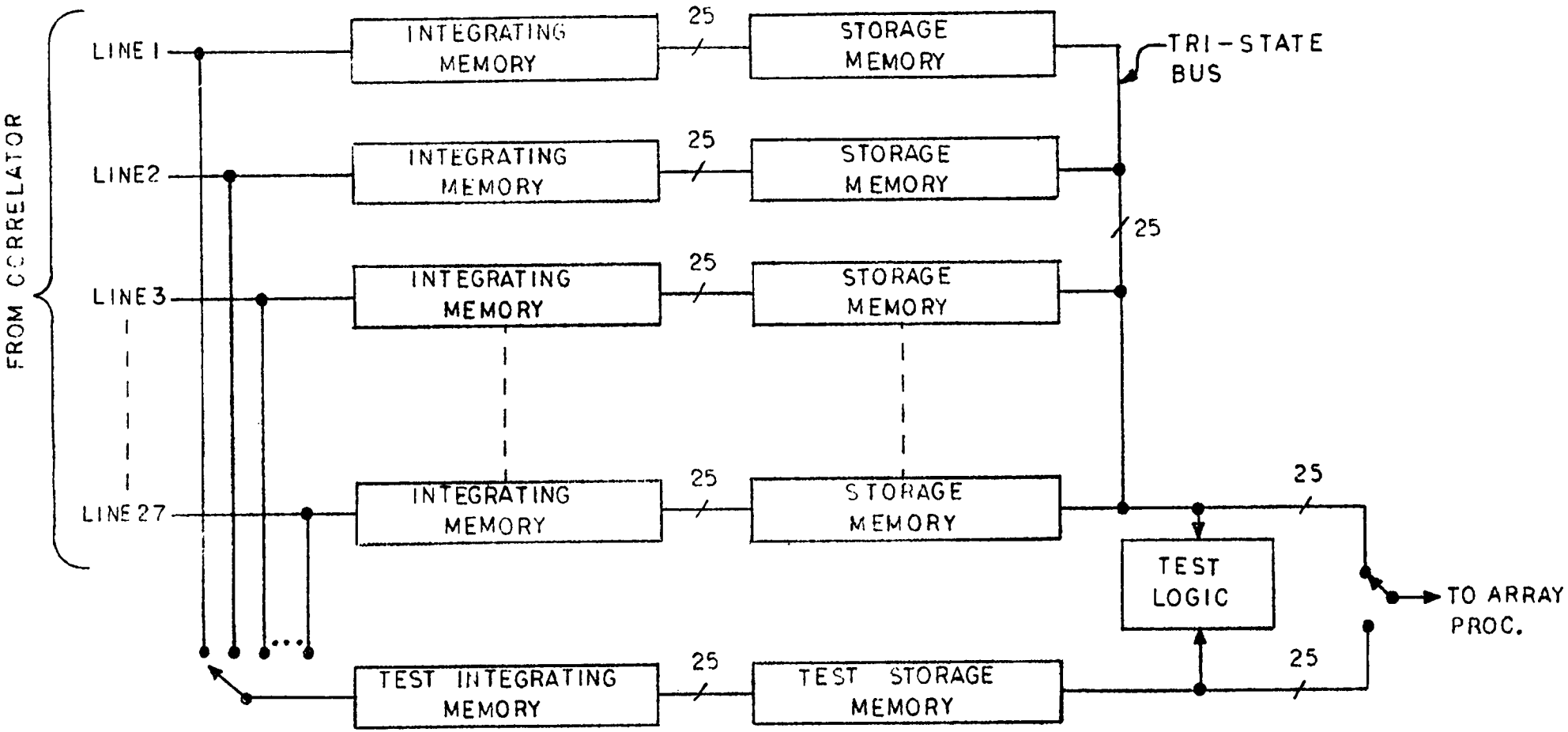
FROM CORRELATOR
LINE 1
LINE 2
LINE 3
LINE 27
INTEGRATING MEMORY
INTEGRATING MEMORY
INTEGRATING MEMORY
INTEGRATING MEMORY
TEST INTEGRATING MEMORY
25
STORAGE MEMORY
STORAGE MEMORY
STORAGE MEMORY
STORAGE MEMORY
TEST STORAGE MEMORY
TRI-STATE BUS
TEST LOGIC
TO ARRAY PROC.

FIGURE 2

3. If an error is detected the test memory advances once more and awaits the result of this test. A second consecutive error causes the logic to assume the test memory is itself bad and a flag is set to prevent any future substitution with the test memory. If no error is found the test memory backs up one place and substitutes for the suspected busted path.
4. No logic exists allowing evaluation of the effectiveness of the healing attempt by looking at data sent to CORA, however, the test memory can still check the suspected busted memory and it continues to do so even after it has substituted for that memory. If 16 consecutive dump times (at any period while substitution exists) are observed with no errors unsubstitution occurs and the test memory resumes its normal circuit in test mode.

Again in summary the test/heal features are:

1. Using observational data and conditions, not artificial data and conditions as in the correlator self test, the integrator system can test and heal itself on a noninterfere basis requiring KD seconds (see above) for a complete test.
2. Error filtering is obtained in that even after an exchange of test logic for suspected busted normal logic has taken place unexchange occurs unless continued malfunctioning is observed.
3. Some testing of the test logic occurs in that 2 consecutive errors in different lines causes the test system to disqualify itself for future healing attempts.
4. All error indications and healing actions are displayed on the front panel and reported to SPECTRE (see Appendix 1).
5. SPECTRE can modify at will any action taken by the system controller on its own (see Appendix 2).
6. Operation is on a quadrant basis with the four sets of test hardware acting independently of each other.

F=6 DATA REQUEST

A A A A A A A A 0 1 1 0 D D D D

ASCII CH. (EXCEPT FOR ERROR READOUT)

	ASCII	A A A A A A A A	DATA VECTORED TO READ	# WORDS
(1)	ERROR READOUT	1 0 0 0 0 0 0 0	RESET CRT ERROR FLAG	—
	ERRIR READOUT	0 0 0 0 0 0 0 0	ERROR BUFFER	3
	A	0 1 0 0 0 0 0 1	DELAYS: LS BITS OF DELAY	5
	B	0 0 0 1 0	DELAYS: MS BITS OF DELAY	5
	C	0 0 0 1 1	DELAYS: MODE OF DELAY	5
	D	0 0 1 0 0	DUTY CYCLES	1
(1)	E	0 0 1 0 1	ERROR BUFFER (CRT ONLY)	3
(2)	F	0 0 1 1 0	FRONT PANEL ERRORS	5
	G	0 0 1 1 1		
	H	0 1 0 0 0		
	I	0 1 0 0 1	INTEGRATOR MODES	
	J	0 1 0 1 0		
	K	0 1 0 1 1		
	L	0 1 1 0 0		
	M	0 1 1 0 1	MODES	2 7
	N	0 1 1 1 0	SAMP. FACTOR, MAX LAG, LAG STEP	1 6
	O	0 1 1 1 1		
	P	1 0 0 0 0	SAMP DELAY	5 4
	Q	1 0 0 0 1		
	R	1 0 0 1 0		
	S	1 0 0 1 1	SIN X COS, 50MS V_s	1 6
	T	1 0 1 0 0	TEST STATUS	3
	U	1 0 1 0 1	INTG. TEST STATUS	4
	V	1 0 1 1 0	V_s	1 6
(1)	W	1 0 1 1 1	ARRAY STORAGE #1	2 5 5
(1)	X	1 1 0 0 0	ARRAY STORAGE #2	2 5 5
(1)	Y	1 1 0 0 1	ARRAY STORAGE #3	2 5 5
(1)	Z	1 1 0 1 0	ARRAY STORAGE #4	2 5 5

NOTES:
(1) CRT ONLY
(2) [illegible]

(OVER)

F=6 CON'T

ERROR BUFFER READOUT

0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0

YIELDS 32 RESPONSES, 16 PAIRS OF ERROR MESSAGES CONSISTING OF:

WORD A → ERROR TYPE
WORD B → ERROR DATA

ERROR TYPE	WORD A	WORD B
ILLEGAL COMMAND	0001	ACTUAL COMMAND
ILLEGAL COMMAND TIME	0002	ACTUAL COMMAND
BT SKIPPED	0003	BT WHEN DISCOVERED
BT EXCEEDED	0004	BT EXCEEDED
LOW DELAY VALUE	0005	I.F.
NO MODES	0006	ZERO
INTERGRATOR SELF TEST ERROR	0007	000A AAAA 0000 00QQ
REPORT INTERGRATOR EXCHANGED	0008	000A AAAA 0000 00QQ
REPORT INTERGRATOR UNEXCHANGED	0009	0000 0000 0000 00QQ
INTERGRATOR SELFTEST DISABLING	000A	0000 0000 0000 00QQ
REPORT DELAY/RECL ERRORS	000B	QQAA 00NN NNNN NNNN
REPORT DELAY/RECL EXCHANGE	000C	000A AAAA 000D 00II
REPORT D/R CANNOT EXCHANGE	000D	000A AAAA 000D 00II
DELAY/RECL SELF TEST DISABLING	000E	000A AAAA 0000 00II
ERROR BUFFER EXCEEDED	FFFF	NO. OF ERRORS PAST 15

F=C SELF TEST INSTRUCT

A A A A A I I I I I O O D D D D

A	I	D D D D	SYSTEM	FUNCTION
N/A	I.F.	0 0 0 0	DLY/MULT	ALLOW EXCHANGE
N/A	I.F.	0 0 0 1		INHIBIT EXCHANGE
N/A	I.F.	0 0 1 0		RESET EXCHANGE
ANT.	I.F.	0 0 1 1		FORCE EXCHANGE
QQAA	00 DD	0 1 0 0		MODIFY DIM SELF TEST
ANT.	I.F.	0 1 0 1		FORCE PARALLEL
—	—	0 1 1 0		DISABLE SELF TEST
—	—	0 1 1 1		ENABLE SELF TEST
N/A	QUAD	1 0 0 0	INTEGRATOR	ALLOW EXCHANGE
N/A	QUAD	1 0 0 1		INHIBIT EXCHANGE
N/A	QUAD	1 0 1 0		RESET EXCHANGE
LINE	QUAD	1 0 1 1		FORCE EXCHANGE
		1 1 0 0		
		1 1 0 1		
		1 1 1 0		
		1 1 1 1		

OUTPUT EX → ANT.

INPUT MUX → ANT.

DLY/MULT SELF TEST:
(PER I.F.)