

National Radio Astronomy Observatory

Very Large Array Program

VLA ELECTRONICS MEMORANDUM NO. 219

New Dewpoint / Ambient Temperature

Ron Weimer
November 1991

1. Background:

The dewpoint and ambient temperature for the VLA system has evolved over the years. A General Eastern system was in use first. This was replaced with an EG&G system. Both used cooled mirror hydrometers to measure dew point temperature. During the Voyager project the reliability of the EG&G system was questioned. A Technical Service Laboratory (TSL) hydrometer was purchased and installed at the VLA weather station to provide a back-up for the EG&G. The TSL model 1063 was the same unit being installed at the 10 VLBA weather stations. A TSL readout station was installed in the VLA Control room. The readings were compared to the EG&G readings and used to correct the computer value as required. The TSL readings were not interfaced into the VLA computers. Data entry was manual via terminal. The TSL unit consist of three subunits. Two are mounted on the VLA weather tower and the third, a readout system, is installed in the control room. Communication from outside units is over a twisted pair cable which carries 600 baud biphasic encoded data. Since this is in the audio frequency spectrum it can be sent over normal telephone pairs. During the summer of 1991 the EG&G system had a major failure - probably lightning induced. Paul Harden worked to repair it but found that repair parts were no longer available from the manufacturer. It was decided to use the TSL system already in place. In order to reduce the software development time it was decided to make the replacement transparent to the software. The EG&G system was input via antenna 0, data set 0, mux addresses 4, 6 and 7. Address 4 is used for ambient temperature and 6 and 7 both are used for dewpoint. For the temperature range of -45°C to +60°C the mux input voltage varies linearly from 0.0 volts to 5.0 volts.

$$I.e \quad V_{DC} = \frac{T^{\circ}C + 45}{21} \quad \text{or}$$

$$T^{\circ}C = 21 * V_{DC} - 45$$

The next section describes the implementation of the interface.

2. Implementation of the TSL interface:

Data set 0 is mounted in a cabinet at the base of the weather tower. The EG&G voltage come to a terminal strip in this cabinet. Also on another terminal strip in the cabinet was the audio encoded data from the TSL unit going to the control room. A wirewrap card was constructed, mounted in this same cabinet, and connected to data set 0 in place of the EG&G voltage. Power supplies already present in the cabinet were used to power the card. Table 1 lists the interconnections in the data set cabinet.

Table 1

TS12 - 3	Clear - TSL data Blue - to control room Blue - J101-8 TSL - VLA card
TS12 - 4	Black - TSL data Black - to control room Black - J101-12 TSL - VLA card
TS6 - 1	Blue J101-86 VTA from TSL VLA card removed wire from J11-C to this terminal
TS6 - 5	Yellow J101-90 VTD from TSL VLA card removed wire from J11-C to this terminal
TS6 - 7	Yellow jumper from TS6-5 - also VTD Removed wire from J11-F to this terminal
TS6 - 2,6,8	Jump together and run wire to J101-49 for analog ground. Removed any wire now on these terminals.
	+15v, -15v, +5v, and ground wired to unused pin on J1 - DC power connector.

The format of the TSL audio data is shown on Figure 1. This is a copy of a page out of the TSL manual. The signal is capable of driving long phone lines and multiple receivers. We merely tap in parallel with the receiver in the control room.

3. Circuit description:

The schematic of the converter card is shown in figure 2 (sheet 1 & 2). The oscillator chip 6A generates a 9600 Hz clock signal, which is 16 times the 600 Hz data rate. The exact frequency is not critical. Variation of greater than 10% should not hurt circuit operation. The output of 6A is buffered with a

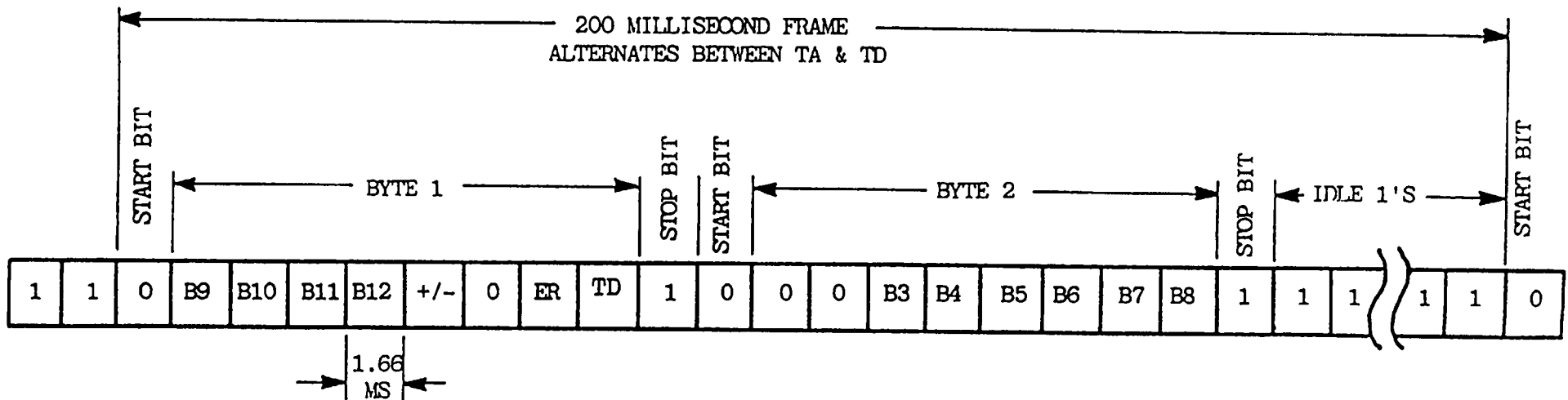
Schmitt trigger. The 555 output signal are slow enough to cause oscillation on some TTL input circuits. The audio biphase signal comes into the card on pins 8 and 12. An audio transformer isolates the logic from any noise on the audio line. The transformer output drives a transistor whose output is also buffered with a Schmitt trigger to sharpened up the waveform edges. Chip 4A and 2A generate a pulse out on every transition of the audio data. Chip 6C, 5C, 5D and associated gates recover the binary data, clock (600Hz), and a start pulse from these transitions. The start pulse detects the first zero after a long string of ones between frames. See Figure 1. Other zeros will also generate start pulse signal but they are ignored by the logic. Chip 4D, 4B and 4C start on the first zero, then count 24 clock pluses, then wait for another start signal. Data is loaded into shift register chips 3B, 3C and 1B during this cycle. After 24 clocks are counted a load pulse is generated. It loads 4 data bits into chip 6D. The output of 6D drives 4 LED's. These might be useful in trouble shooting the system in the future. If the TSL transmitter is not in an error condition the load pulse is used to generate latch pluses for the D/A converters. If there is an error condition the D/A latches hold the last good data. TDL latches dewpoint data and TAL latches ambient temperature data. The data from the TSL is in sign plus magnitude format. The D/A converter requires an offset binary count input. The exclusive or gates in chips 2A, 2B and 2C convert the sign plus magnitude code to an offset binary code. The 51.2° bit is ignored so that the D/A responds to +/- 51.1 °C. Temperatures outside that range are not converted correctly. I don't think that is a problem at the VLA site. Chips 1C and 1D latch the dewpoint data. D/A chip 1E converts the binary code to an analog voltage in the range from +5V to -5V. Two opamps in chip 5G generates an offset and scales the voltage so that it matches the EG&G values. Chips 3D, 3E and 3F convert the ambient temperature data to an EG&G compatible voltage.

4. Physical Layout:

Appendix A is a copy of the assembly information for the converter card. Appendix B is a copy of the input to the PC WIREWRAP program used to wrap the card. Two cards were built. One was in use for some months, then it was replaced with the second one and stored in the cabinet in the electronics area.

5. Acknowledgement:

Thanks to Nelson Atencio and Ernesto Navarrette for help with construction and testing the cards.

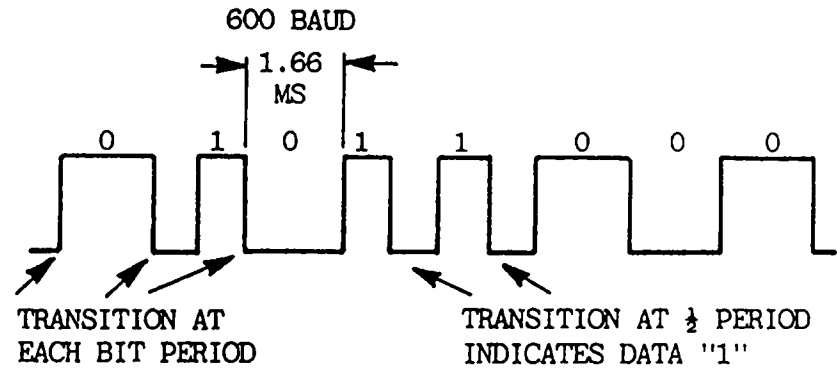


BIT WEIGHTING

B1	.025°
B2	.05°
B3	.1°
B4	.2°
B5	.4°
B6	.8°
B7	1.6°
B8	3.2°
B9	6.4°
B10	12.8°
B11	25.6°
B12	51.2°

POL. "1" = MINUS

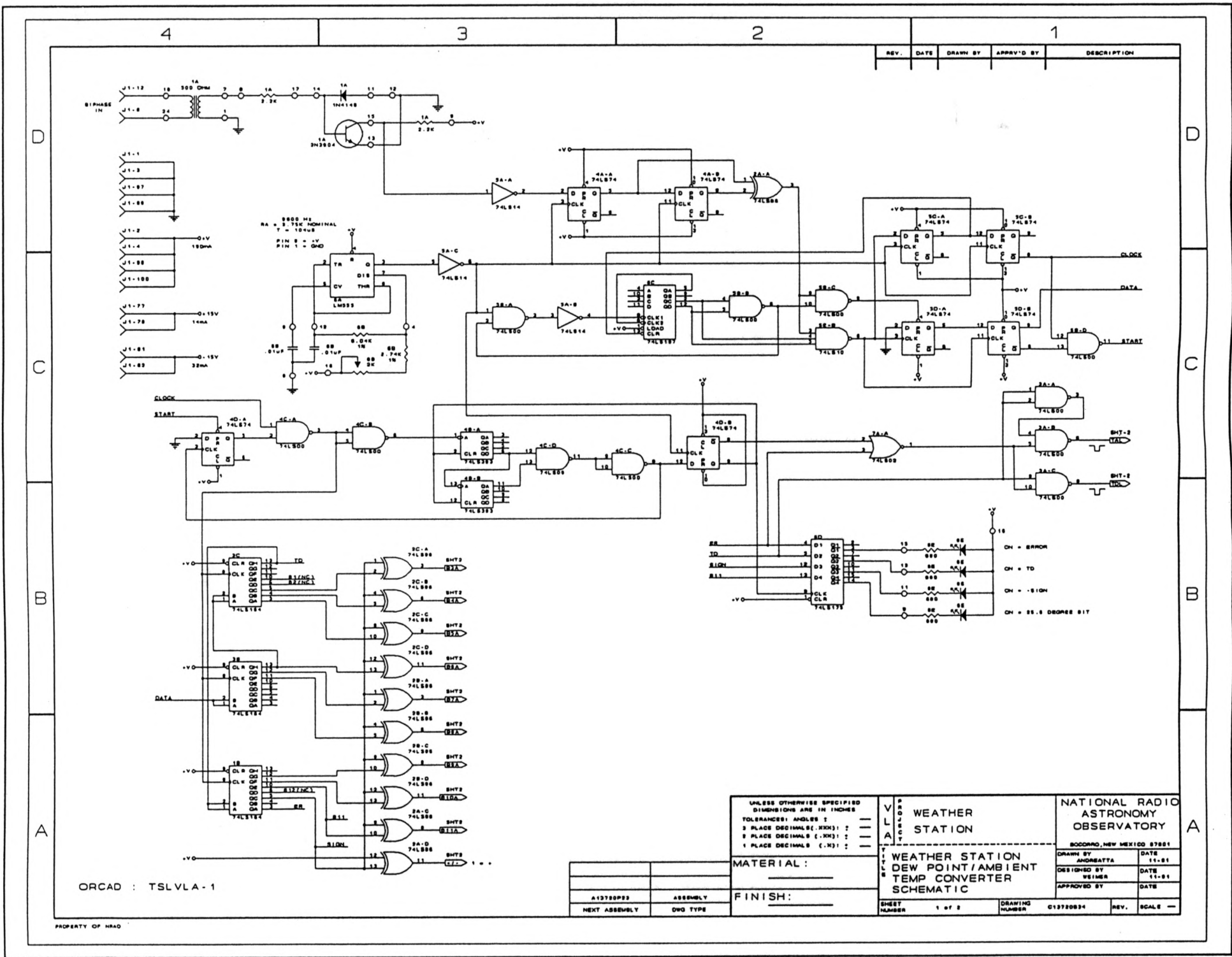
CODING IS MACHESTER (B1-PHASE)



SERIAL DATA FORMAT

Fig. 1

Fig. 2 Sheet 1 of 2



ORCAD : TSLVLA-1

PROPERTY OF NRAO

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES : ———
3 PLACE DECIMALS (.XXX) : ———
2 PLACE DECIMALS (.XX) : ———
1 PLACE DECIMALS (.X) : ———

MATERIAL :
FINISH :

WEATHER STATION
DEW POINT/AMBIENT
TEMP CONVERTER
SCHEMATIC

NATIONAL RADIO ASTRONOMY
OBSERVATORY
BOCCANO, NEW MEXICO 87601

DRAWN BY	ANDREATTI	DATE	11-81
DESIGNED BY	WEIMER	DATE	11-81
APPROVED BY		DATE	

SHEET NUMBER 1 of 2 DRAWING NUMBER C13720834 REV. SCALE —

A13720834	ASSEMBLY
NEXT ASSEMBLY	DNW TYPE

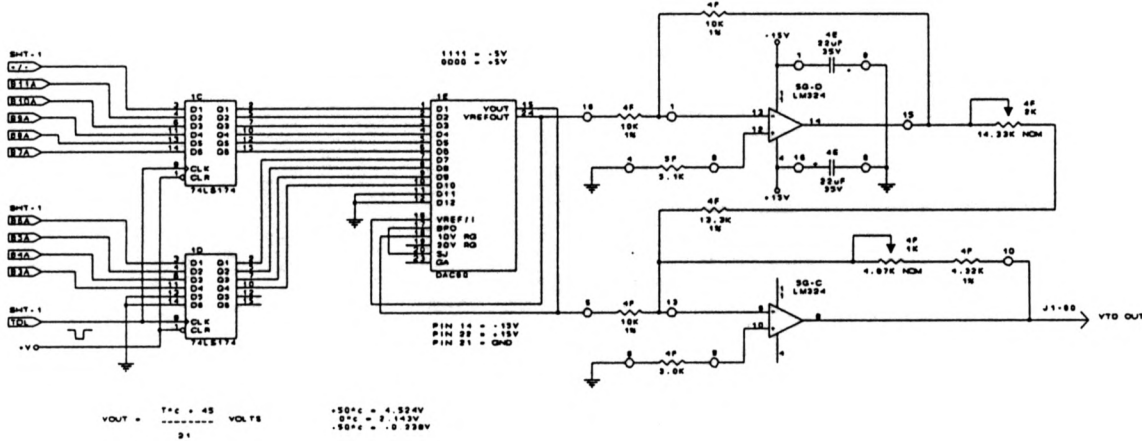
4

3

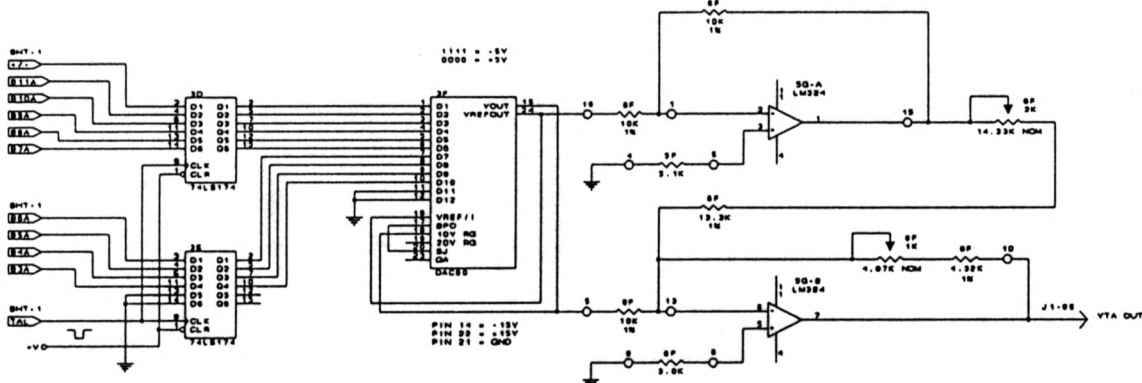
2

1

REV.	DATE	DRAWN BY	APPR'D BY	DESCRIPTION



DEW POINT
LATCH-D/A-SCALING



AMBIENT TEMP
LATCH-D/A-SCALING

ORCAD : TSLVLA-2

PROPERTY OF NRAO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES : — 3 PLACE DECIMALS (XXX) : ? 2 PLACE DECIMALS (.XX) : — 1 PLACE DECIMALS (.X) : —		V L A T S W E A T H E R S T A T I O N	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
MATERIAL : _____		WEATHER STATION DEW POINT/AMBIENT TEMP CONVERTER SCHEMATIC	DRAWN BY ANDREATTA DATE 11-81
FINISH : _____		DESIGNED BY WEINER DATE 11-81	APPROVED BY DATE
A13720P03	ASSEMBLY	SHEET NUMBER 2 OF 2	DRAWING NUMBER C13720034
NEXT ASSEMBLY	DWG TYPE	REV.	SCALE

Fig. 2 Sheet 2 of 2

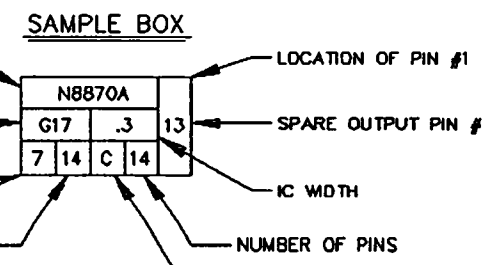
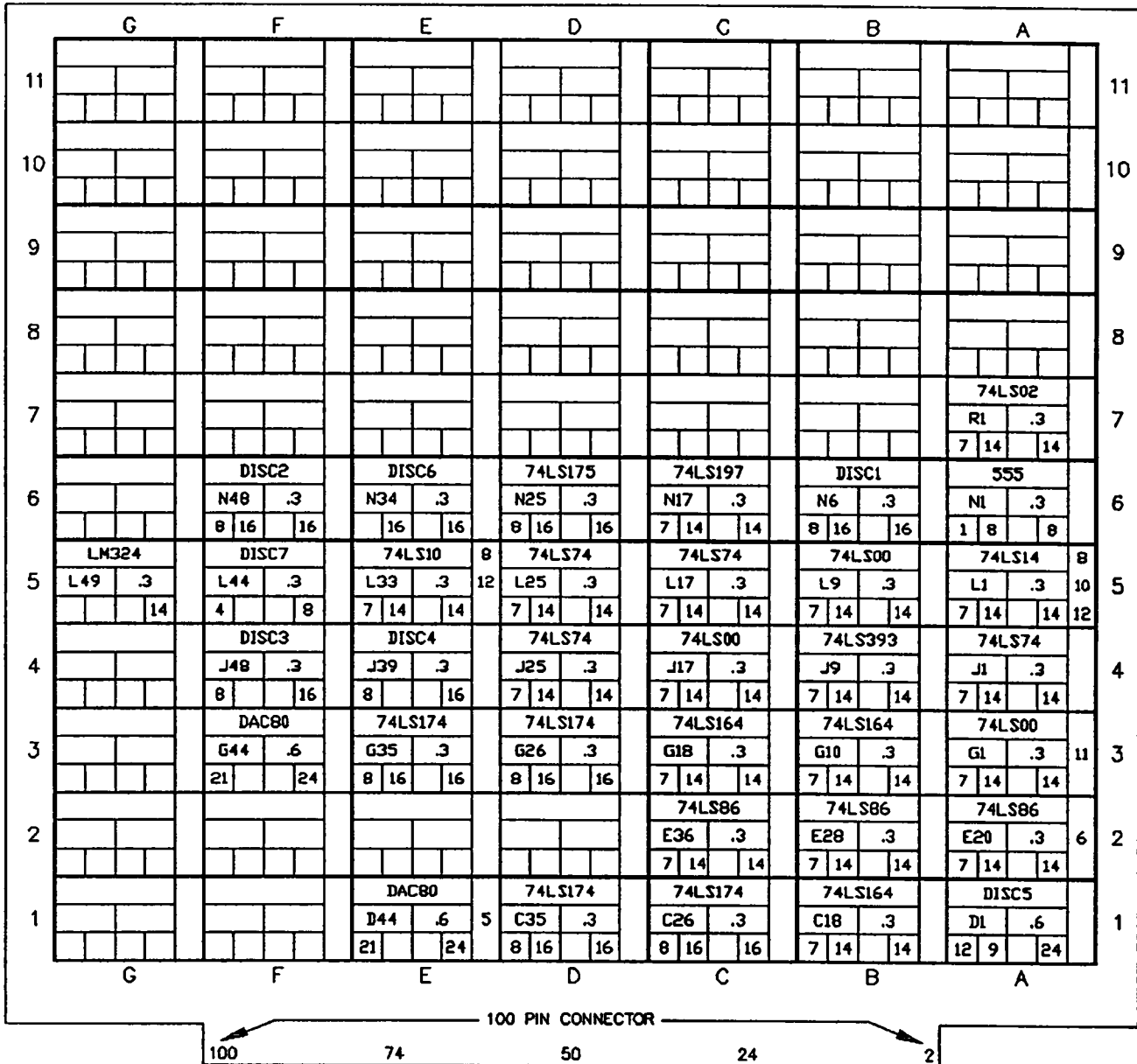
Appendix A

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

ACAD : TSL-ASSY	V L A	P L O R T	WEATHER STATION	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801						
	T I T L E		WEATHER STATION DEW POINT/AMBIENT TEMP CONVERTER ASSEMBLY	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">DRAWN BY ANDREATA</td> <td style="width: 30%;">DATE 11-91</td> </tr> <tr> <td>DESIGNED BY WEIMER</td> <td>DATE 11-91</td> </tr> <tr> <td>APPROVED BY</td> <td>DATE</td> </tr> </table>	DRAWN BY ANDREATA	DATE 11-91	DESIGNED BY WEIMER	DATE 11-91	APPROVED BY	DATE
DRAWN BY ANDREATA	DATE 11-91									
DESIGNED BY WEIMER	DATE 11-91									
APPROVED BY	DATE									
C13720S34										
NEXT ASSEMBLY	SCHEMATIC DWG. TYPE	SHEET NUMBER 1 of 7	DRAWING NUMBER A13720P23	REV. SCALE —						

WIRE WRAP BOARD COMPONENT LOCATION

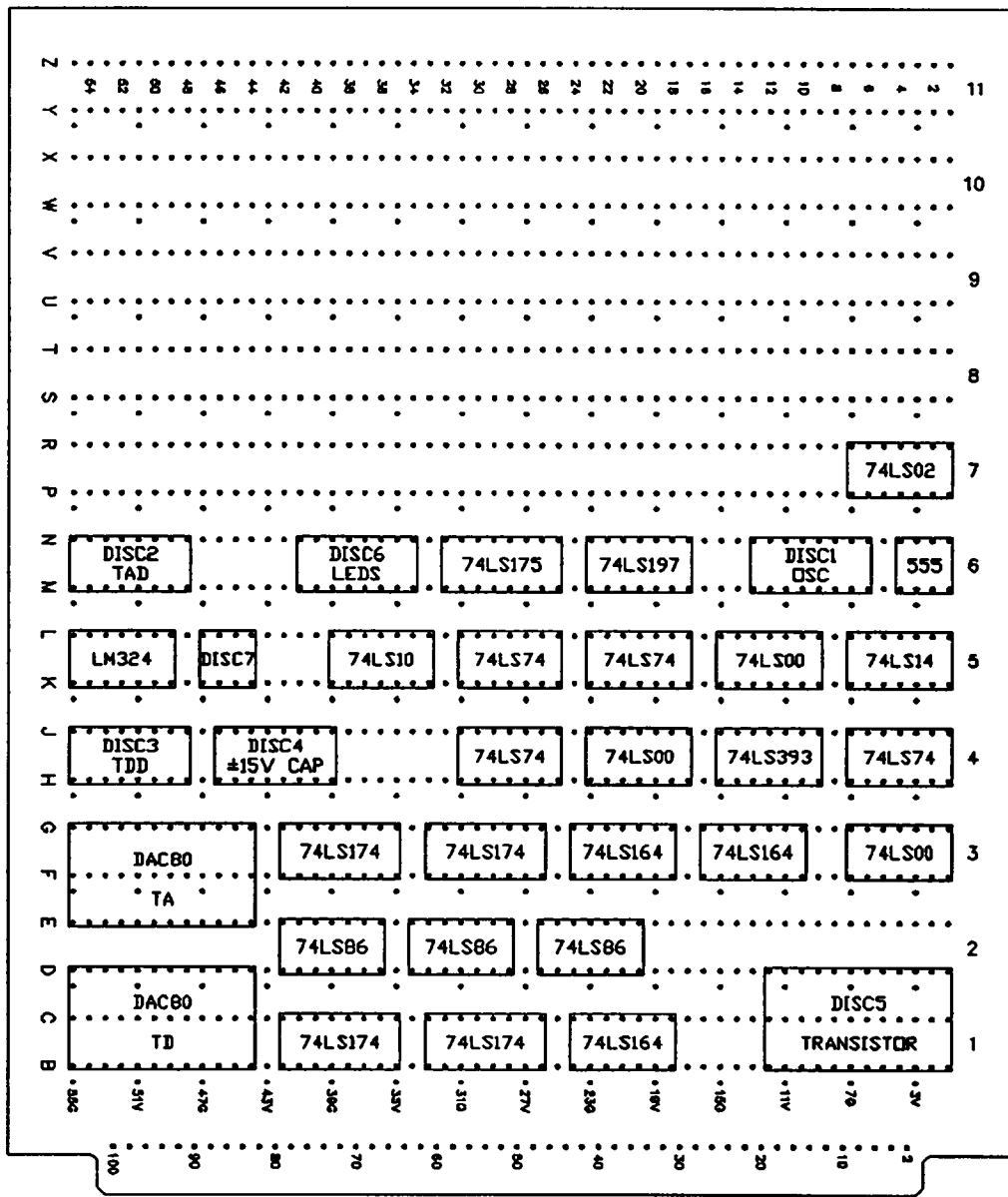
LOCATION _____



- NOTES :**
1. TOP VIEW, COMPONENT SIDE
 2. THIS COLUMN NOT AVAILABLE
 3. VCC CONNECTOR PINS :
P2,4,98,100
GND CONNECTOR PINS :
P1,3,27,49,73,97,99

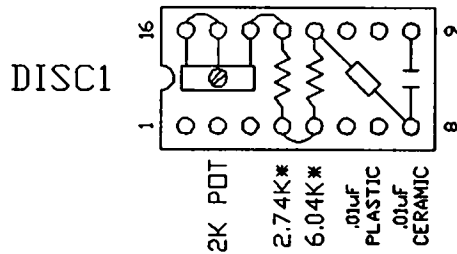
.019 uF ERIE RED CAP CAPACITOR PLUGGED INTO VCC AND GND ASSOCIATED WITH IC

DWG. NO.	A13720P23	SHT. NO.	2 of 7	REV.
----------	-----------	----------	--------	------

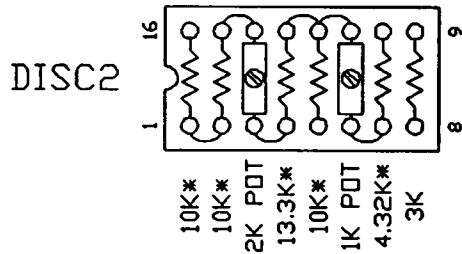


DWG. NO.	A13720P23	SHT. NO.	3 of 7	REV.
----------	-----------	----------	--------	------

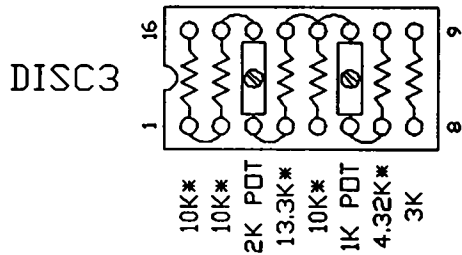
DISCRETE CHIP LAYOUT



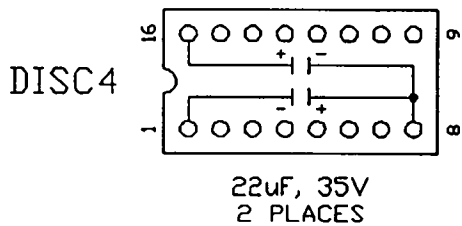
LOCATION = 6B
PIN #1 = N6
* = USE 1% RESISTORS



LOCATION = 6D
PIN #1 = N48
* = USE 1% RESISTORS



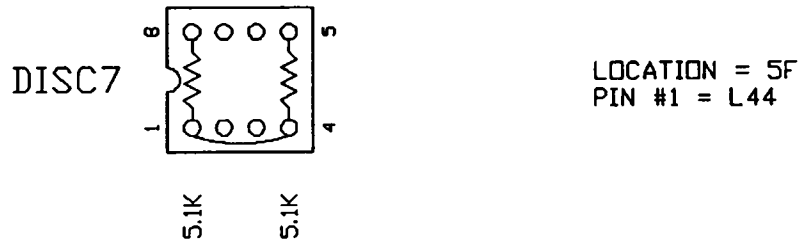
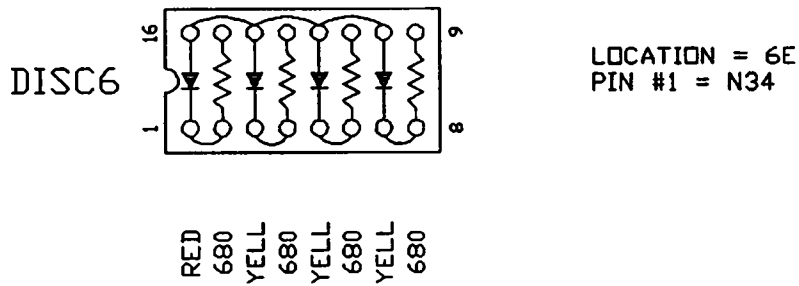
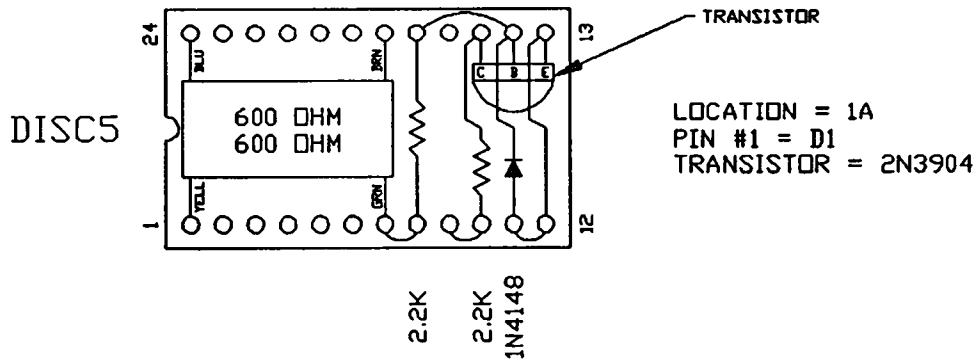
LOCATION = 4F
PIN #1 = J48
* = USE 1% RESISTORS



LOCATION = 4E
PIN #1 = J39

DWG. NO.	A13720P23	SHT. NO.	4 of 7	REV.
----------	-----------	----------	--------	------

DISCRETE CHIP LAYOUT



DWG. NO.	A13720P23	SHT. NO.	5 of 7	REV.
----------	-----------	----------	--------	------

PARTS LIST

<u>DISCRIPTION</u>	<u>QUANTITY</u>
74LS00	3
74LS02	1
74LS10	1
74LS14	1
74LS74	4
74LS86	3
74LS164	3
74LS174	4
74LS175	1
74LS197	1
74LS393	1
555	1
LM324	1
DAC80	2
24 PIN X .6" HEADER	1
8 PIN X .3" HEADER	1
16 PIN X .3" HEADER	5
SHALLOWWAY BOARD	1
.01uF POLY CAPACITOR	1
.01uF CERAMIC CAPACITOR	1
22uF, 35V CAPACITOR	2
.047uF GLASS DECOUP CAPACITOR	30
600 : 600 TRANSFORMER	1
RED LED	1
YELLOW LED	3
2N3904 TRANSISTOR	1
1N4148 LED	1
2K OHM POT	3
1K OHM POT	2
5%, 1/4W, 2.2K OHM RESISTOR	2
5%, 1/4W, 3K OHM RESISTOR	2
5%, 1/4W, 680 OHM RESISTOR	4
5%, 1/4W, 5.1K OHM RESISTOR	2
1%, 2.74K OHM RESISTOR	1
1%, 4.32K OHM RESISTOR	2
1%, 6.04K OHM RESISTOR	1
1%, 10K OHM RESISTOR	6

DWG. NO.	C55006A011	SHT. NO.	6 of 7	REV.
-------------	------------	-------------	--------	------

NAME	BACK PIN #	TO	FROM	NAME	FRONT PIN #	TO	FROM
GND	1	BLK		+5	2	VHT/RED	
GND	3			+5	4		
	5				6		
	7			DATA IN #1	8	TB12-3	
	9				10		
	11			DATA IN #2	12	TB12-4	
	13				14		
	15				16		
	17				18		
	19				20		
	21				22		
	23				24		
	25				26		
GND	27				28		
	29				30		
	31				32		
	33				34		
	35				36		
	37				38		
	39				40		
	41				42		
	43				44		
	45				46		
	47				48		
GND ±15V	49	BLK ←	← TB6-2,6,8		50		
	51				52		
	53				54		
	55				56		
	57				58		
	59				60		
	61				62		
	63				64		
	65				66		
	67				68		
	69				70		
	71				72		
GND	73	BLK			74		
	75				76		
+15V	77	RED		+15V	78	RED	
	79				80		
-15V	81	YELL		-15V	82	YELL	
	83				84		
	85			VTA	86	TB6-1	
	87				88		
	89			VTD	90	TB6-5,7	
	91				92		
	93				94		
	95				96		
GND	97			+5	98		
GND	99	BLK		+5	100	VHT/RED	

DWG. NO. A13720P23

SHT. NO. 7 of 7

REV.

Appendix B

* THIS IS A CIRCUIT THAT CONVERTS THE BIPHASE OUTPUT OF THE
 * TSL HYDROMETER TO TWO ANALOG VOLTAGES REPRESENTING THE CURRENT
 * AMBIENT TEMP AND DEW POINT TEMP.
 * THE SCALING IS: -45 DEG C = 0 VOLT
 * +60 DEG C = +5.0 VOLT
 * DATE: 24 JUNE 1991
 * CREATED BY RON WEIMER
 * VERSION 3
 * REVISED : 27 JUNE 1991
 * CORRECTED A NUMBER OF PROBLEMS--ADDED A CIRCUIT TO INHIBIT D/A UPDATE
 * IF THE ERROR FLAG IS SET BY THE TSL TRANSMITTER
 *
 *
 *

DECLARE

*LCN	#PINS	PIN1LCN	TYPE	VCC	GND	COMMENTS
1A	24	D1	2	9	12	*DISC5 INPUT TRANSFORMER
1B	14	C18	1	14	7	*74LS164
1C	16	C26	1	16	8	*74LS174
1D	16	C35	1	16	8	*74LS174
1E	24	D44	2	0	21	*DAC80
2A	14	E20	1	14	7	*74LS86
2B	14	E28	1	14	7	*74LS86
2C	14	E36	1	14	7	*74LS86
3A	14	G1	1	14	7	*74LS00
3B	14	G10	1	14	7	*74LS164
3C	14	G18	1	14	7	*74LS164
3D	16	G26	1	16	8	*74LS174
3E	16	G35	1	16	8	*74LS174
3F	24	G44	2	0	21	*DAC80
4A	14	J1	1	14	7	*74LS74
4B	14	J9	1	14	7	*74LS393
4C	14	J17	1	14	7	*74LS00
4D	14	J25	1	14	7	*74LS74
4E	16	J39	1	0	8	*DISC4
4F	16	J48	1	0	8	*DISC3
5A	14	L1	1	14	7	*74LS14
5B	14	L9	1	14	7	*74LS00
5C	14	L17	1	14	7	*74LS74
5D	14	L25	1	14	7	*74LS74
5E	14	L33	1	14	7	*74LS10
5F	8	L44	1	0	4	*DISC7
5G	14	L49	1	0	0	*LM324
6A	8	N1	1	8	1	*555
6B	16	N6	1	16	8	*DISC1
6C	14	N17	1	14	7	*74LS197
6D	16	N25	1	16	8	*74LS175
6E	16	N34	1	16	0	*DISC6
6F	16	N48	1	0	8	*DISC2
7A	14	R1	1	14	7	*74LS02

*
 *
 *
 *

WIRELIST

* EXTRA GROUNDS AND VCC
 S 4A14 4A4 4A1 4A13 4A10 S 5C14 5C13 5C10 5C4 5C1
 S 6C14 6C1 S 6A8 6A4 S 4D14 4D13 4D10 4D1 S 3B14 3B9
 S 3C14 3C9 S 1B14 1B9 S 2A14 2A12 S 6D16 6D1 S 3D16 3D1
 S 3E16 3E1 S 3F21 3F11 3F12 S 1C16 1C1 S 1D16 1D1 S 1E21 1E11 1E12

S 4D7 4D2 S 1A12 1A1
S 5D14 5D13 5D10 5D1
S 3E8 3E13 3E14 S 1D8 1D13 1D14 S 5D7 5D2
* I/O Pins
S P8 1A24 S P12 1A18 S P86 5G7 6F10 S P90 5G8 4F10
* +15 VOLT
S P77 1E22 3F22 4E16 5G4 S P78 5G4
* -15 VOLT
S P81 1E14 3F14 4E1 5G11 S P82 5G11
* CLOCK / DATA RECOVERY
S 1A15 5A1 S 5A2 4A2 S 4A5 4A12 2A1 S 4A9 2A2 S 2A3 5B9 5E3
S 5B8 5D4 S 5E6 5D3 5D11 5C2 S 5D12 5D5 S 5D8 5B13
S 5C5 5C12 6C13 S 5A6 5B1 4A3 4A11 5C3 5C11 4D11 S 5B3 5A3
S 5A4 6C8 S 6C5 6C6 S 6C2 5B4 5E4 S 6C12 5B5 5E5 S 5B6 5B2 5B10
S 6B4 6A7 S 6B12 6A6 6A2 S 6A5 6B9 S 6A3 5A5 S 5C8 5B12 4C1
S 5B11 4D4 S 5D9 3B1 3E2
* START STOP CONTROL
S 4D5 4C2 S 4C3 4C4 4C5 3B8 3C8 1B8
S 4C6 4B1 S 4B6 4B13 4C12 S 4B11 4C13 S 4C11 4C10 4C9 S 4C8 4D12 4D3
S 4D9 4B12 4B2 6D9 S 4D8 7A2 S 7A1 3A5 3A10
S 3B13 3C1 3C2 2C13 S 3C13 1B1 1B2 3A1 3A2 3A9 6D5
S 3A3 3A4
* SHIFT OUT
S 3B11 2B5 S 3B12 2B2 S 3C3 2C10 S 3C4 2C5 S 3C5 2C2 S 1B3 6D4 7A3
S 1B5 6D12 2A13 2A9 2B12 2B9 2B4 2B1 2C12 2C9 2C4 2C1
S 1B10 6D13 2A10 S 1B11 2B13 S 1B12 2B10
* LED DRIVE
S 6D3 6E15 S 6D6 6E13 S 6D11 6E11 S 6D14 6E9
* DATA LATCH
S 3A6 3D9 3E9 S 3A8 1C9 1D9
S 2A11 3D3 1C3 S 2A8 3D4 1C4
S 2B11 3D6 1C6 S 2B8 3D11 1C11 S 2B6 3D13 1C13 S 2B3 3D14 1C14 S 2C11 3E3 1D3
S 2C8 3E4 1D4 S 2C6 3E6 1D6 S 2C3 3E11 1D11
* D/A INPUTS AMB
S 3D2 3F1 S 3D5 3F2 S 3D7 3F3 S 3D10 3F4 S 3D12 3F5 S 3D15 3F6 S 3E2 3F7
S 3E5 3F8 S 3E7 3F9 S 3E10 3F10
* D/A OUTPUT AMB
S 3F24 3F16 6F16 S 3F15 3F18 6F5 S 3F17 3F20
S 6F1 5G2 S 5G1 6F15 S 6F13 5G6 S 5G5 6F9
* D/A INPUTS DEW
S 1C2 1E1 S 1C5 1E2 S 1C7 1E3 S 1C10 1E4 S 1C12 1E5 S 1C15 1E6 S 1D2 1E7
S 1D5 1E8 S 1D7 1E9 S 1D10 1E10
* D/A OUTPUT DEW
S 1E24 1E16 4F16 S 1E15 1E18 4F5 S 1E17 1E20
S 4F1 5G13 S 5G14 4F15 S 5G9 4F13 S 5G10 4F9
* EXTRA RESISTORS
S 5G3 5F5 S 5G12 5F8
*
*
END