Plan for VLA High Time Resolution Processor (HTRP)

(Previously known as Phased Array Processor)

March 23, 1988

Major Capabilities:

Sample VLA IFs with time constants of 0.2 to 4 milliseconds and 32/64 channels
Interface to correlator for (Pulsar) gating
Sample and Display VLA "system" data

Scientific Applications:

Flare stars
Pulsar studies including control of sample gating of pulses/non-pulses
Short time scale solar event studies
Search for coherent emission components
Scintillation studies
Occultations

"Available" Components:

Outputs of analog sum port panel
Current System for IF conversion and VLBI Mark III IF Distrib. and Video Conversion
Master LO System for timing
Labmaster, 12-bit DMA A/D converter with 40,000 sample/sec capability

Additional Components to be Obtained:

Integrators to give 0.2 to 4 ms sampling in up to 32/64 channels
HTRP computer – AT-compatible, 80386/80387 ($\geq$ 16 MHz), $\geq$ 130 MByte disk drive
High capacity tape storage - 6250 bpi tape or video tape storage before 6250 bpi tape
Software in C for HTRP computer and exportability to VAX/CONVEX

Responsibilities:

Mark McKinnon – Most of real work on hardware, software, and his Ph.D. thesis
Durga Bagri – Engineering design and advice
Ken Sowinsky – Advice on interfacing to on-line system and correlator
Pat Crane – Advice on VLBI interfacing
Tim Bastian – Advice on specifications/use; liason with non-NRAO people; thesis advice
Bob Hjellming – Coordination; assisting on computer hardware/software; thesis supervisor

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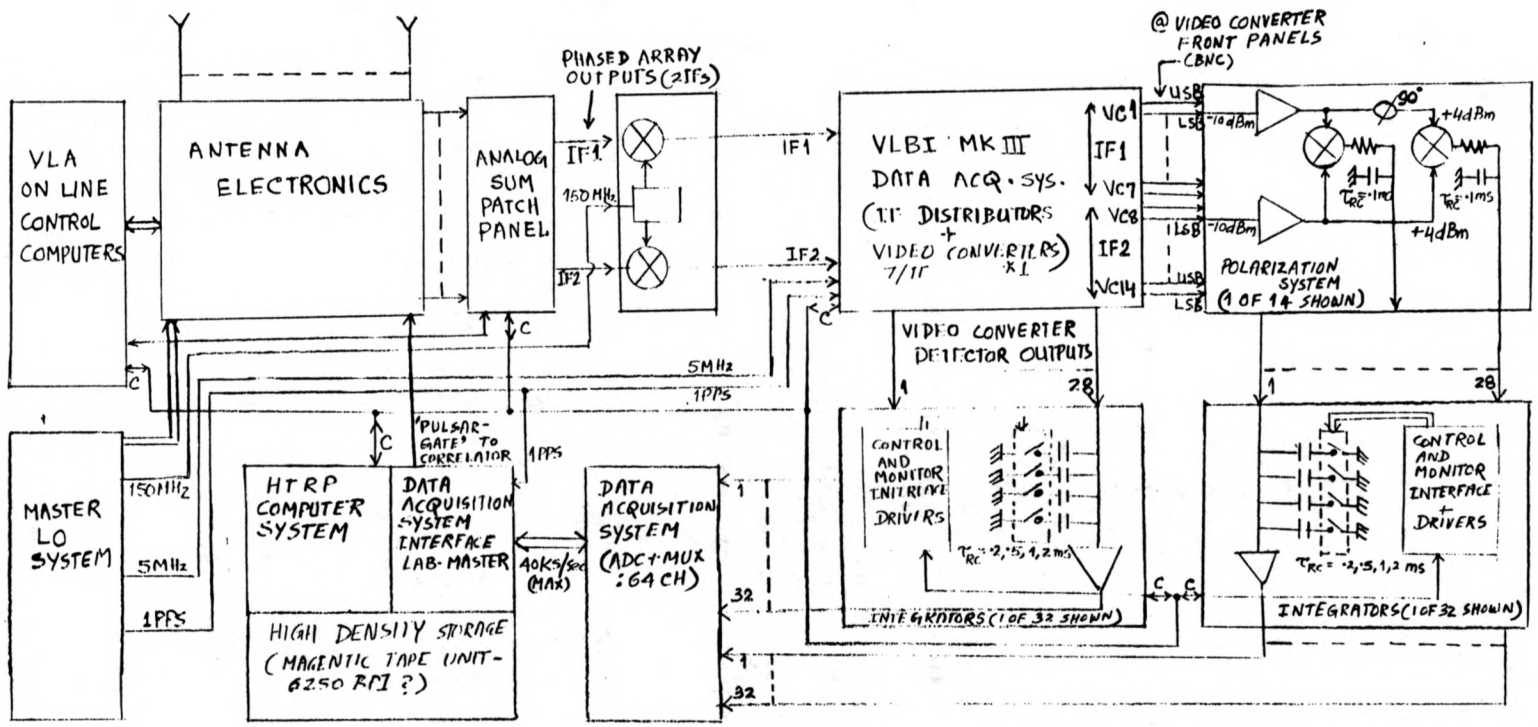

C = RS232 FULL DUPLEX COMMUNICATION

*1 = ALL BUT 4 VIDEO CONVERTERS HAVE ONLY 2&4 MHz BAND-WIDTH FILTERS - INSTALLED; SWITCHING HARDWARE FOR ALL FILTERS EXISTS?

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

PROJECT

TITLE: BLOCK DIAGRAM: HIGH TIME RESOLUTION PROCESSOR (HTRP) FOR THE VLA

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