HTRP
MEMO NO. 104

May 20, 1988

To: M. Goss, R. Sramek, and J. Campbell

From: R. Hjellming

Subj: Status of Plans for High Time Resolution Processor (HTRP) at the VLA

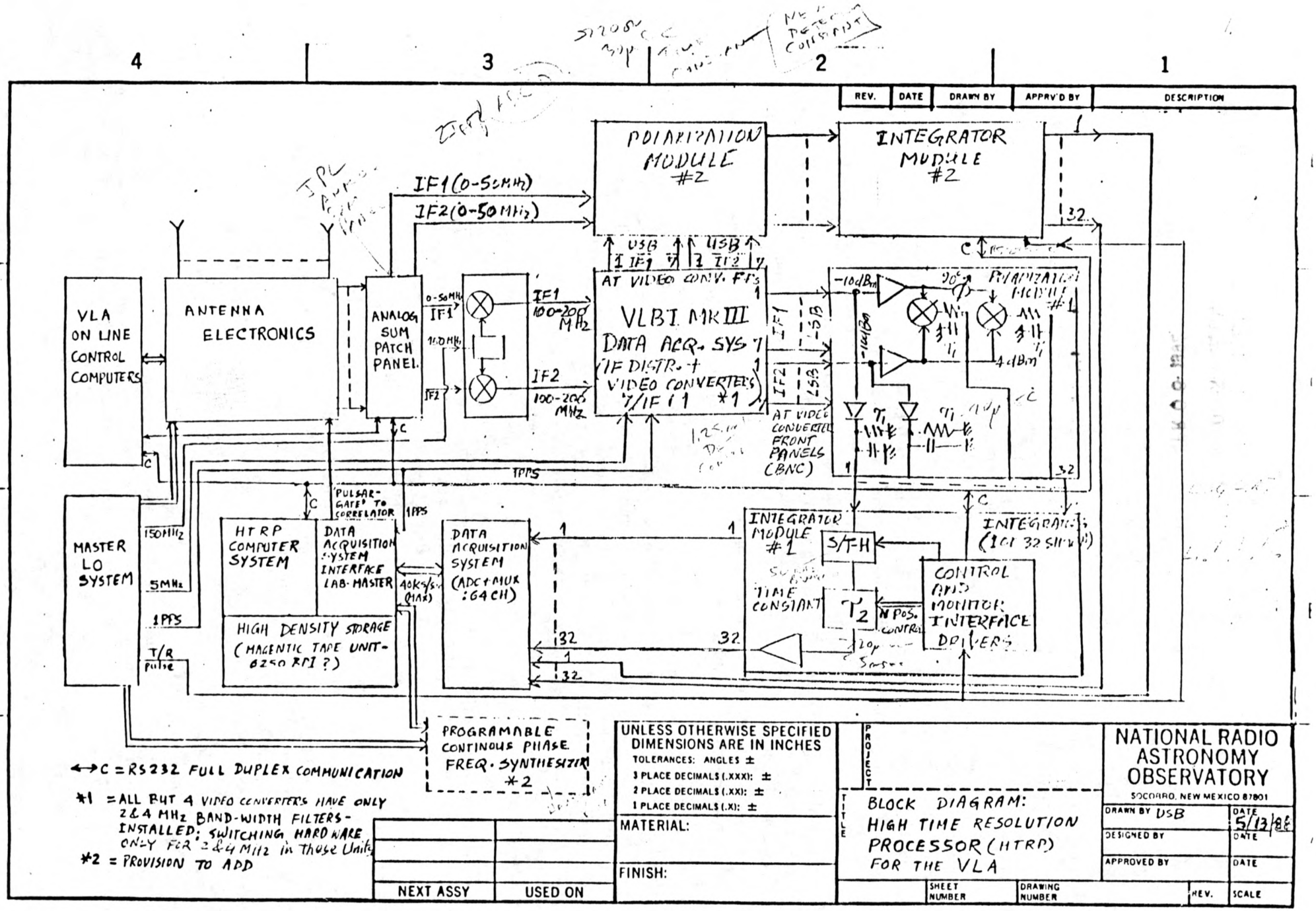
The basic outline of the design (and specifications) of the High Time Resolution Processor system for the VLA, hereafter referred to as the HTRP, is now essentially complete. The purpose of this memo is to summarize the current concept and our plan of implementation.

The objective of this system is sampling of the VLA analog sum panel outputs at high time resolution for 32/64 frequency channels and 2/1 polarizations. It will use the JPL-modified analog sum panel and all but the detection part of the VLBI Mk III data acquistion system. Two IFs, from any combination of the VLA A, B, C, and D IFs will have channel/frequency selection by the VLBI Mk III hardware, but the detection phase of the latter hardware will be replaced by a dual system consisting of two polarization modules, with a fundamental time constant of 20-30 microsec. Each polarization module will be followed by an integrator module with sample and hold circuits allowing simultaneous sampling in 16 channels and 2 polarization with integrations times selectable in factors of two from the fundamental time constant of the polarization modules up to 5 millisec. Each integrator module will deliver 32 channels of data to a data acquisition system with a maximum sampling rate of 40,000 (12-bit) samples per second, leading to a data rate of 60-80 KByte/sec, depending upon whether one packs and unpacts the 12-bit samples. The data acquistion system will reside in the HTRP computer system.

The HTRP computer system will be a 20 MHz 80386/80387 computer with at least a 130MByte hard disk and the obvious peripherals and at least 640X400 or 768X348 monochrome graphics. It will be installed with an Ethernet card allowing a DECNET connection to the VLA VAX/CONVEX computers. A major requirement is that the system have AT-compatible slots for users to install their own signal processing boards. Eventually a 6250 bpi, 9 track tape drive may record the data stream, but initially we plan to use a "Gigastore" device based upon VCR technology, which is currently available for computers of this type, with a capability to record (in streaming mode) 120 KBytes/sec for up to 6 hours. The basic concept is that the latter device will record data during observing, then it will be transferred later from VCR tape to other computers with tape drives. We initially plan to delay direct use of a tape drive, in part because a single 6250 bpi tape will hold slightly less than an hour of data (sampling at maximum rate), and the only extensive experience in the PC industry with tape drive on PCs deals with lower density tapes and much lower data rates. Later in the project it is planned to have a programmable, continuous phase, frequency synthesizer.

We plan to procure the computer system in June 1988, immediately connecting it to the analog sum panel, with the Ethernet/DECNET connection to our other computers. The immediate objective is sampling of the current analog sum ports to study stability and get preliminary experience with HTRP processing and display of these signals. The detailed design of the modules will proceed during the summer of 1988 with operation of at least one polarization/integrator module system using the 1.25 millisec detectors of the VLBI Mk III system in the fall of 1988. We plan to defer purchase of the Gigastore device until later in 1988, assuming it is still the preferred mass storage device.

Mark McKinnon will be responsible for hardware integration and software development in the HTRP computer as part of his Ph.D thesis, with supervision by D. Bagri and R. Hjellming and close collaboration with the the groups headed by Larry Beno and Dave Weber. These groups will be involved in the building of the polarization and integrator modules, respectively.



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PROJECT

TITLE: BLOCK DIAGRAM: HIGH TIME RESOLUTION PROCESSOR (HTRP) FOR THE VLA

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