HTRP Bench Test Results

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I. Introduction.

The purpose of this memorandum is to document bench testing of the HTRP. The testing is similar to what was conducted for the prototype set of phase-shift, detector, and integrator cards (memorandum dated March 21, 1990). The objectives of the tests were (1) verify detector output voltage is linear with input power, (2) verify that signal phase as determined by cross-product detector outputs is constant with input power, (3) verify the actual integration times are consistent with their nominal values, (4) verify that the integrator cards respond to computer commands by checking configured integration times and voltage bias offsets, and (5) verify that signals are routed to their proper locations on appropriate connectors.

The test results show that the detectors, integrators, bias offsets, and computer communications perform very well. All signals were properly routed to their assigned locations. The dynamic range is not restricted by non-linear phase behavoir as was previously thought. Power supply noise appears to be present in the detector outputs.

II. Test Procedure.

The detector linearity testing was conducted by connecting the output of a signal generator to a power splitter. The two outputs of the power splitter were connected to the RCP and LCP inputs of a single channel on the HTRP. The lengths of the cables between the power splitter outputs and HTRP inputs were approximately the same. The output of each detector (RR, LL, RL, and LR) was measured for different values of the signal generator sinusoid amplitude. The input power was measured with a power meter at one of the power splitter outputs. With this test configuration, the right circular polarization (RCP) and left circular polarization (LCP) inputs are approximately in phase. Therefore, the RL output should ideally be zero ($\sin 0 = 0$). Signal in RL was treated as a phase error, which was computed as $\arctan(RL/LR)$ after RL and LR were compensated for bias offset. The bias offset is the detector output when no signal is applied to the detector. This correction was not applied to the data in the HTRP memorandum which discussed allowable operating ranges. Not correcting for bias led to the seemingly real behavior of non-linear phase at small input power. Thus, the *incorrect* conclusion was drawn that the HTRP dynamic range was restricted to a small range of input power where the phase was constant. The detector linearity test procedure was conducted for all 16 sets of phase-shift and detector cards at a signal generator frequency of 2.0MHz.

The integration time test configuration was identical to that for the detector linearity test except the signal generator output was amplitude-modulated with a 20Hz square pulse. Also, a 37-foot cable was inserted between one power splitter output and its corresponding HTRP input to introduce a phase offset (about 41 degrees at 2.0MHz for a dielectric constant of 2.3). The long cable insured the presence of a signal in the RL detector

output so the RL integration time could be measured. The amplitude-modulation caused the capacitor in the RC integrator to repeatedly charge and discharge. Since the voltage across a capacitor in an RC circuit varies as

$$V_c = E_o(1 - e^{-t/RC}), \tag{1}$$

the integration time can be measured with an oscilloscope at $t = RC$ when $V_c = 0.632E_o$. The integration times for all four detected outputs were varied under computer control between nominal values of 25, 50, 100, 200, 500, 1000, 2000, and 5000 microseconds. The input power was not varied during the measurement of integration times. The integration time tests were conducted for 14 of the 16 integration cards. Two of the integration cards needed additional quality control checks.

III. Results and Discussion.

The performance of each detector set was evaluated with three figures which show the variation of RR detector output, LL detector output, and phase with input power. Each detector set consists of a phase-shift card and a detector card. Ideally, the detector output should vary linearly with input power, and the phase error should remain constant at zero degrees with input power. Realistically, the detector output will saturate at some large output power, and the phase error will be constant and non-zero.

The plots of detector outputs versus input power show the measured values (open circles) and a least squares fit to the data (solid line). The equation of the fit is shown in the upper left-hand corner of each figure. The detector gains listed in Table A are the slopes of the lines in each plot. As can be seen in the figures, all parallel-product detectors display the desired linear response. All detectors saturate at a detector output voltage around 4.0 volts. The nominal design point of the detectors was a 1.0 volt response for a 0.1 milliwatt input, corresponding to a gain of 10 volts per milliwatt. All detectors show a gain less than the nominal value. The actual value of the gain is not important; however, the gain for all detectors in one polarization (RR or LL) should be approximately the same so that a single detector does not restrict the dynamic range of all channels. Additionally, the average gain of the RR detectors should be approximately equal to the average gain of the LL detectors so that the dynamic range of one polarization does not limit the other. The average gains of the RR and LL detectors are 7.85 ± 0.83 and 7.72 ± 0.81, respectively. The small gain errors indicate that dynamic range is not strongly limited by a single channel in one polarization. As can be seen in Table A, the dynamic ranges in RCP and LCP will ultimately be determined by detectors 12 and 16, respectively, because these detectors have the largest gains in one polarization and will be the first to saturate. The dynamic range is not strongly restricted by one polarization because the RR and LL average gains are equivalent within the calculated errors.

The plots of phase error versus input power show that the phase offset is constant over the input power range for most detector sets. The dashed line in the plots is the average of eight phases measured at intermediate input powers. The average phase offset for each detector set is listed in Table A. The deviation from constant phase at large input power is due to detector saturation. The deviation at small input power is due to the error in

the measured values of the RL and LR detector bias offsets. Detector set 11 showed an unusually large phase offset which varied with input power. Further investigation revealed that a capacitor with a capacitance which differed from the design value had been installed on detector card 11. The detector has since been repaired. The phase offset of detector set 7 is also unusually large, and should be checked for similar problems. The performance of the detector sets indicates they are capable of less than one degree deviation over the input power range.

The source of the phase offset in the cross product detector outputs may be explained by analyzing the expressions derived for RL and LR in the memorandum on polarization calibration dated March 12, 1990. The expressions for RL and LR are equations 34 and 35, respectively, in the memorandum. For the nearly ideal bench-testing arrangement, one may neglect the cross-coupling between inputs discussed in the polarization calibration memorandum. In this case the equations for RL and LR become

$$RL = \frac{1}{2} B_{RL} P \sin(\phi - \psi_{RL}) \tag{2}$$

$$LR = \frac{1}{2} B_{LR} P \cos(\phi - \psi_{LR}) \tag{3}$$

where B_{RL} is the amplitude of the RL detector complex gain, ψ_{RL} is the phase of the RL detector complex gain, ϕ is the actual phase difference between RCP and LCP signals, and P is the polarization amplitude. B_{LR} and ψ_{LR} are the amplitude and phase, respectively, of the LR detector complex gain. If the RCP and LCP inputs are perfectly in phase ($\phi = 0$), the phase errors shown in the attached figures can be represented mathematically by

$$\theta = \arctan(RL/LR) = \arctan\left(\frac{-B_{RL}}{B_{LR}} \frac{\sin\psi_{RL}}{\cos\psi_{LR}}\right) \tag{4}$$

Equation (4) shows that a non-zero phase offset is due to non-zero ψ_{RL} and detector gain amplitudes which are not equal. The existence of a phase error allows one to immediately conclude that all RL detectors contribute an instrumental phase regardless of the detector gain ratios. Otherwise, the phase error would be zero ($\arctan(0) = 0$). A non-unity gain ratio also contributes to the phase error. From Table A, one sees for a given detector set, the RR and LL detector gains are different. Since all detectors, RR, LL, RL, and LR, are fundamentally the same electronic circuit, one can assume that the RL/LR gain ratios may have magnitudes similar to the RR/LL gain ratios (0.71 to 1.34 from Table A). The RL and LR gains were not determined directly in this analysis.

Stipulating $\phi = 0$ in the preceding analysis is a good assumption. The sources of external phase in the bench test are the power splitter and interconnecting cable. The power splitter introduces very little phase because it is purely resistive. The average phase error of all detector sets, excluding sets 7, 11, and 13, of -4.67 degrees would require a difference in input cable length of about 4.2 feet at 2.0MHz. Since the cables were of equal length and very short, they cannot account for the phase offset. It is interesting to note that the phase error is similar for most detector sets. This implies that the source of

the phase offset has been systematically designed or constructed into the detector sets or additional external phase sources have not been identified.

All eight possible integration times were checked for 14 integrator cards. Instead of tabulating all 112 integration times, I shall summarize the integrator card testing results by noting that all measured integration times were about ten percent larger than their design values. The fact that the design and actual integration times differ has no impact on the HTRP except that a user must have an idea of what the actual integration times are (e.g. Nyquist sampling). The monitor and control (MC) card responded to all computer commands, and the integrator cards were correctly configured for the appropriate voltage bias offset and integration time.

IV. Conclusions.

The following list identifies the highlights of HTRP bench testing:

(1) Detector outputs are linear with input power.

(2) Integration times are typically 10 percent larger than their nominal design values.

(3) Phase as determined by RL and LR is constant with input power for the detector sets.

(4) The dynamic range is not restricted by non-linear phase behavior at low input powers as was previously thought. The dynamic range is restricted by detector saturation at large input powers.

(5) The monitor and control card responded to computer commands, and the integrator cards were subsequently configured for the proper integration times and bias offsets.

(6) Power supply noise appears to be present in the detector outputs.

(7) Signals were routed to their proper locations on appropriate connectors.

V. References.

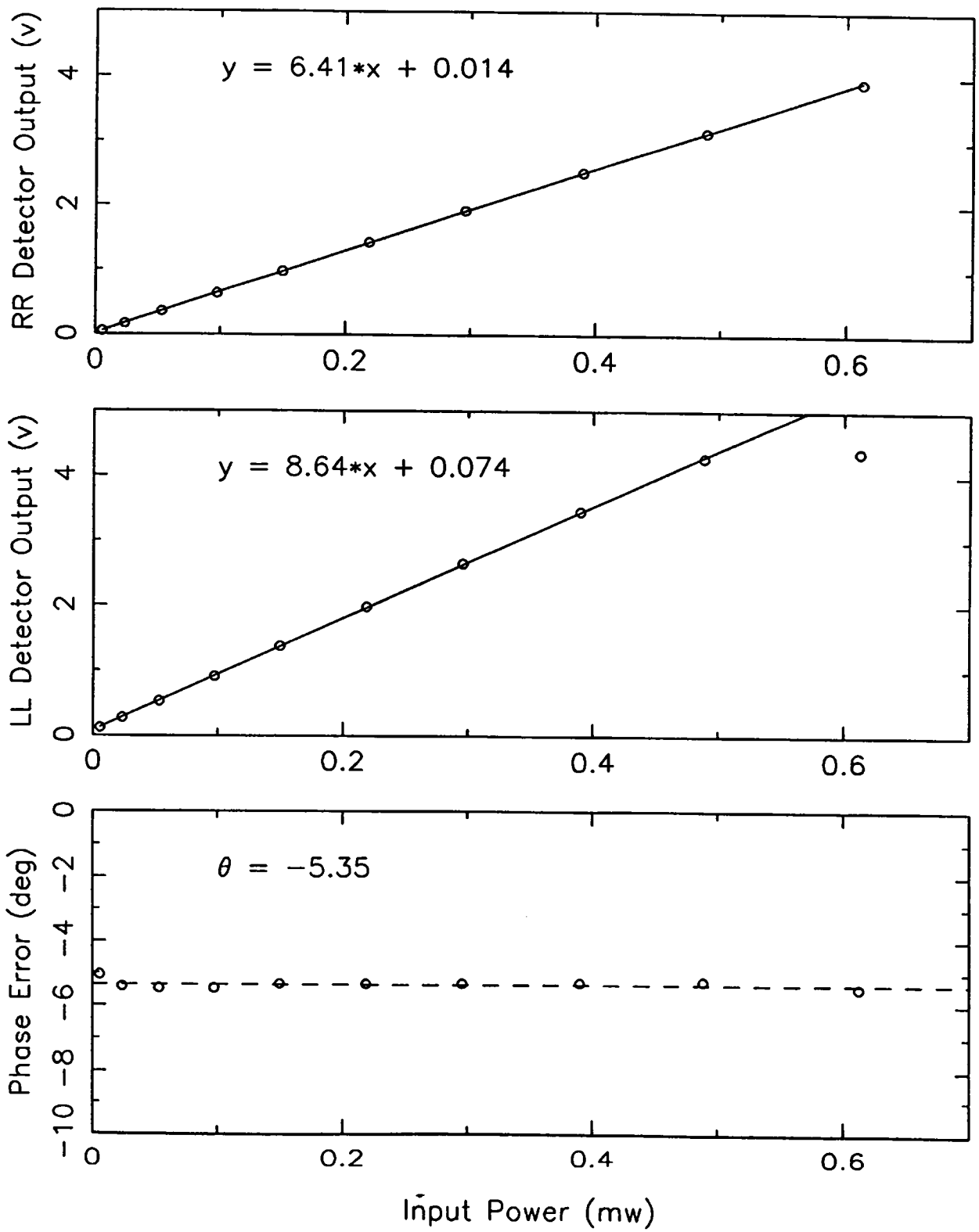
McKinnon, M.M., March 21, 1990, HTRP Memorandum: Allowable Operating Ranges for the HTRP.

McKinnon, M.M., March 12, 1990, HTRP Memorandum: Polarization Calibration of the VLA Analog Sum.

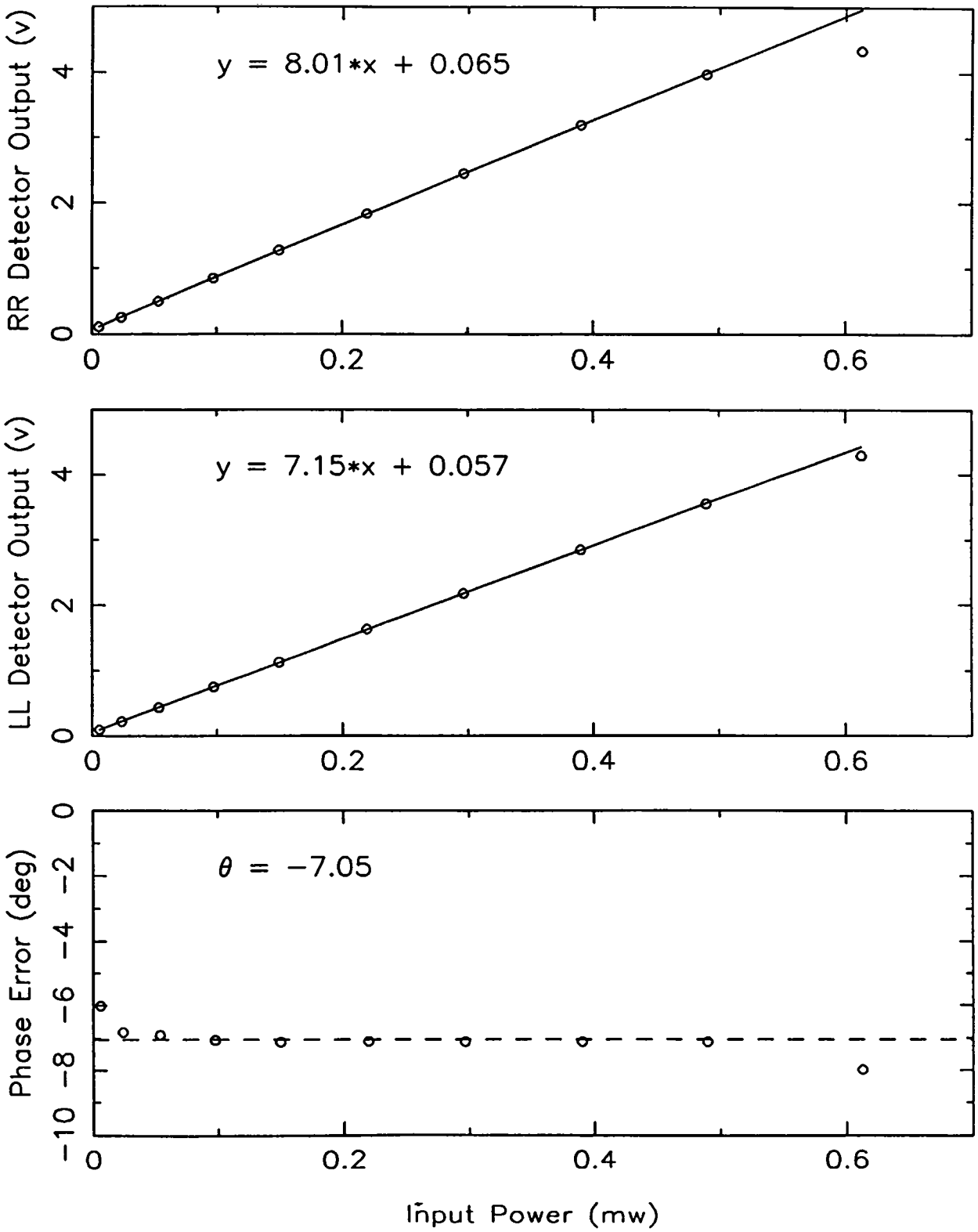
Table A. Gains and Phase Errors of HTRP Detectors.

Set	RR Gain (v/mw)	LL Gain (v/mw)	Phase Error (θ)
1	6.41	8.64	-5.35
2	8.01	7.15	-7.05
3	8.37	7.90	-6.95
4	8.66	7.71	-6.34
5	8.15	6.21	-2.39
6	8.20	8.39	-4.77
7	8.40	8.44	-15.25
8	8.16	8.11	-4.16
9	8.31	7.96	-3.61
10	6.93	7.61	-1.06
11	6.32	8.85	61.86
12	8.90	6.62	-4.58
13	8.38	6.87	-6.39
14	7.74	7.22	-5.24
15	6.54	7.07	-4.82
16	8.19	8.82	-4.39

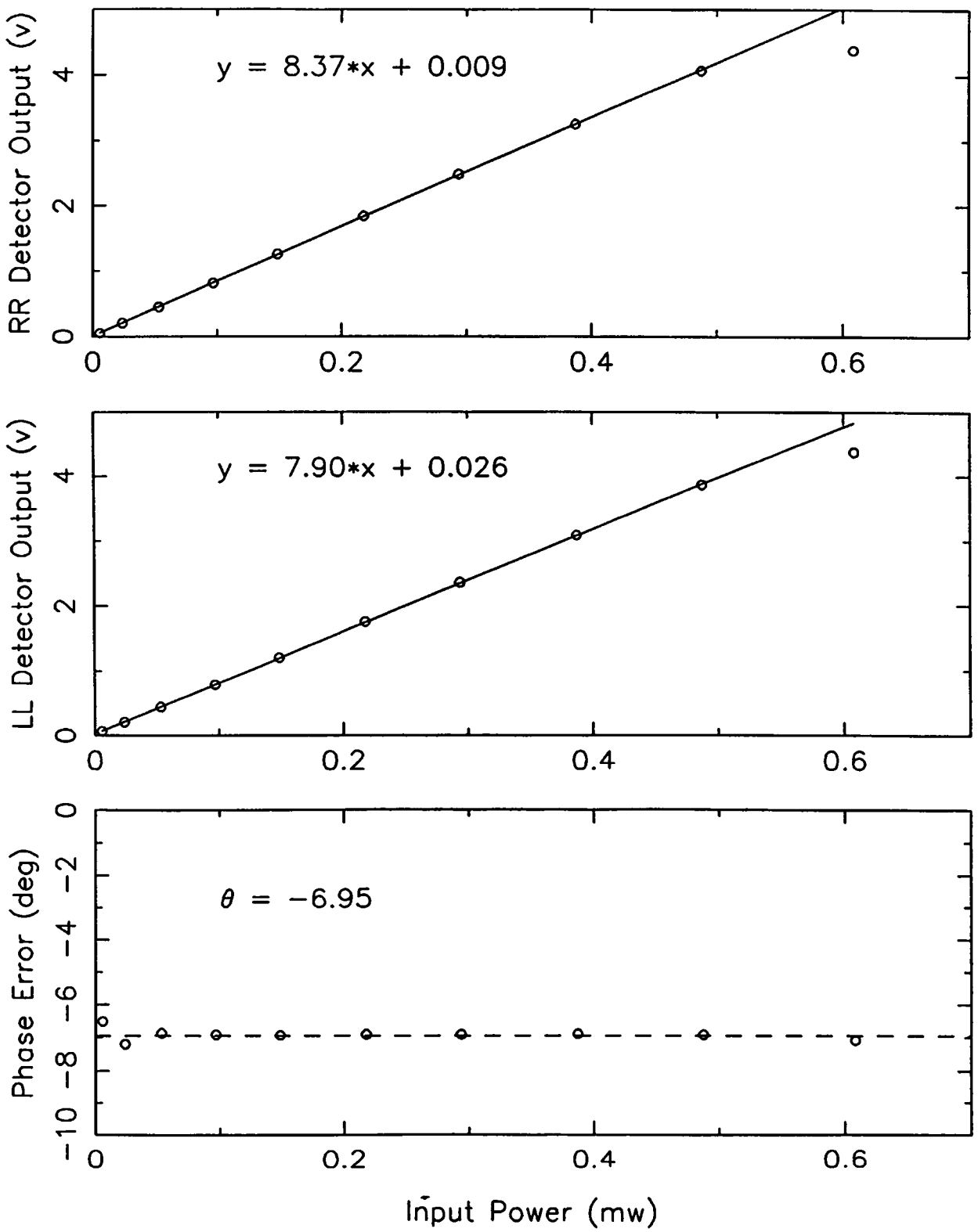
HTRP Detector Set 1 Performance



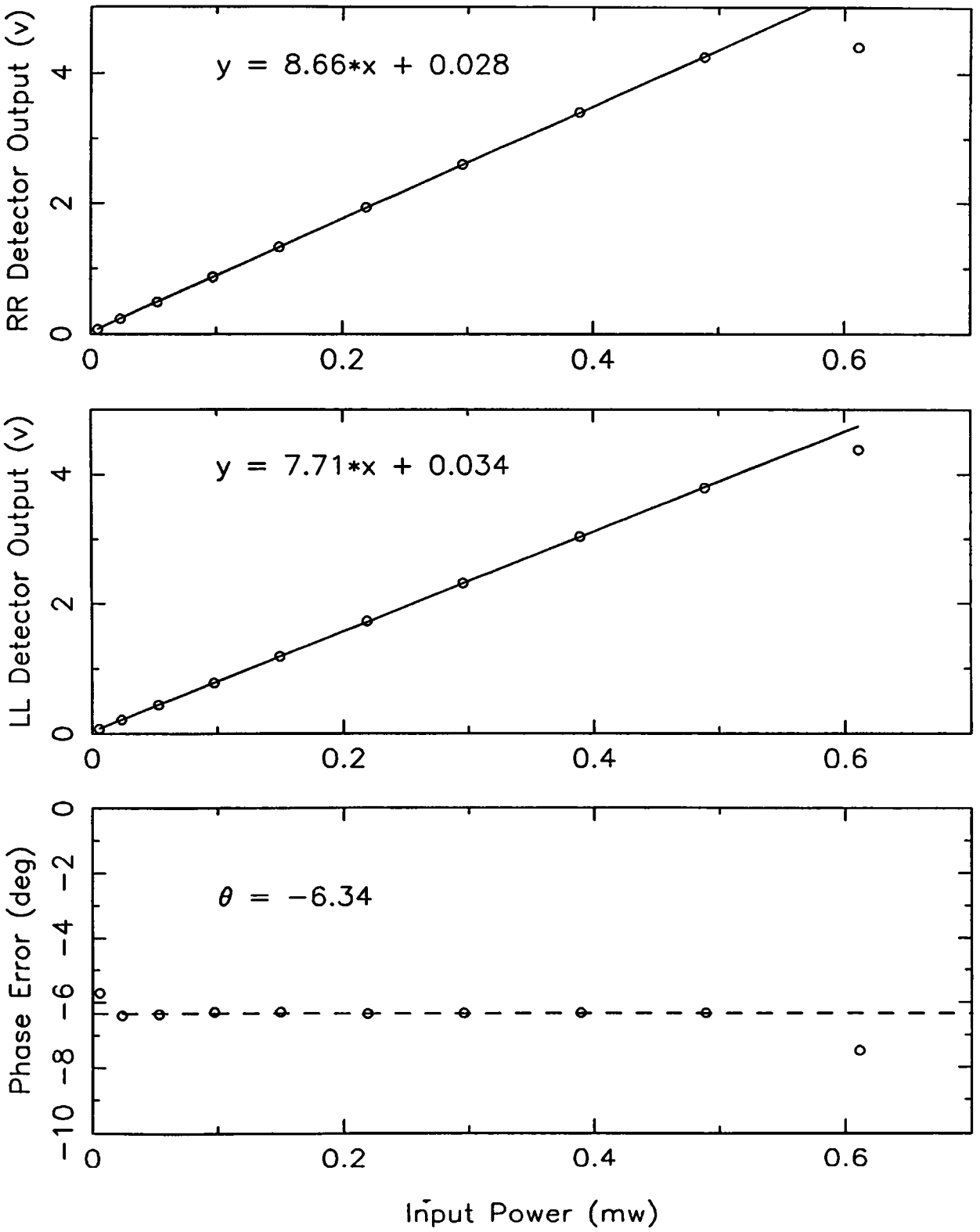
HTRP Detector Set 2 Performance



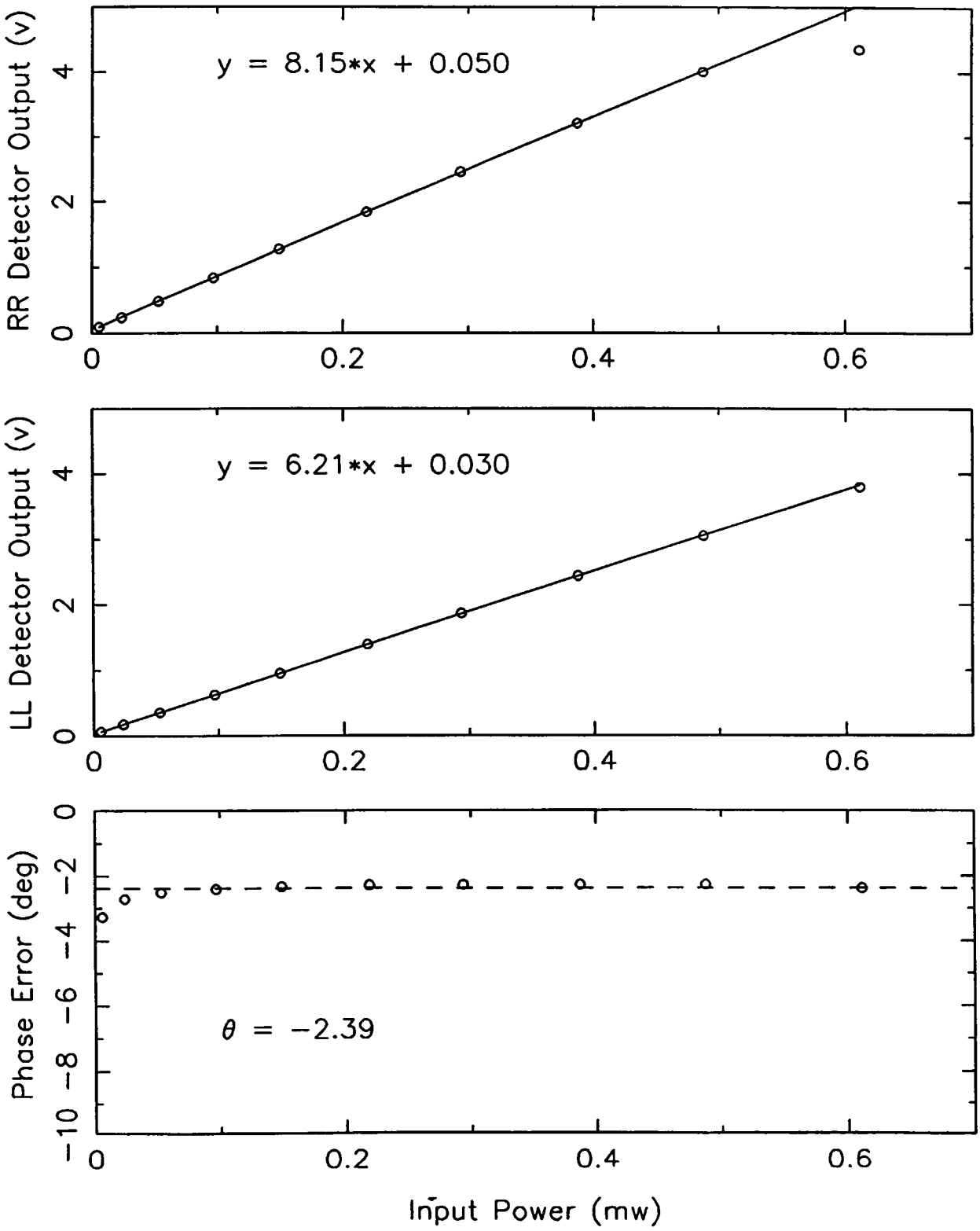
HTRP Detector Set 3 Performance



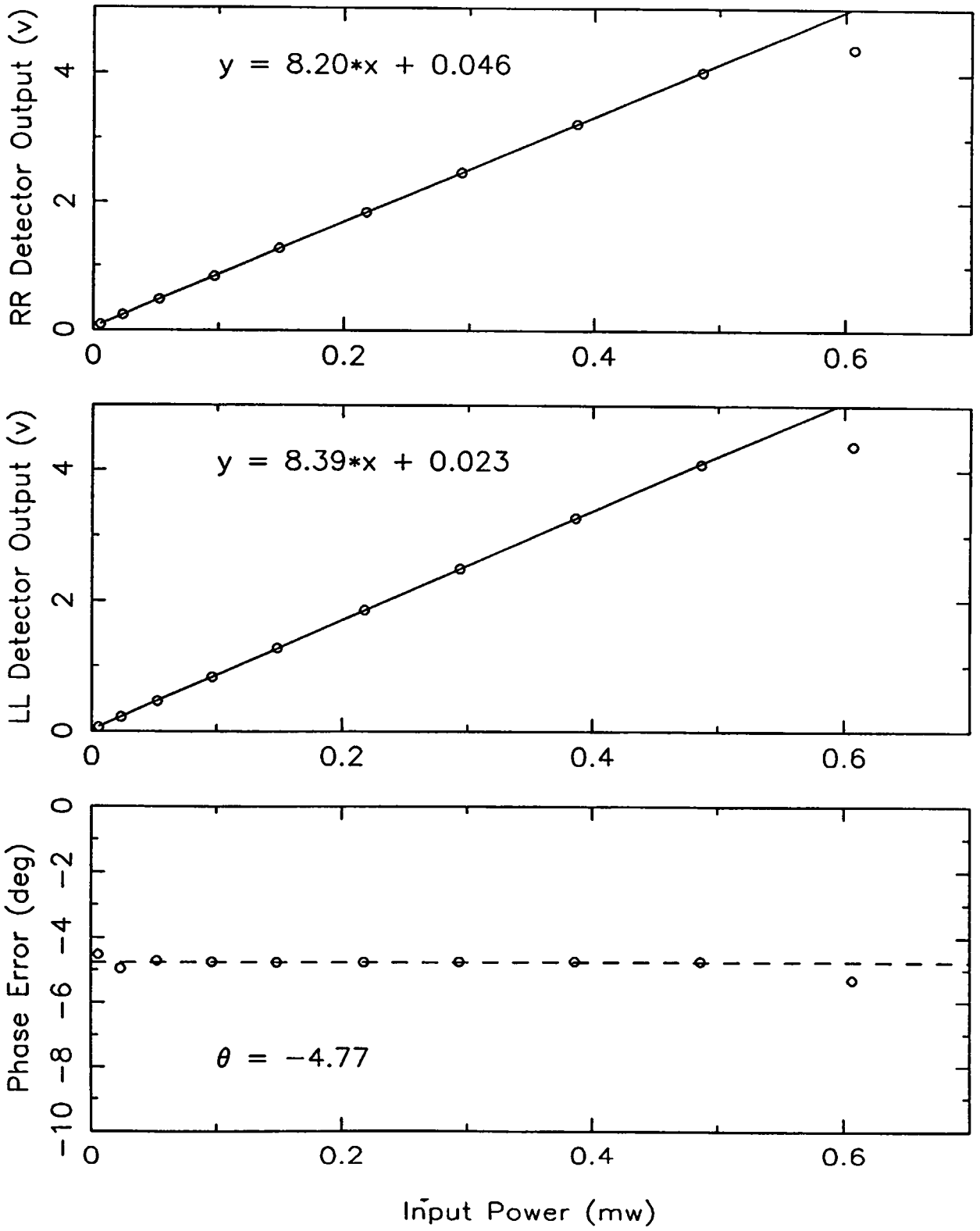
HTRP Detector Set 4 Performance



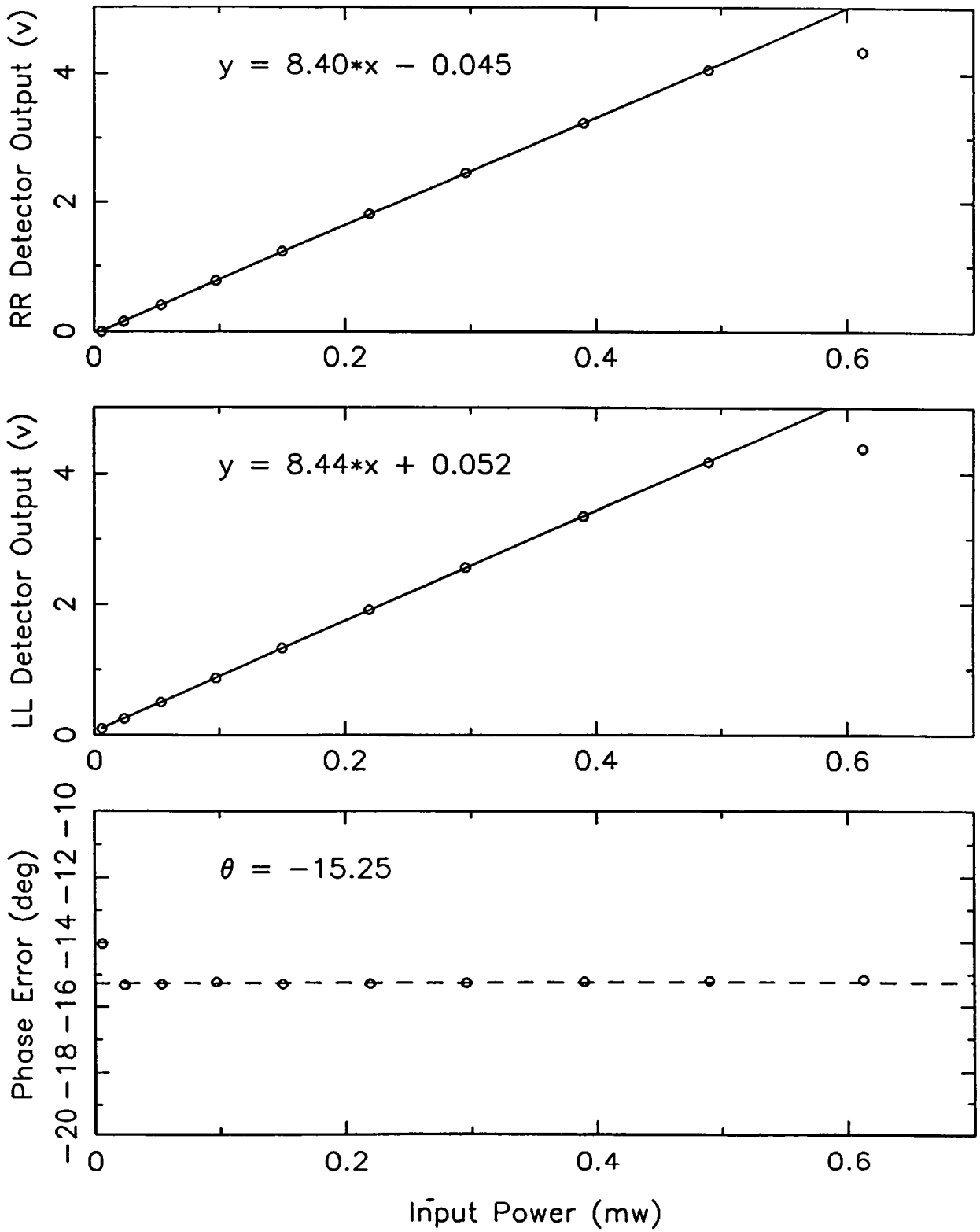
HTRP Detector Set 5 Performance



HTRP Detector Set 6 Performance



HTRP Detector Set 7 Performance



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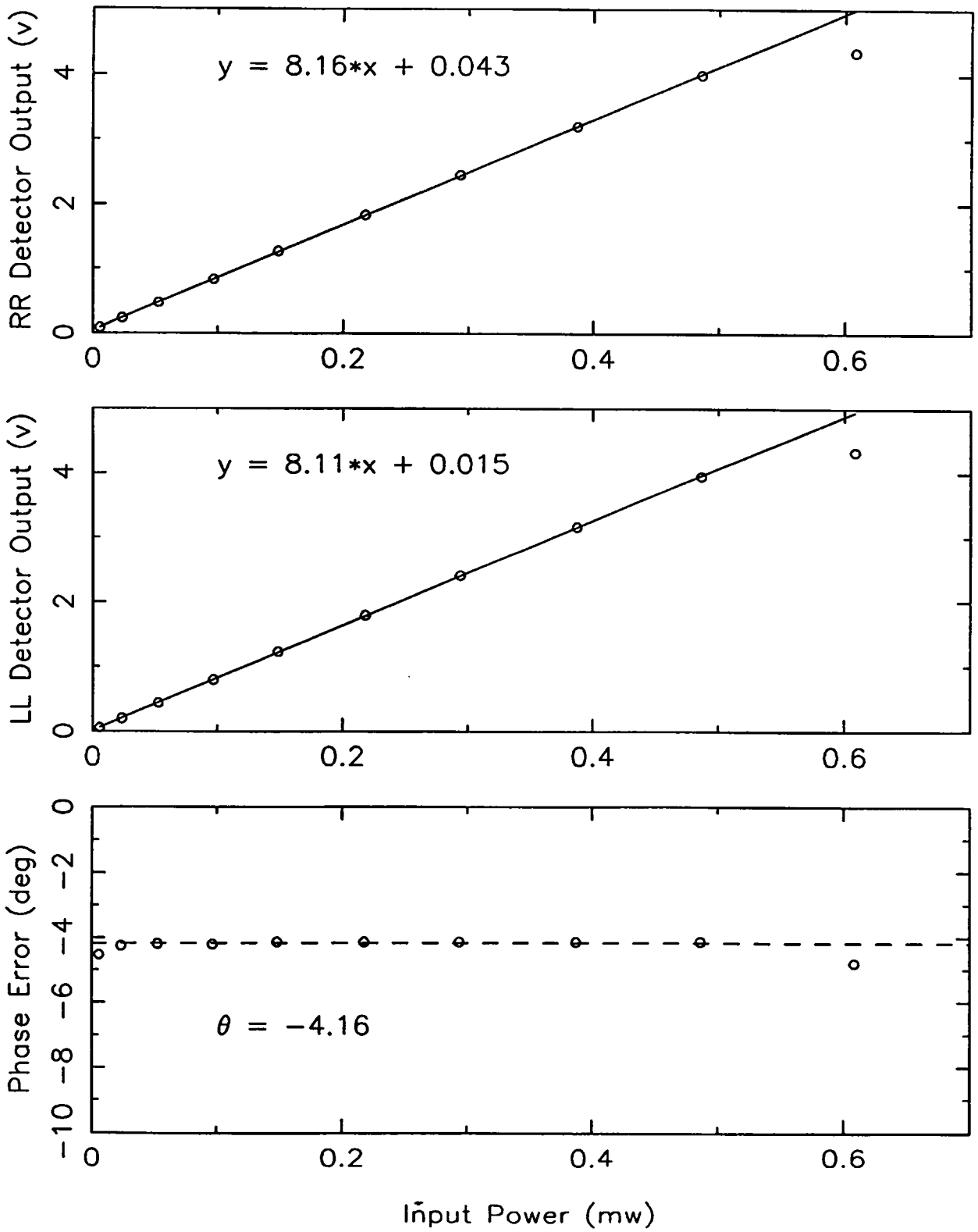

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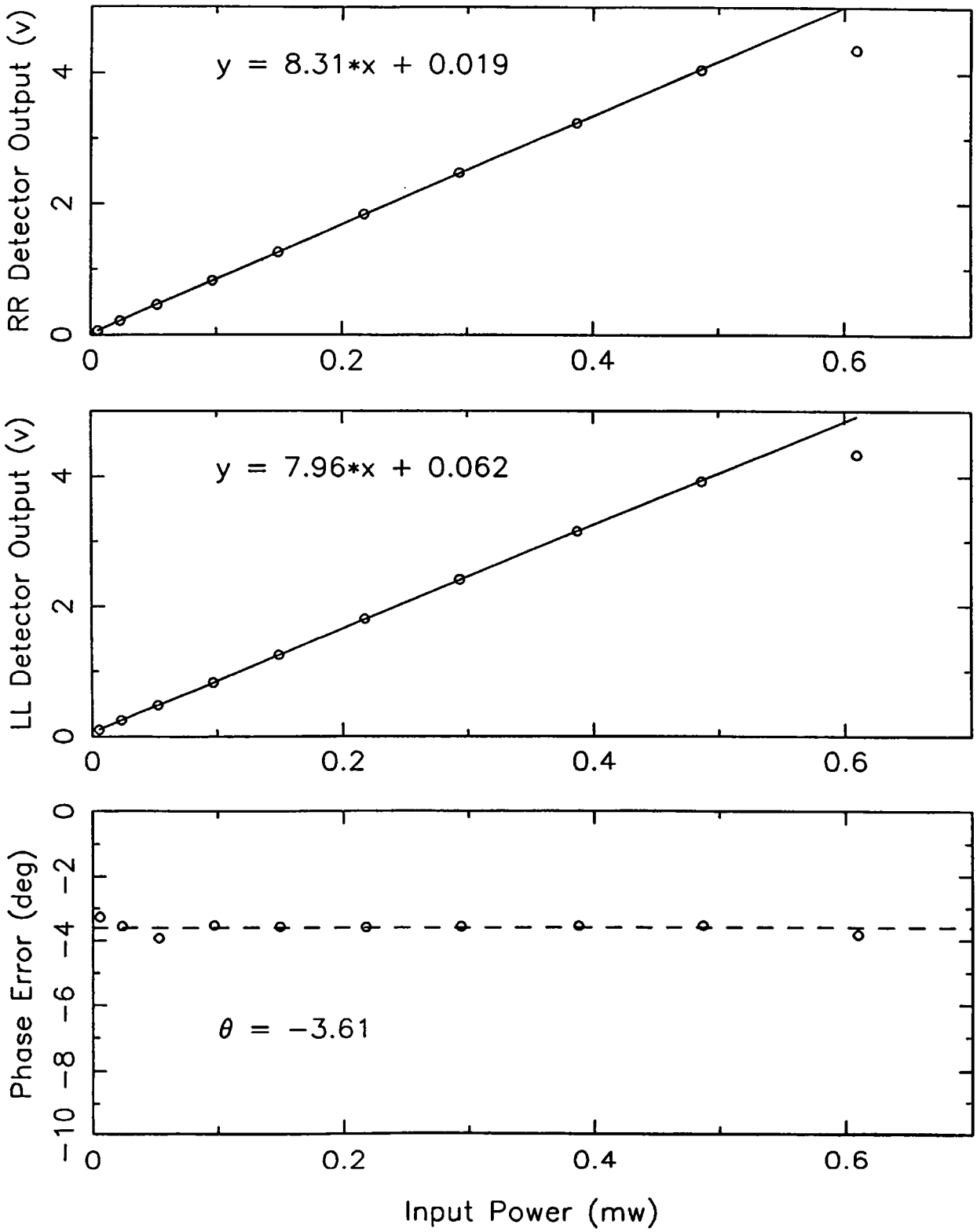

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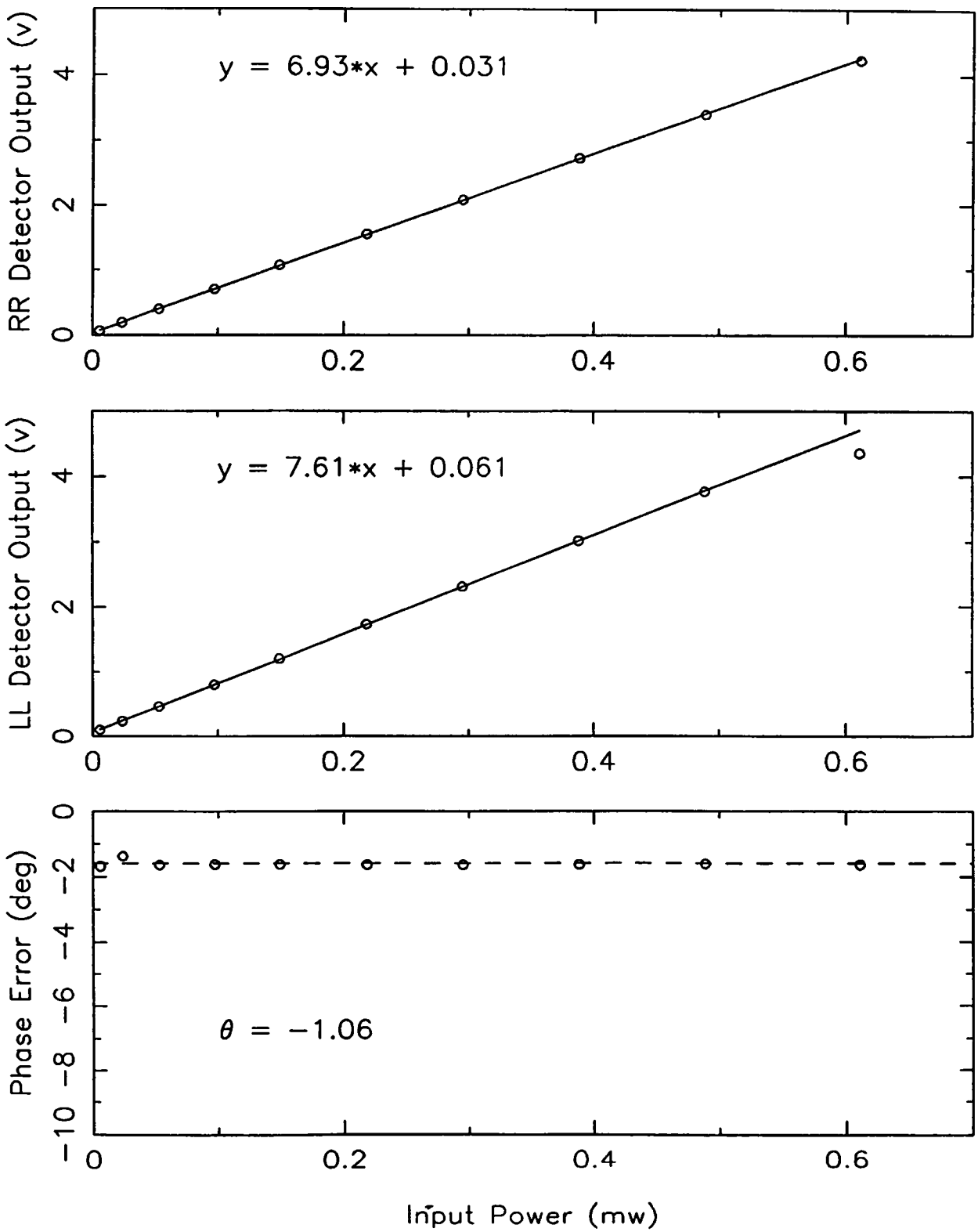
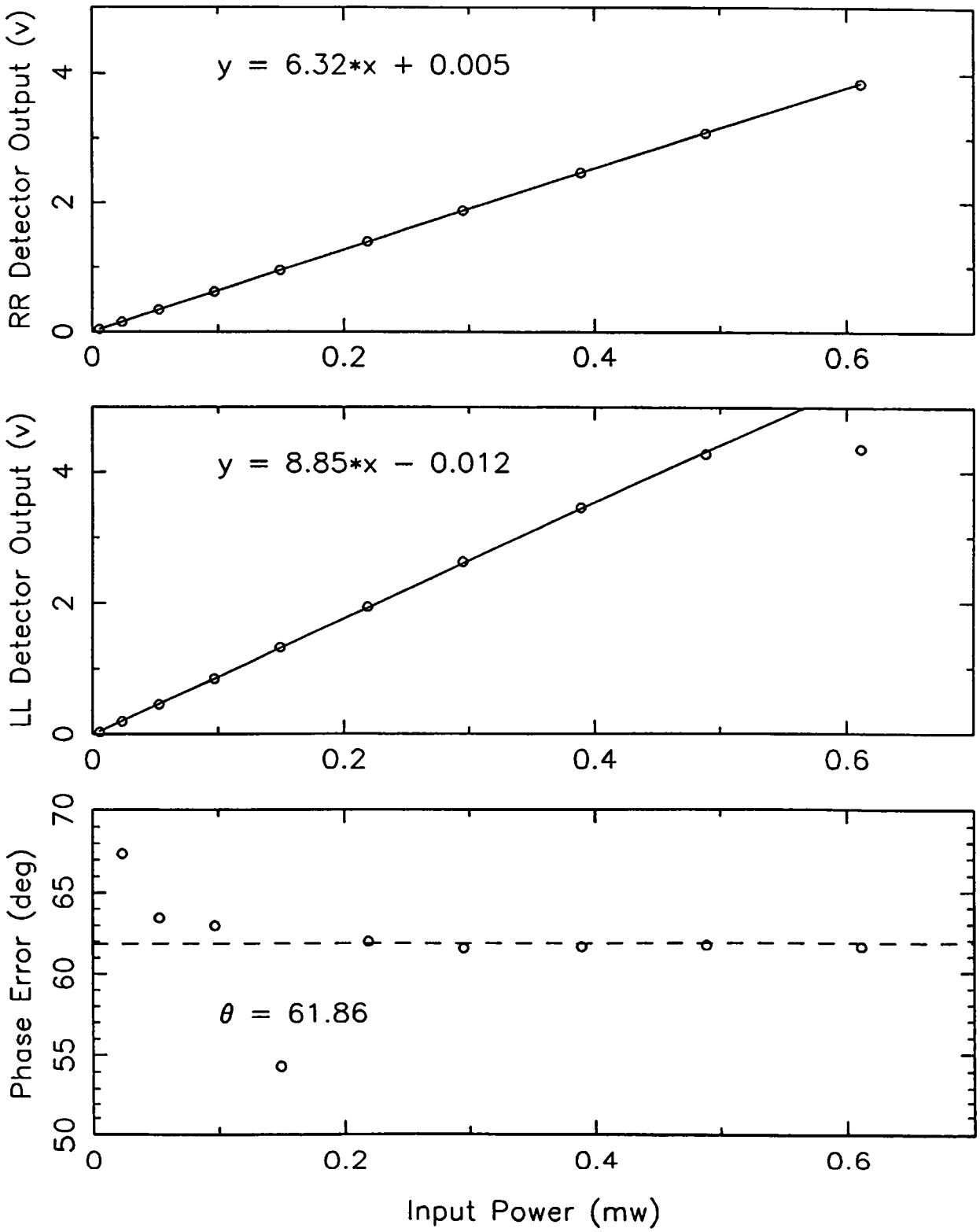
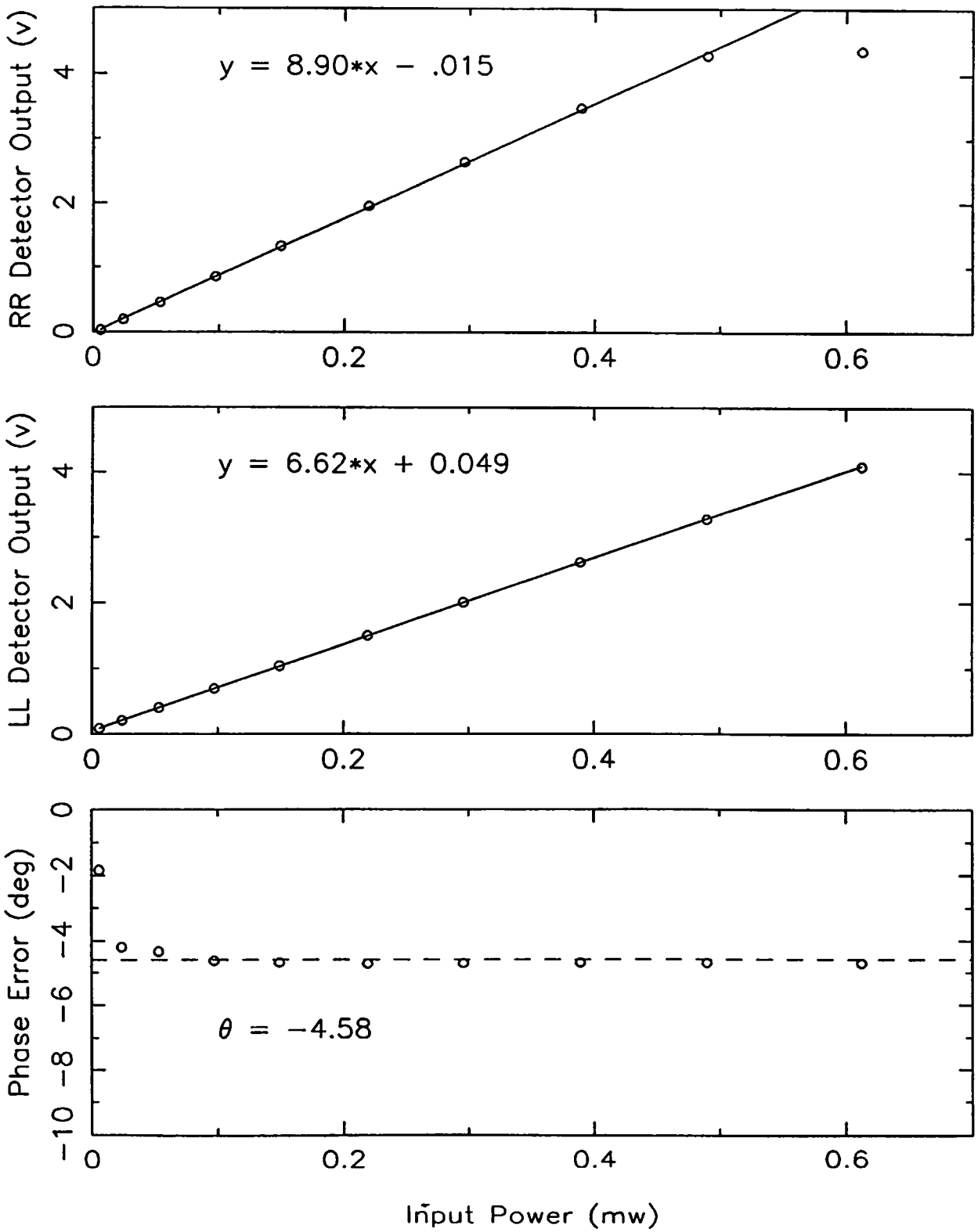


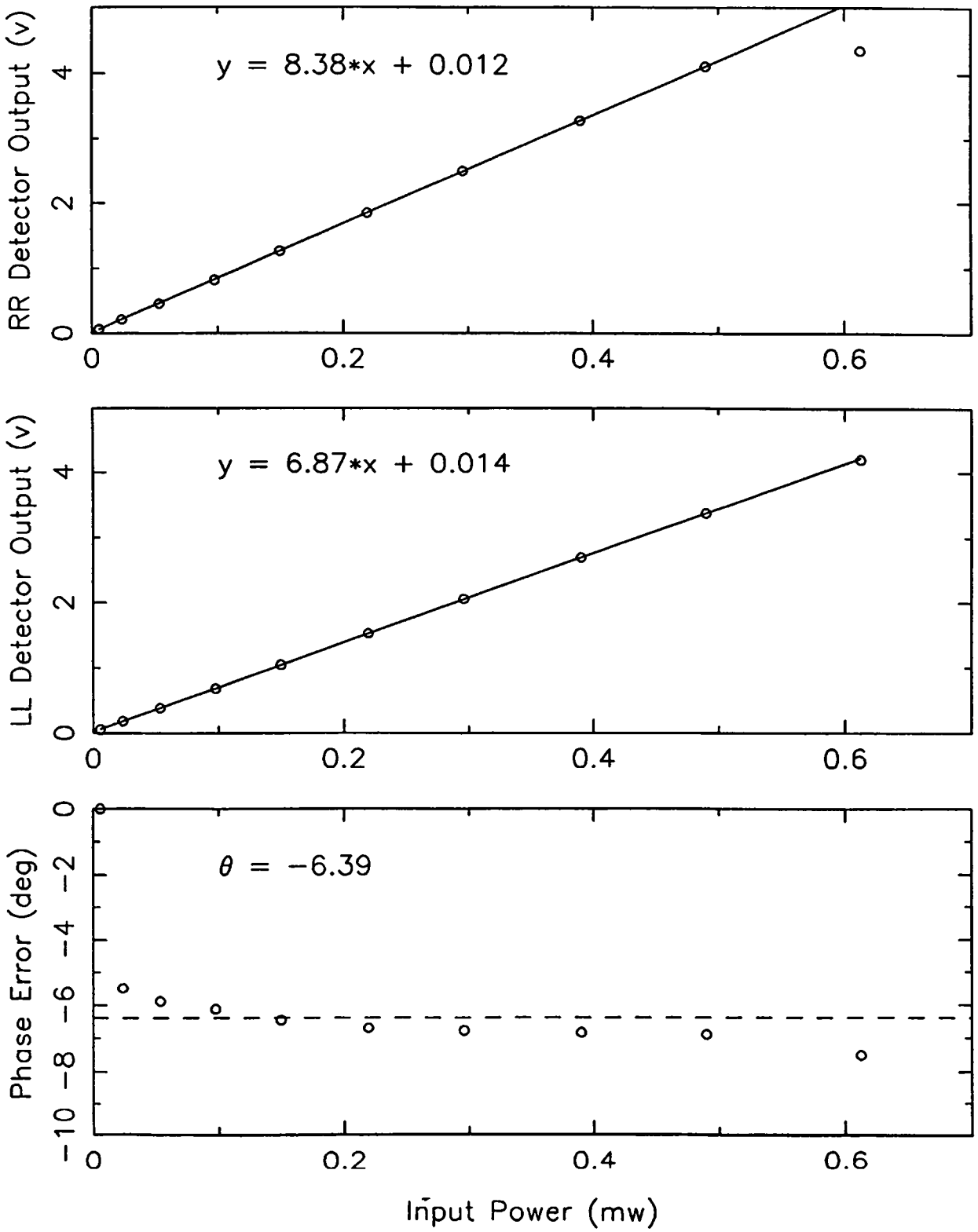
HTRP Detector Set 11 Performance



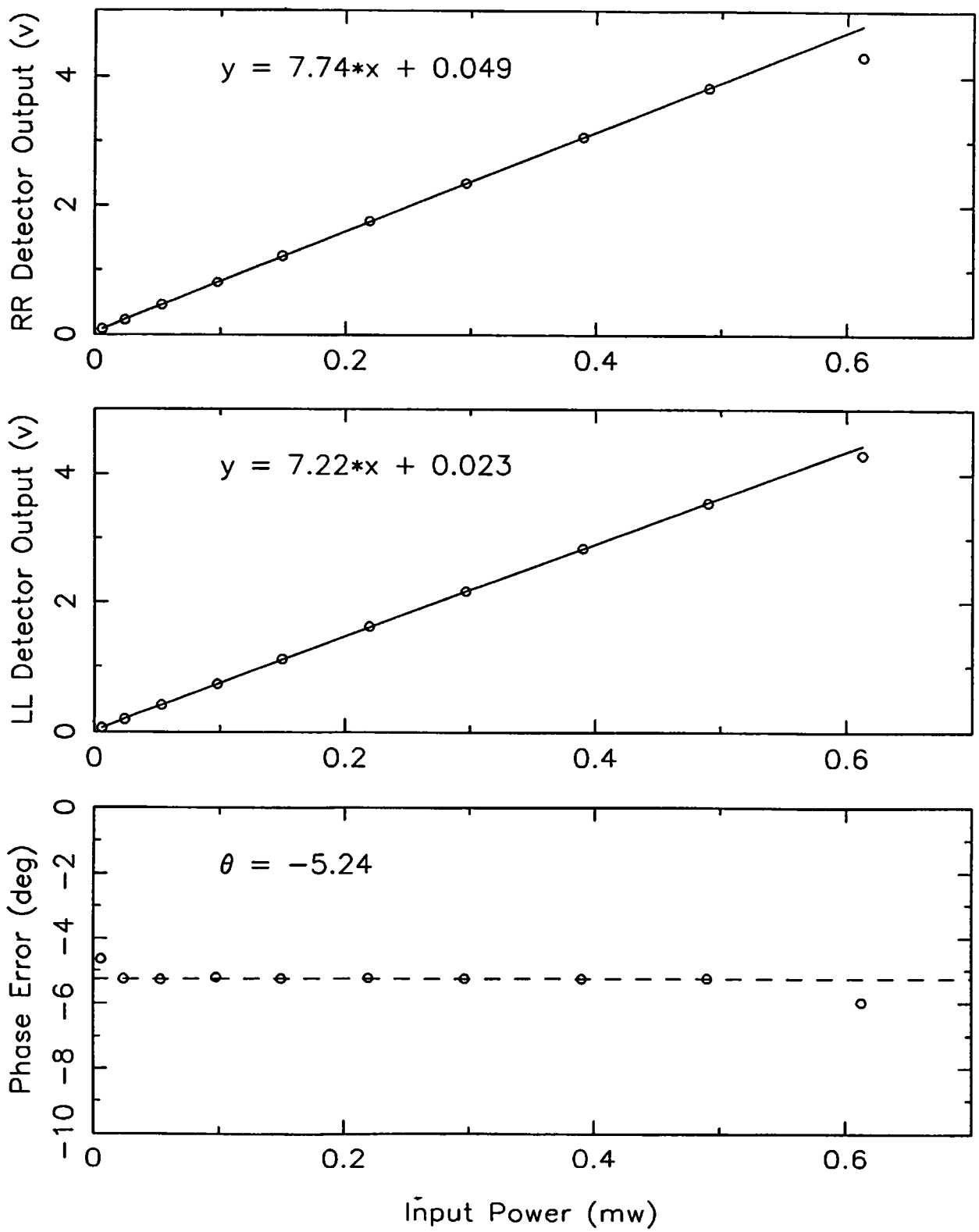
HTRP Detector Set 12 Performance



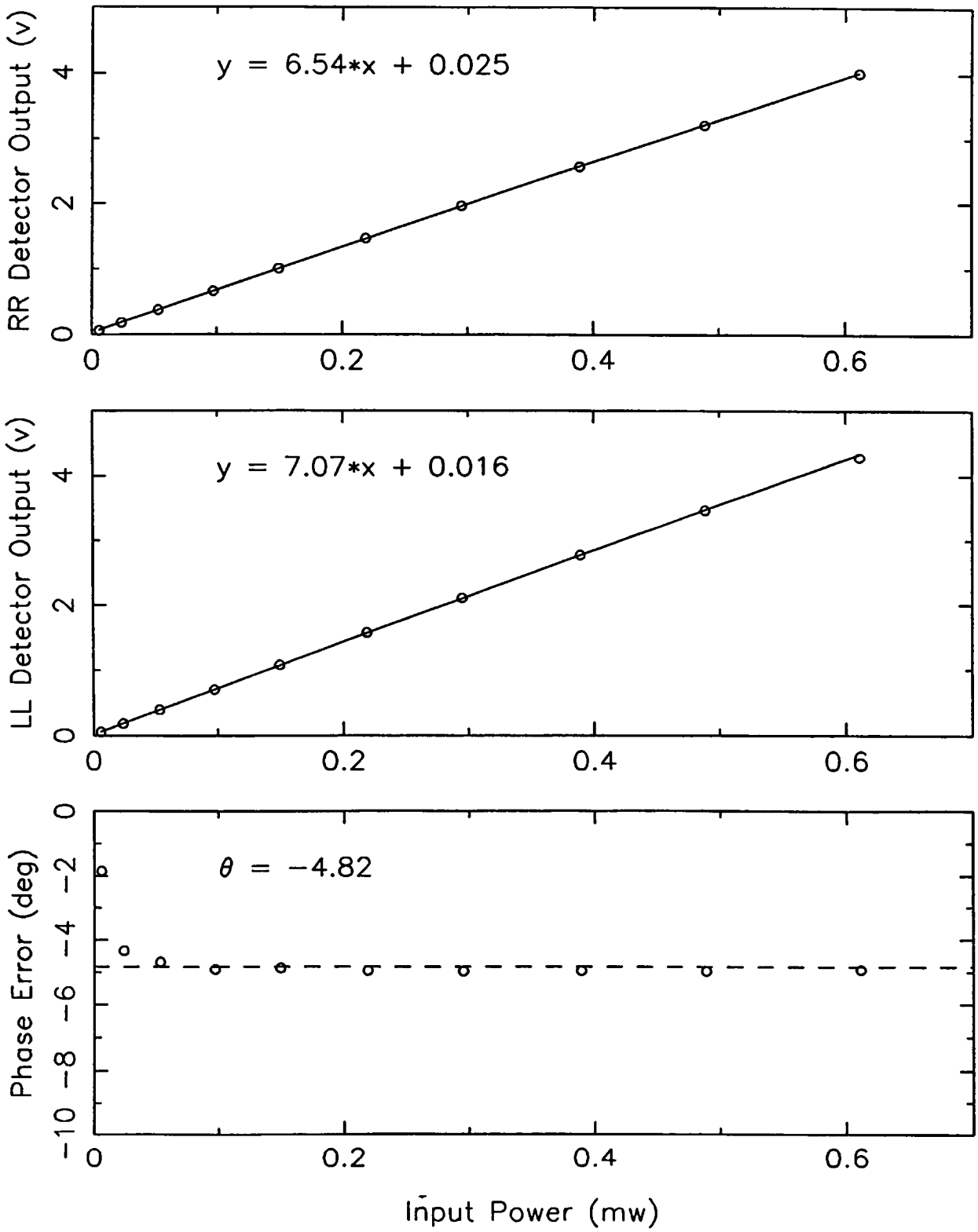
HTRP Detector Set 13 Performance



HTRP Detector Set 14 Performance



HTRP Detector Set 15 Performance



HTRP Detector Set 16 Performance