Gated Sampling of the HTRP

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I. Introduction.

Gating of High Time Resolution Processor (HTRP) data sampling was developed for observations of pulsed emission from pulsars. If an observer is only interested in the pulsed emission, there is no need to sample the off-pulse noise. The gating of data sampling reduces the required capacity of computer disk and/or magnetic tape by about 90 percent of that required by continuous sampling because the duration (duty cycle) of a pulsar pulse is typically less than 10 percent of the pulsar's period. Subsequently, the amount of time invested in both the development of data analysis software and the actual analysis of the data is greatly reduced. In this memorandum I discuss how the Advanced Micro Devices (AMD) 9513A System Timing Controller is used to produce gated sampling of HTRP data. The AMD 9513A is part of the LabMaster DMA 100, which performs the actual analog-to-digital (A/D) conversion of HTRP data.

II. Gating Process Description.

The process of gated sampling is not as simple as performing A/D conversions during a gate. The AMD 9513A must conduct counting operations required by the HTRP data acquisition computer for the proper handling of sampled data. Given a frequency reference and an external pulsar timing gate, the AMD 9513A must meet the following requirements.

1. Determine the desired A/D conversion rate from the frequency reference.
2. Produce a gate synchronous with the external pulsar timing signal. The gate width must be an integer multiple of the number of samples taken across the pulsar pulse.
3. Count the number of samples written to computer memory by direct memory access (DMA) so the data acquisition computer can be instructed to write data to disk.
4. Notify the computer when one of the data buffers, located in computer memory, is full so that data buffers can be switched. (Data is written to computer disk from one buffer while sampled data is written into the other buffer, i.e. the number of samples in a write-to-disk operation is the same as the number of samples in a data buffer.)
5. Trigger the HTRP track-and-hold (T-H) circuitry. The T-H circuitry insures that samples of every HTRP channel represent the same instant in time.

The five 16-bit counters of the AMD 9513A are configured in accordance with Figure 1 to satisfy the above requirements. Counter number 5 uses the frequency reference to determine the data sampling rate. The output of counter 5 is the external start-of-conversion (ESOC) signal required by the LabMaster A/D circuit. Counter 5 is level-gated by the output of counter 1, which determines the integer number of samples across the pulsar pulse from the frequency reference. The counting process of counter 1 is edge-triggered by the external pulsar timing signal. The particular operating mode of counter 1 does

not allow for repeated operation; therefore, it must be rearmed by counter 2 when the sampling across the pulsar pulse is completed. Counter 2 does this by simply counting the falling edge of the gate to counter 5. The LabMaster A/D circuit produces an End A/D signal which is used by counter 3 to determine the number of data samples written to computer memory by the LabMaster. The output of counter 3 notifies the computer when to switch data buffers and write data to disk. The End A/D signal is also used by counter 4 to drive the HTRP T-H circuit. The output of counter 4 depends upon the number of HTRP channels sampled.

The data acquisition computer operating system indirectly constrains the number of samples collected each pulsar period. The computer operating system limits the size of each data buffer to 16,384 samples because an MS-DOS memory segment is 64 kilobytes and each sample occupies two bytes. Therefore, to insure that the buffer change and disk write occur when data is not being sampled, the number of samples collected each pulsar period must be a power of two and less than or equal to 16,384. The number of samples of each LabMaster (HTRP) channel per pulsar pulse is then limited to 256 because there are 64 LabMaster channels. Considering the maximum sampling rate (100kHz) of the LabMaster, I have found that 64 samples of a single HTRP channel are adequate for typical pulsar duty cycles. If one collects 64 samples of 64 channels each pulsar period, a disk write will occur every four periods.

The counter configuration in Figure 1 imposes certain limitations upon sampling rates and gate durations. The limitations are summarized in Tables 1a and 1b for reference frequencies of 1MHz and 100kHz, respectively. The tables assume all 64 channels are sampled. The ESOC frequency is the reference frequency divided by the counter 5 divisor. Since 64 channels are sampled, the time interval between samples of a channel is 64 times the ESOC period. As shown in Table 1a, the fastest sampling interval of an HTRP channel is 0.64 milliseconds. The sampling interval is also the period of the counter 4 output to the HTRP T-H. The gate durations in the tables assume 64 samples of a single channel; therefore, the gate durations are 64 times the sampling interval. The maximum channel samples listed in the tables are generally limited by the maximum range of counter 1. All 9513A counters can count to any value between 0 and 65,535 because they are 16-bit counters. The maximum number of channel samples is $N_{max} = 65,535/N_c/D_5$, where N_c is the number of channels sampled and D_5 is the counter 5 divisor. Again, the table entries assume $N_c = 64$. An additional constraint on the maximum channel samples is the data buffer size as cited above. The majority of entries in Table 1b are limited by this constraint.

For a pulsar observation the gate durations should be selected based upon the actual pulsar pulse width and the desired sampling resolution across the pulse. One should properly account for dispersion smearing in calculating the gate duration to insure that all HTRP frequency channels are adequately sampled during the gate. The desired pulse sampling resolution ultimately restricts the application of this gating system to observations of relatively slow pulsars. If an observer desires sampling resolution equivalent to 512 samples across the entire pulsar period, the fastest pulsar which could be sampled with the LabMaster DMA 100 would have a period of $0.64 \times 10^{-3} \times 512 = 0.328$seconds. The gating system could be used with a faster A/D converter to improve sampling resolution

of faster period pulsars. The only restriction imposed by the 9513A counters is that they are not recommended for use with reference frequencies greater than 5MHz.

III. Individual Counter Configurations.

The five counters in the AMD 9513A System Timing Controller can produce complex waveforms using count values entered into the load and hold registers of each counter. This versatility of the 9513A is what allows one to produce complex timing systems such as gated sampling. Below I present a detailed summary of the operation of each counter used in the gated sampling scheme of Figure 1. The operating modes I refer to are also discussed in the AMD 9513A Handbook.

1. Counter 1 is configured as a hardware-triggered delayed pulse strobe (AMD 9513A Mode I). The counter counts low to high transitions of the frequency reference. Counter 1 does not begin counting until a gate edge is applied to the counter after it has been armed. The gate edge is provided by the external pulsar timing signal. The counter output, which is terminal count (TC) toggled, is a delayed strobe whose start time and duration are set by the values loaded into the counter's load and hold registers. The load register value determines the time delay between the gate edge and the strobe. The duration of the strobe is determined by the hold register value. The load register value is very small (1 or 2) because the counter output should be nearly synchronous with the pulsar timing signal (e.g. if the load value is 1 and the frequency reference is 1MHz, the time delay between the pulsar timing signal and the strobe is one microsecond). The hold register value is set by the product of the number of channels sampled, the number of samples per channel, and the counter 5 load register value (e.g. to take 64 samples of 64 channels at 100kHz with a 1MHz frequency reference, the counter hold register value should be 40,960). After generating the strobe, the counter disarms itself. Counter 1 is rearmed by software which monitors the status of the counter 2 output (see below). Counter 1 must be rearmed before subsequent pulsar timing signals will be recognized. The output of counter 1 provides the gate for counter 5.

2. Counter 2 is configured as a software-triggered strobe with no hardware gating (AMD 9513A Mode A). This counter simply changes its TC-toggled output from low to high when the output of counter 1 makes a high to low transition. A status bit is also set which notifies the data acquisition computer that all samples of the pulsar pulse have been collected. The computer then resets the output of counter 2 low, and rearms counters 1 and 2. Counter 2 will not resume counting until it is rearmed by this software-generated command, thus the name software-triggered strobe. Since counter 2 effectively counts each pulsar pulse, the value of 1 is entered into its load register.

3. Counter 3 is configured as a rate generator with no hardware gating (AMD 9513A Mode D). This counter counts the low to high transitions of the End A/D signal. The number of samples (16,384) to be written into a data buffer is entered into the counter 3 load register. Once armed, the counter will count to TC repeatedly. Upon TC, the counter automatically reloads itself from the load register. The counter 3 output is

configured for TC-toggled, and is originally set low. When the counter reaches TC, its output toggles high and a status bit is set to notify the data acquisition computer that the data buffer is full. The computer then resets the counter output to low.

4. Counter 4 is also configured as a rate generator with no hardware gating (AMD 9513A Mode D) which counts the low to high transitions of End A/D. The number of channels sampled, usually 64, is entered into the counter 4 load register. The output of counter 4 is a TC pulse. The pulse generated every 64 samples by counter 4 is used by the HTRP T-H circuit. Counter 4 counts repetitively with no computer interaction.

5. Counter 5 is configured as a rate generator with level gating (AMD 9513A Mode E). In this mode, counter 5 acts as a gated frequency generator. It only counts its frequency source, the low to high transitions of the frequency reference, when its gate is active (high). The counter 5 gate is the output of counter 1. The value entered into the counter 5 load register is the source frequency divider. For example, a load register value of 10 is required to produce a 100kHz output from a 1MHz source. The gated counting of counter 5 proceeds on a continuous basis with no direct computer interaction by automatically reloading the load register value.

IV. Reference.

Advanced Micro Devices 9513A Handbook.

AMD9513 Counter Configuration for Gated HTRP Sampling

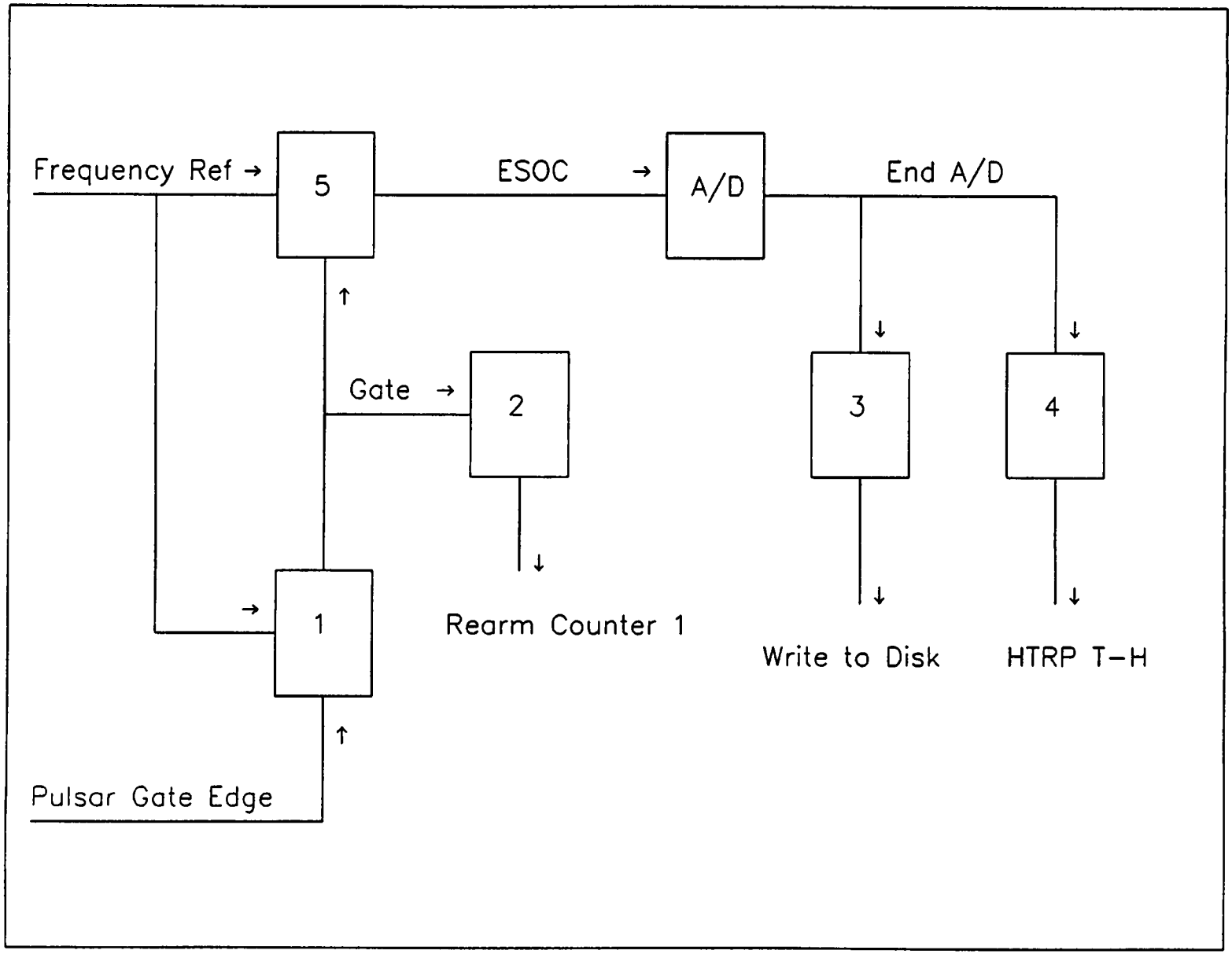

Table 1a: Properties of Gated Sampling with a 1MHz Frequency Reference

Counter 5 Divisor	ESOC Period (usec)	Sampling Interval (msec)	Gate Duration (msec)	Max Channel Samples
10	10	0.64	41.0	102
11	11	0.70	45.1	93
12	12	0.77	49.2	85
13	13	0.83	53.2	78
14	14	0.90	57.3	73
15	15	0.96	61.4	68
16	16	1.02	65.5	63

Table 1b: Properties of Gated Sampling with a 100kHz Frequency Reference

Counter 5 Divisor	ESOC Period (usec)	Sampling Interval (msec)	Gate Duration (msec)	Max Channel Samples
1	10	0.64	41.0	256
2	20	1.28	81.9	256
3	30	1.92	122.9	256
4	40	2.56	163.8	255
5	50	3.20	204.8	204
6	60	3.84	245.8	170
7	70	4.48	286.7	146