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| VLBA CORRELATOR MEMORANDUM NO. 007 |
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To: VLBA Correlator Group Date: 8 Dec 1983

From: Martin S. Ewing

Subject: Minutes of Local Group Meeting, 12/07/83

Present: Pearson, Peterson, Dillon, Vavrus, Seling, Whitney, Rayhrer, Ewing.

We opened with the observation that we must be making progress since there is an agenda for this meeting.

VLSI REPORT

John Peterson gave us his update on the VLSI work. He has completed the design and layout for a chip containing one "computational element" which will leave JPL next week. He expects samples to be delivered in 6-8 weeks. (The computational element consists of the logic to handle 2- or 4-level multiplications and prescaling for a single "complex" lag. - MSE)

John plans to lay out a 4- to 8-lag version next, before moving to a full test of a 16-lag (dual 8-lag) chip. He is looking into the possibility of including 18 elements on a chip so that we can hope to improve yield by reconfiguring each chip at wafer test time. Even if this were not needed for the VLBA project, it is of considerable interest for the JPL VLSI program.

There may be a possibility of having up to 10 or 20,000 chips fabricated and tested <u>for free</u> if we are able to meet some simple pad layout conditions. This would be part of a larger program to develop IC production and test capabilities at the Lab. We expressed considerable interest in this possibility if it is compatible with the VLBA schedule.

CORRELATOR SPECIFICATIONS

Ewing reported conversations with Larry D'Addario, who is looking at system interfaces and specifications. A persistent issue is the "channelization" of the IF, data recording, and correlator systems. Really there are two problems. First, why choose 16 Mb/s as the standard channel rate? This number seemed to be reasonably compatible with (1) the capabilities of a tape recorder track, (2) the clock rate of an

n-MOS VLSI chip, and (3) previous VLBI practice. Ewing pointed out that 16 Mb/s was only thought of (by the Rogers/Clark/Ewing committee - see VLBA Memo 196) as a nominal figure; it might actually be as low as 12 or as high as 20 Mb/s.

D'Addario suggested 12.5 Mb/s, as a submultiple of 100 MHz and compatible with VLA needs. A few VLBA antennas may have to be interoperable with the VLA. The same IF system may have to serve for VLA and VLBA simultaneously. Mark III compatibility would have to be provided by making 4 and 8 Mb/s clock rates available as special cases.

Whitney pointed out that VLA effective bandpasses are considerably below 50 MHz, so a precise match is not needed for VLBI use of VLA elements. The antennas that need to be matched to VLA requirements are so few that they seem to be a very weak driver for configuring the whole VLBA.

Peterson pointed out that his VLSI design is aimed at 16 MHz and has a "guaranteed maximum" of 20 MHz. Running at 12 would be very conservative, but if we are really aiming at a lower rate, especially below 10 MHz, we might well have chosen a CMOS chip. This would have system advantages, primarily saving power. His n-MOS design cannot easily be converted to CMOS, since PLA layout tools are not now available for CMOS.

The feeling around the table was that from a system viewpoint, 16 Mb/s was still a "good" goal. Although still having some compatibility with 4 and 8 Mb/s, 12 Mb/s was thought to be "bad." (This, however, may be the preferred choice for the data recorders.) Sorry, Larry, but 12.5 Mb/s was rated "particularly bad." Strictly from a correlator viewpoint, of course, 12 and 12.5 are practically the same; both are easier than 16, but seem to make less efficient use of the IC technology.

A second issue, more important to the correlator, is whether "broadband" channels (sample rates > VLSI clock rate) are needed. This seems to boil down to a question of whether multiple 8 MHz IF channels can provide as good data a single 16 or 32 MHz channels. Ewing has been canvassing and has not been able to find any significant constituency for the broad channels. In some cases they might be more <u>convenient</u> than the 8 MHz channels and save some post-processing computing, but they do not seem necessary. The broad channels might facilitate interoperation with the VLA, but this is unclear.

There are substantial reasons why the correlator should not be required to support broad single channels. The "computational" capability is present with the 16 MHz VLSI to support up to 64 Mb/s streams; there are enough lags provided for spectroscopy to permit bandwidth quadrupling. But the problems of data switching, time skews, etc. are known to be thorny; although they may not increase the hardware costs greatly, they promise to complicate the design and increase the risk of the project.

FORMATTING

Because of Alan Whitney's visit and D'Addario's suggestion, we reconsidered the issue of data formatting. Is it appropriate for the correlator to accept "Mark III" formatted data streams? There was considerable feeling that, although Mark III format may be a good choice for a specific recording system, that it is too technology-dependent to foist on the correlator proper. See VLBA Memo 142. (A video disk system, for example, might have no need for the parity bits.)

The Data Playback System (DPS) - correlator interface was discussed at some length; a blackboard diagram showed the DPS on the left, and the correlator on the right. The information needed on the right consists of

1. Data Stream
2. Data Clock
3. Data Sync (time tag)
4. Data Validity (should this data be correlated?)

This information is needed in "real time." Of course, other information including station identification, tape quality, logging data, etc. is needed at later stages, but does not have to be passed at high speed. Mark III provides all the required information, but also a lot of "non-real time" data too.

What input does the DPS need from the correlator control computer? There will have to be "housekeeping:" mount tapes, rewind tapes, start and stop, etc. But during operation, the key command to the DPS is "shift data stream by +/- N bits." Rayhrer suggests "retard data stream by N bits." Whitney says no problem, but you will get "advance" too.

We further discussed the question of synchronous vs. asynchronous systems. Asynchronous systems force the use of self-clocking codes or separate clock lines; they also have considerable potential for mutual interference between signals -- occasionally a lot of little crosstalk pulses will add up to a giant one. The present Mark III/ Block II correlators accept "very asynchronous" streams from tape -- all the deskewing (track-to-track and recorder-to-recorder) is done in the correlator. The majority view was that this is a recorder-dependent situation and that it might be better to place all deskewing in the DPS, with a synchronous transfer from the DPS to the correlator.

Should data be recorded transparently, or should Mark III-style data replacement be allowed for housekeeping and synchronizing information? Whitney reported that Haystack people still felt that the cost and complexity of transparent recording was excessive and that there had never been any ill effects of data replacement seen at Haystack. Rayhrer mentioned that JPL has had to provide transparent recording for the DSN telemetry arraying project and that it was reasonably simple. Rayhrer will publish some information on this as a correlator memo.

We would have gone on in this discussion, had not Whitney explained that Alan Rogers is developing a recording system specification that will be the answer to all our worries.

RELATIONS WITH THE CONCURRENT PROCESSOR

The JPL VLBI Systems group is contributing to the Caltech Concurrent Processor project, which is being led by the High Energy Physics group with DOE sponsorship. The aim of the project is to develop a 1024-node processor with 500 MFlop/sec capability. Already a moderate performance (6 x VAX-11/780) 64-node prototype is working. This machine is interesting for astronomy imaging problems, of course, but our interest here is in the hardware.

The CP "supernode" is expected to be a 32-bit microprocessor board with 1 MB memory and fast floating point and/or array processing capability, with the power of "several" VAXes. All this should be available at a marginal cost of $2 - $5K. Prototypes are expected by summer of 84, so that the node appears to be very suitable for the Fringe Processor role in the VLBA correlator. It also may prove to be the most economical processor for phase/delay computations.

FUTURE MEETINGS

Tues., Dec. 13, 10:30 PST - 112 E. Bridge

Teleconference "Global" correlator meeting

Weds., Dec. 21, 14:00 PST - 212 N. Mudd

Local Meeting

Mon - Tues, Jan 16 - 17 - NRAO

Overall VLBA Design Review

*Mon., Feb 13 (?) - Caltech

Review of Block II and Mark III Correlators
for VLBA project. (East-coast participation!)

*Tues. - Thurs., Feb 14 - 16 - Caltech

Various correlator working group meetings.

* Tentative