Interoffice Memorandum

CALIFORNIA INSTITUTE OF TECHNOLOGY

To: VLBA Correlator Memo Series   Date: 9 July 1984

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Subject: Current Status of JPL VLSI Project

    Enclosed is a series of documents which gives the status of
the JPL project. These include

    1.   GPS Specification Document (GPS-1 through GPS-3). This
memo gives a picture of the requirements set by a JPL group for a
VLSI correlator chip to support a small, portable receiver for
the Global Positioning Satellite system. The block diagram indi-
cated is only representative of the requirement;   the current
VLSI design differs in details.

    2.   VLBI Chip Characteristics (A-1 through A-4). This is
the current design target for the VLBI chip. It is to be imple-
mented through a PLA methodology. The PLA block connections are
shown on p. A-2; the blocks are defined on p. A-3. A floor plan
showing how 4 "complex" lags might be implemented is given on p.
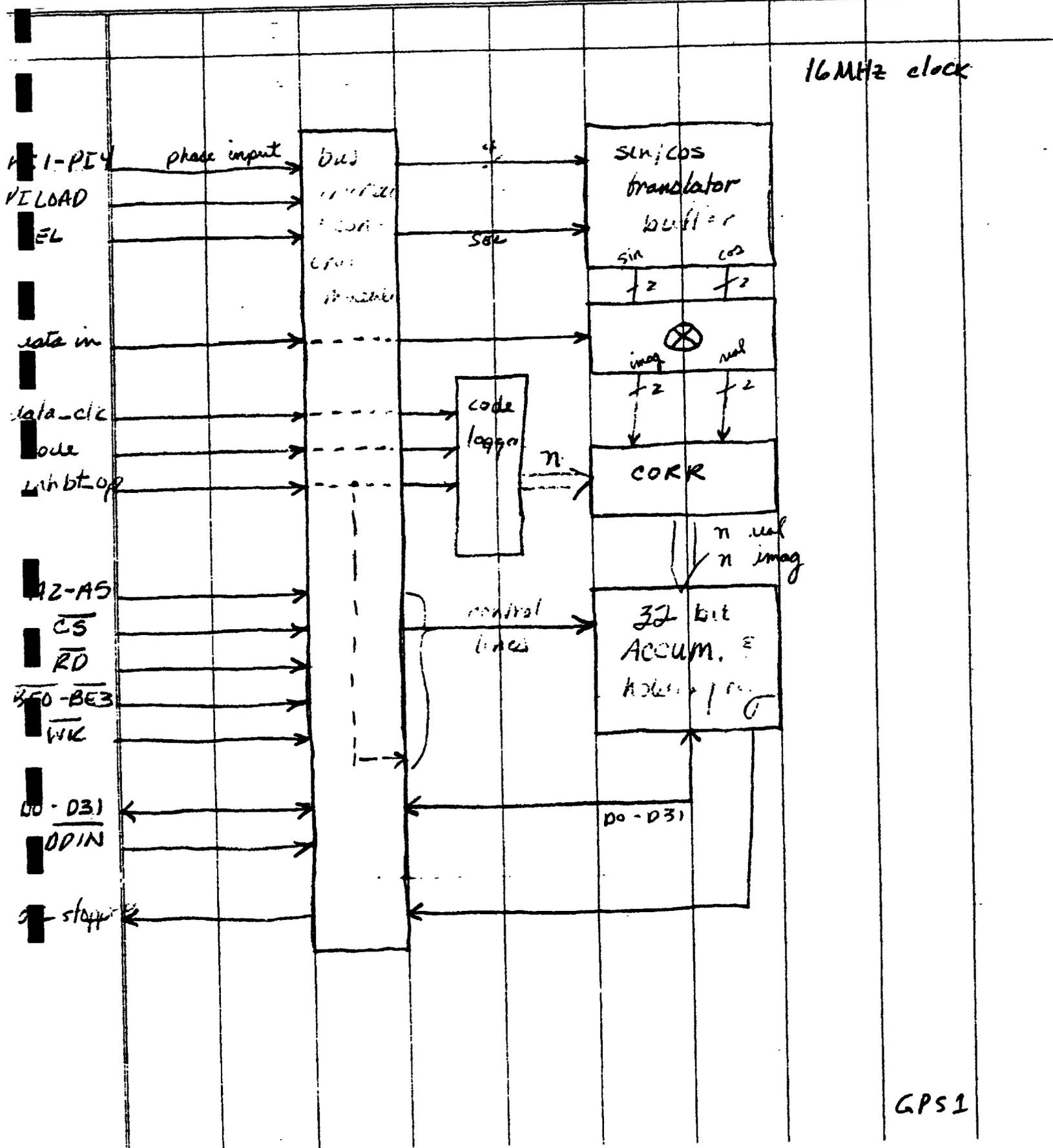A-4.

    3.   The PLA methodology is being tested via a "special
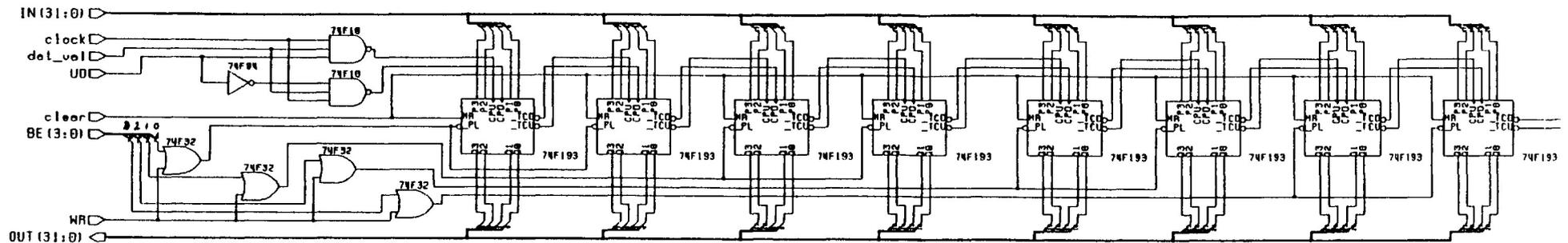project" chip described in B-1 and pictured on B-2.

    4.   Detailed layouts of 9 types of PLA cells are provided in
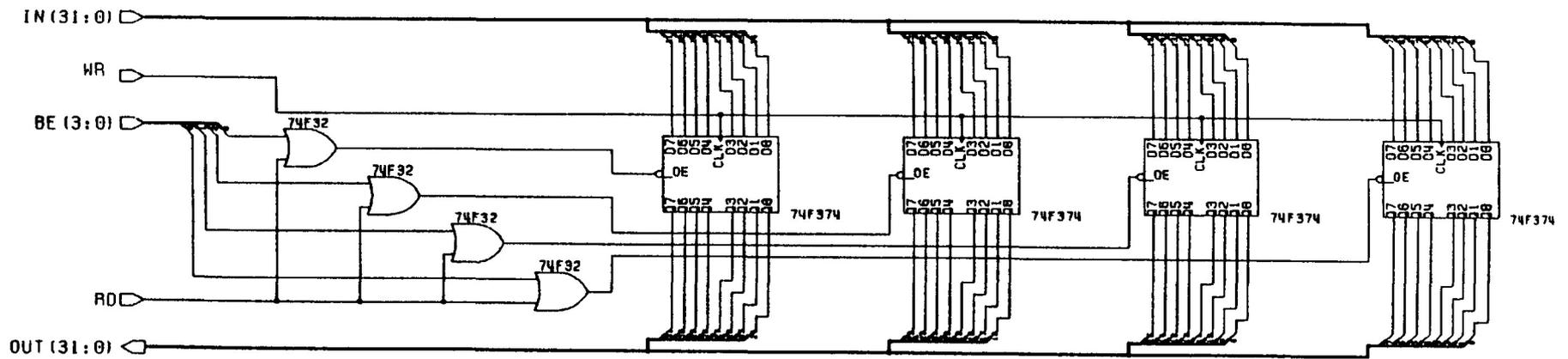an appendix. (Not supplied to memo series)

Block Diagram — GPS correlator

UCA / SHEET 1

J. Srinivasan

16 MHz clock

HS1-PL4 — phase input → bus interface decode / interface

PI LOAD

EL

sin/cos translator buffer

sel

| sin | cos |
| ÷2 | ÷2 |

data in

⊗

| imag | real |
| ÷2 | ÷2 |

data clk

code logic

clk

inhibit op

n → CORR

n real
n imag

A2-A5

CS

RD

BE0-BE3

WR

control lines →

32 bit Accum. Σ holding reg.

D0-D31

D0-D31

ODIN

S stop

GPS1

32 bit U/D counter (accum)

GPS 3

32 bit holding register

VLBI Cross-Correlator

CHIP CHARACTERISTICS:

* 2, 3, 4 - Level   4-Lag cross-correlator & integration

* 8 - 6bit up integration counters

* 8 - 6bit integration hold registers

* +1, 0, -1 bit delay (vernier) for data & bvalid

* 3 - level phase mixing for one data stream

* N-channel mos Technology

* 16 mhz data correlation bit-rate

* 40 pin Hermetic DiP Package

A - 1

1-Lag cross-correlator

A-2

DEFINITION OF CELLS

CX - cross-correlates two data streams A_{1-2} B_{1-2}. output L_{1-3} is product for 2-3-4 level input. S_2-selects mode 2-3 level or 4 level

R_c/R_s - takes output from L_1-L_3 and phase rotates it with R_{1-3}. Product P_{1-3} is output. R_c-is cosine cell R_s-is sine cell

Lag I/Lag D - Lag delay for data and invalid with oversampling of 1X, 2X, or 4X

Accu - output from multipliers P_{1-3} are pre-scaled for 8-clock time and the overflow C_o produces a complex data stream.
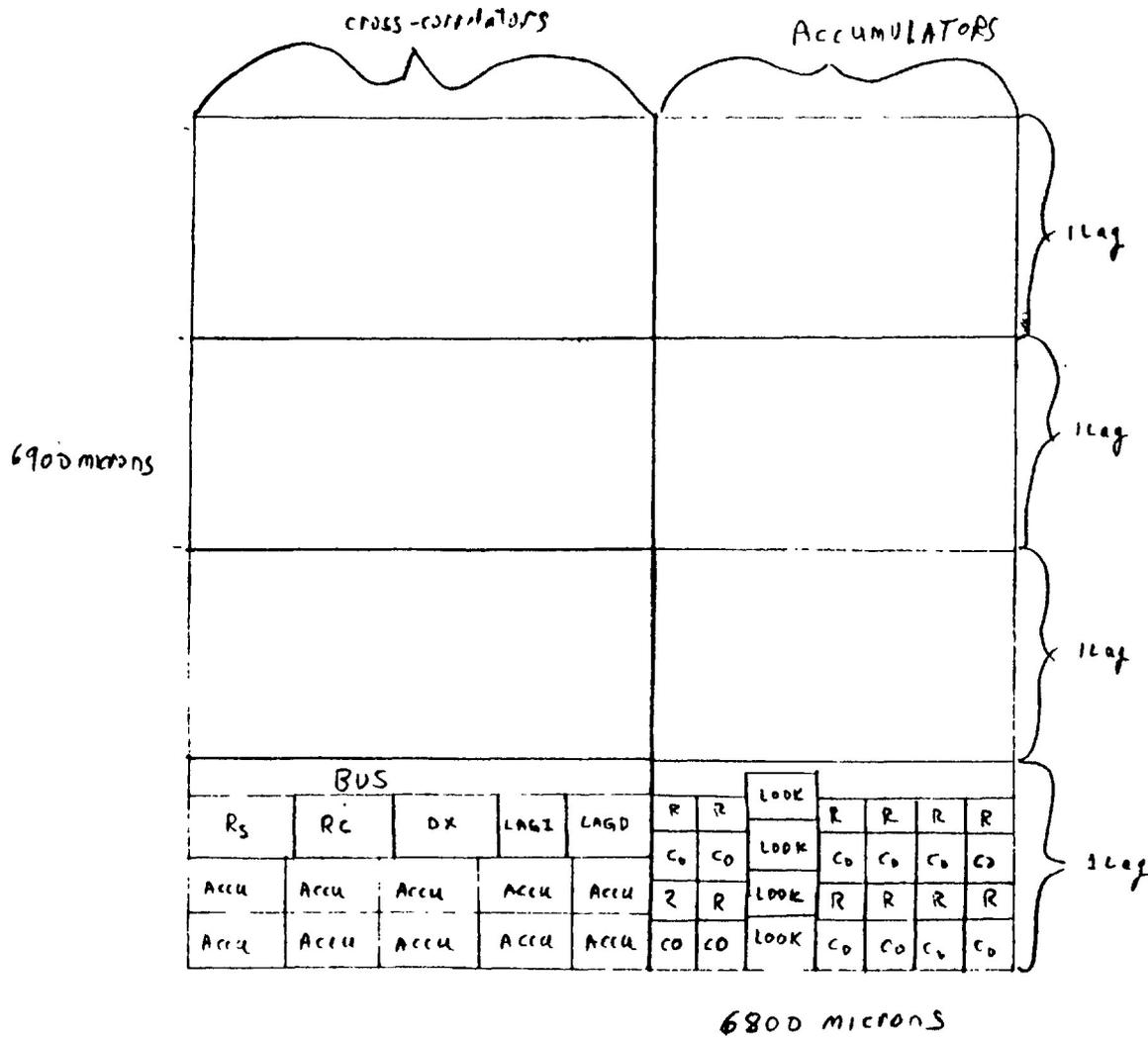
C_o - 6 bit up counter

LOOK - LOOK AHEAD FOR 6 BIT UP COUNTER

R - Holding reg. for 6 bit up counter

A-3

FLOOR PLAN OF VLBI
CROSS - CORRELATOR CHIP
40 PIN PACKAGE

4-Lag complex cross-
correlator

cross-correlators   ACCUMULATORS

6900 microns

1 Lag

1 Lag

1 Lag

1 Lag

BUS							LOOK				
R_s	R_c	DX	LAG1	LAGD	R	R		R	R	R	R
							LOOK				
					C_0	C_0		C_0	C_0	C_0	C_0
Accu	Accu	Accu	Accu	Accu	R	R	LOOK	R	R	R	R
Accu	Accu	Accu	Accu	Accu	CO	CO	LOOK	C_0	C_0	C_0	C_0

6800 microns

□ ← 100 μm , 20 μm

(PREPARED BY)	(DATE)	(REPORT NO.)
(CHECKED BY)	(DATE)	(PROJECT)

TITLE

This picture shows 16 DX cells and 10 Accu cells arranged in a test configuration. This was done to test the fabrication process for a dense but simple to design chip. This is the chip that is being refabricated because of a fabrication error.

B-1

VLSI FOR A VLBI PROCESSOR
JPL ACCOMPLISHMENTS SINCE JUNE 1983 (Cont'd)
CROSS-CORRELATOR SUBCIRCUIT