CALIFORNIA INSTITUTE OF TECHNOLOGY

MEMORANDUM

To: VLBA Correlator Memo List

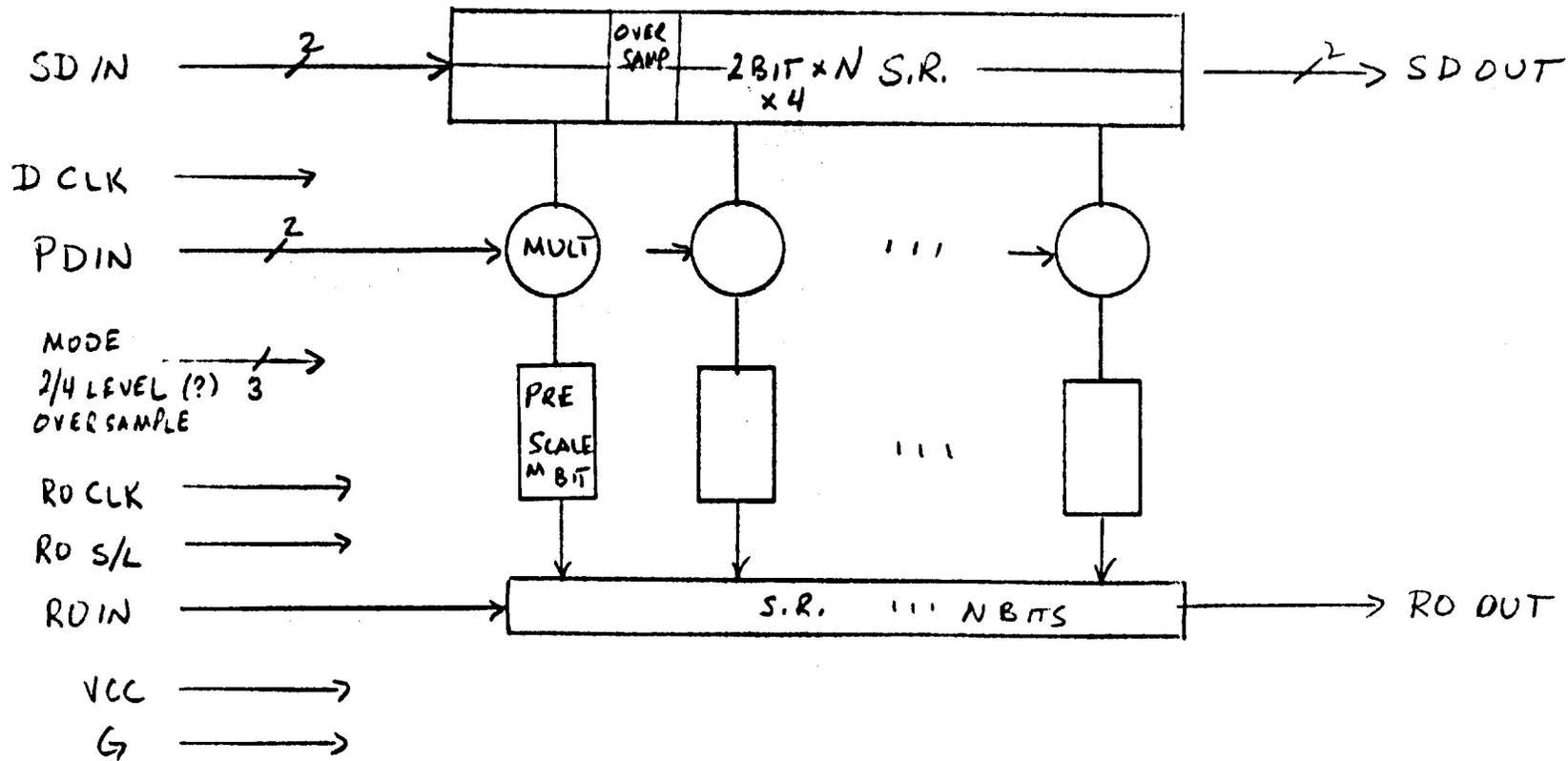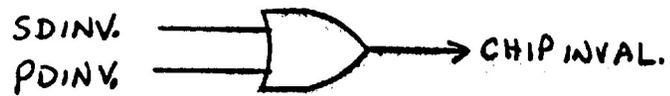From: Martin Ewing   Date: 20 July 1984

Subject: Alternative schemes for VLSI chip

Dave Fort and I have begun to look at various architectural schemes for a VLSI correlator chip with the objective of finding a good design for a possible gate array or custom cell implementation.

John Peterson's design (memo VC023) is also under consideration. The semi-custom approach he is taking has somewhat different design constraints than the commercial options we are looking into. Therefore, an optimal design approach for a gate array or custom cell may look rather different from the diagram he presented.

We will need to do a cost/benefit tradeoff at the system level for all these approaches. Factors to consider include number of chips per system, cost per chip, package size, power consumption, clock rate, design cost, total system hardware cost and size, etc.

Any number can play this game, and I encourage everyone to submit his pet correlator architecture. I begin with two variations attached herewith.
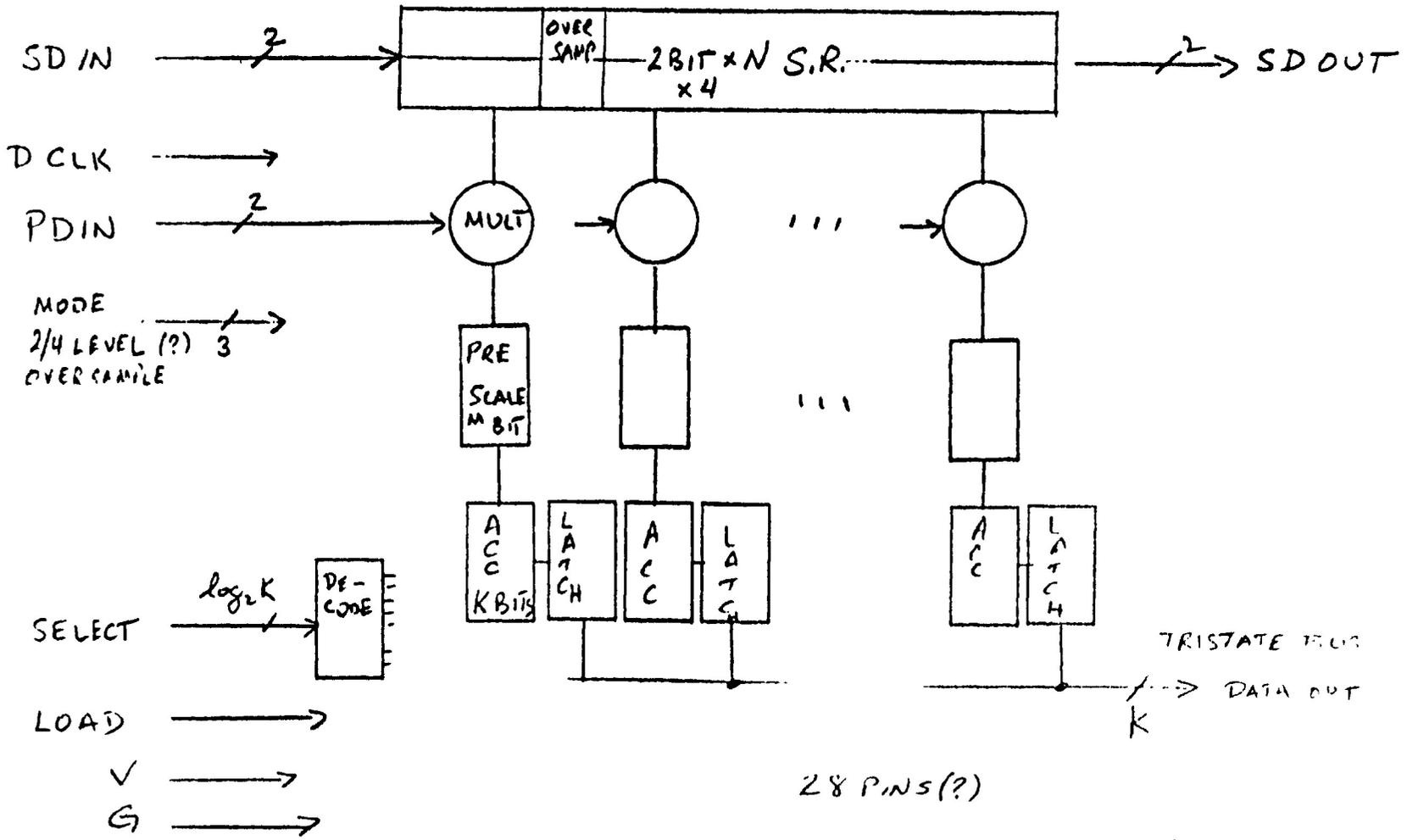
SDINV.
PDINV. ⟶ CHIP INVAL.

SD IN ⟶ 2

| | OVER SAMP | 2 BIT × N S.R. × 4 |

⟶ 2 ⟶ SD OUT

D CLK ⟶

PDIN ⟶ 2 ⟶ MULT ◯ ' ' ' ◯

MODE
2/4 LEVEL (?) 3
OVER SAMPLE

PRE SCALE M BIT

RO CLK ⟶

RO S/L ⟶

RO IN ⟶ S.R. ' ' ' N BITS ⟶ RO OUT

VCC ⟶

G ⟶

OFF CHIP: PHASE ROTN   18 PINS   ALTERNATIVE
           VERN. DELAY   VLSI LAYOUT
           (INVALIDATE TIMING)   7/20/84 MSE
ISSUES: PRESCALER SIZE (M)
         WHOLE CHIP INVALIDATE
         NO READOUT OF LSB
         N. LAGS (N)
         HOW TO HANDLE OUTPUT DATA?

SDINV.
PDINV.   ) — CHIP INVAL.

SD IN ——— 2 ———→ | | OVER SAMP | 2 BIT × N S.R. × 4 | ——→ 2 → SD OUT

D CLK ----→

PDIN ——— 2 ———→ (MULT)   →( )   · · ·   →( )

MODE
2/4 LEVEL (?) 3
OVER SAMPLE

PRE SCALE M BIT

SELECT — log₂K → | DE-CODE | | A C C K BITS | | L A T C H | | A C C | | L A T C H | | A C C | | L A T C H |

LOAD ———→

V ———→

G ———→

K

TRISTATE BUS
→ DATA OUT

28 PINS(?)
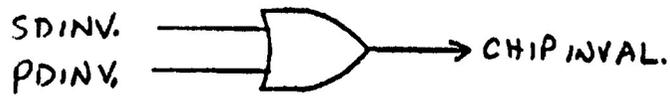
OFFCHIP: PHASE POTN
          VERN. DEL.
          (INVALIDATE TIMING)

ISSUES: TRADE OFF N vs M vs K
        ACCUMULATE TIME, ETC.

ALTERNATIVE
VLSI DESIGN
1/20/84 HJL