AUSTRALIA TELESCOPE CORRELATOR CHIP

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The Australia Telescope Correlator Chip is a full custom VLSI circuit designed by the CSIRO Division of Radiophysics to meet a specific requirement of the Australia Telescope Project. The design uses a 2.5 micron silicon gate NMOS process.

The circuit contains 64 digital correlators, arranged in an eight by eight matrix, fed from a set of eight X inputs and a set of eight Y inputs. Each X input is correlated with every Y input. A correlator multiplies its two input signals and accumulates the result.

The input data format, common to all sixteen inputs, can be either one bit (sign) or two bit serial (magnitude,sign). The circuit has two modes of operation to cover these two input data formats. In both modes, the maximum input data rate is specified at 12 Mbits/sec, at which rate each correlator performs 12 million correlations per sec in one bit mode or 6 million correlations per second in 2 bit mode.

Each correlator consists of an input section which decodes the input data, an 8 bit pipelined Manchester Carry binary up/down counter, an overflow register, a serial adder/subtractor, a 16 bit accumulator shift-register and a 16 bit result shift-register.

In one bit mode, for each input data sample (i.e. bit), the counter counts either +n or -n according to the following table,

Y Input \ X Input	0	1
0	+n	-n
1	-n	+n

where n can be chosen to be 1,4 or 16, determined by two control inputs PCT0 and PCT1.

In two bit mode, the counter counts according to the following truth table.

Y Input \ X Input	11	10	00	01
11	+16	+4	-4	-16
10	+4	+1	-1	-4
00	-4	-1	+1	+4
01	-16	-4	+4	+16

Input data format: (sign,magnitude)

The input BLANK, when active, will cause the chip to cease operation and hold the present accumulated value.

The accumulated result can reach +-2**23 (24 bits) before overflow occurs, however only the most significant 16 bits are available for readout.

There are two control signals which control the acumulation and readout of the circuit. The input WORD occurs once every 16 input samples and defines the serial adder cycle. Every 16 input samples, the LSB of the 16 bit accumulator contents appears at the input to the serial adder. At this time, the output of the overflow register is sampled to determine whether an over- or under-flow of the 8 bit counter occurred during the previous adder cycle. If so, the overflow register is cleared and during the next adder cycle the accumulator contents are incremented or decremented accordingly.

After a (usually large) number of adder cycles the input signal LOAD terminates the accumulation, captures the result, and begins the next accumulation. LOAD becomes active simultaneously with WORD and remains active for one complete adder cycle (16 input samples). At the completion of the load sequence, the accumulator and result register contents have been exchanged, the first adder cycle of the new accumulation has been done (i.e. no loss of data during readout), and all result registers are connected in series. The resulting 1024 bit shift register is shifted out on the SEROUT serial output line during the following 1024 input sample periods, whilst being loaded from the SERIN serial input line. This provides a method of pre-setting the accumulators to particular values at the start of an accumulation. It should be noted that this only applies to

the 16 most significant bits. There is no provision for pre-setting the 8 least significant bits.

Additional Features

The AT correlator chip also contains a programmable delay section, acting on all 16 input signals. To explain the function of this section, some details of the intended application of the chip to the AT need to be understood.

In the AT correlator, the chips are arranged in four by four arrays to make up a module containing a 32 by 32 array of correlators. These are fed from two 1 to 32 line serial to parrallel converters with input data rates of 320 Mbits/sec (in one bit mode) and output rates of 10 Mwords/sec. (1 word = 32 bits). A module therefore provides a measure of the cross correlation function of the two serial input streams over a range of +-32 sample lags and with a triangular weighting function. If the input data rate is halved, but the data is still clocked in at 320 Mbits/sec, only a quarter of the available correlators provide non-redundant information. Under these conditions, the delay section, suitably programmed, will allow the remaining three quarters to measure other lag values, thereby increasing the total lag measurement range. This process can be continued until the input data rate has been reduced by a factor of 32, there being only one active X and Y input to the 32 by 32 correlator array. The module then provides a complete 1024 lag measurement for each input sample pair. To achieve this feature,the necessary connection between ajacent chips in the array is accomplished through the outputs XOUT.8 and YOUT.8 and the inputs XCASCIN and YCASCIN.

The delay section is programmed with serial data to the PROGIN input. This data is clocked in with clock inputs PHPA and PHPB. The PROGOUT output allows chips to be chained together for programming.

Clock Generator

The correlator chip has an on-chip clock generator to produce the required two phase (for one bit mode) or four phase (for two bit mode) internal clock signals. The inputs PHID and SYNCH control and synchronise the clock generator to the input data.

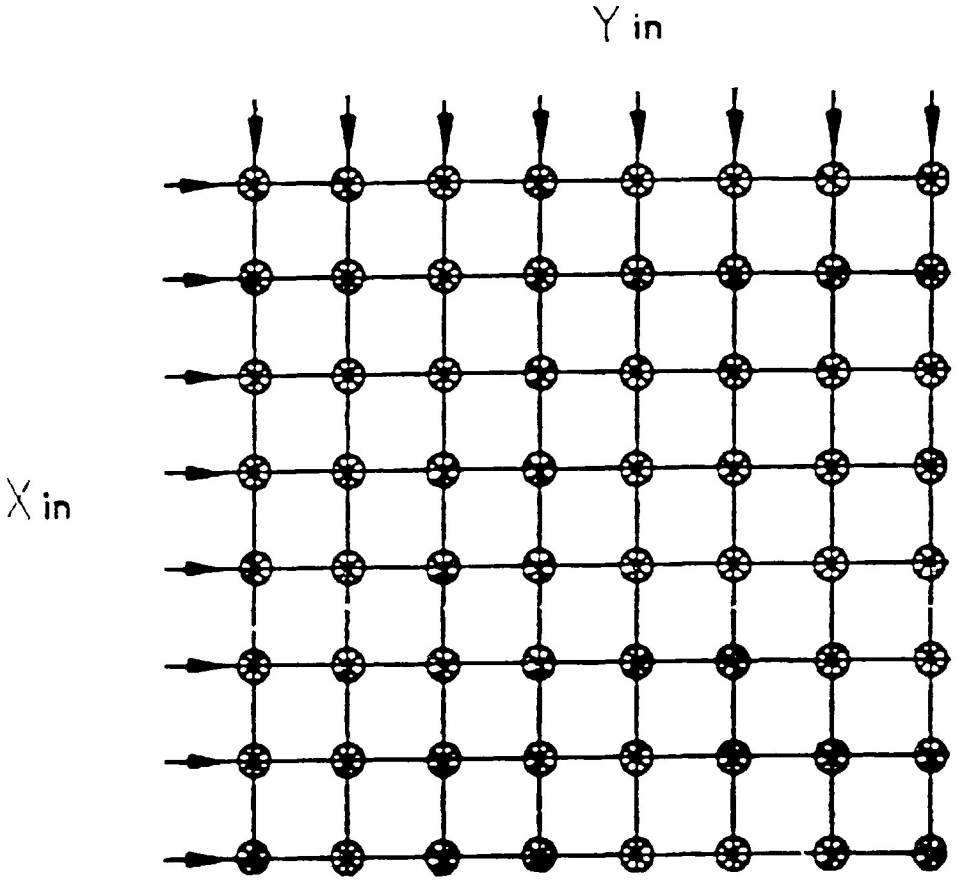
Packaging

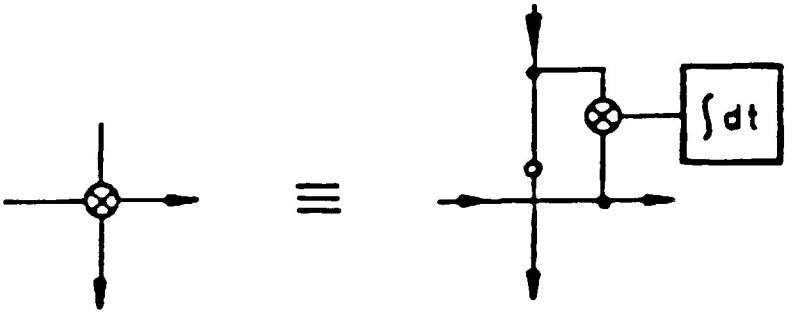
The chip is packaged in a standard 40 pin dual in line ceramic package. A preliminary pinout is shown below.

Pin	Signal	Pin	Signal
1	X.8	21	Y.8
2	XCASCIN	22	Y.7
3	nc	23	Y.6
4	nc	24	VDD (5V)
5	GND	25	Y.4
6	nc	26	Y.3
7	XOUT.8	27	Y.2
8	PCT1	28	Y.5
9	PCT0	29	Y.1
10	BLANK	30	PROGOUT
11	SEROUT	31	PHPA
12	SERIN	32	PHPB
13	WORD	33	PROGIN
14	LOAD	34	X.1
15	YOUT.8	35	X.5
16	nc	36	X.2
17	nc	37	X.3
18	PHID	38	X.4
19	SYNCH	39	X.6
20	YCASCIN	40	X.7

NOTE

A second chip, providing a programmable delay function at variable signal widths (up to 16 inputs and outputs) is also under development. Two of these chips, placed between two of the correlator modules descibed above, allow the modules to be concatenated, to give an increased lag coverage.

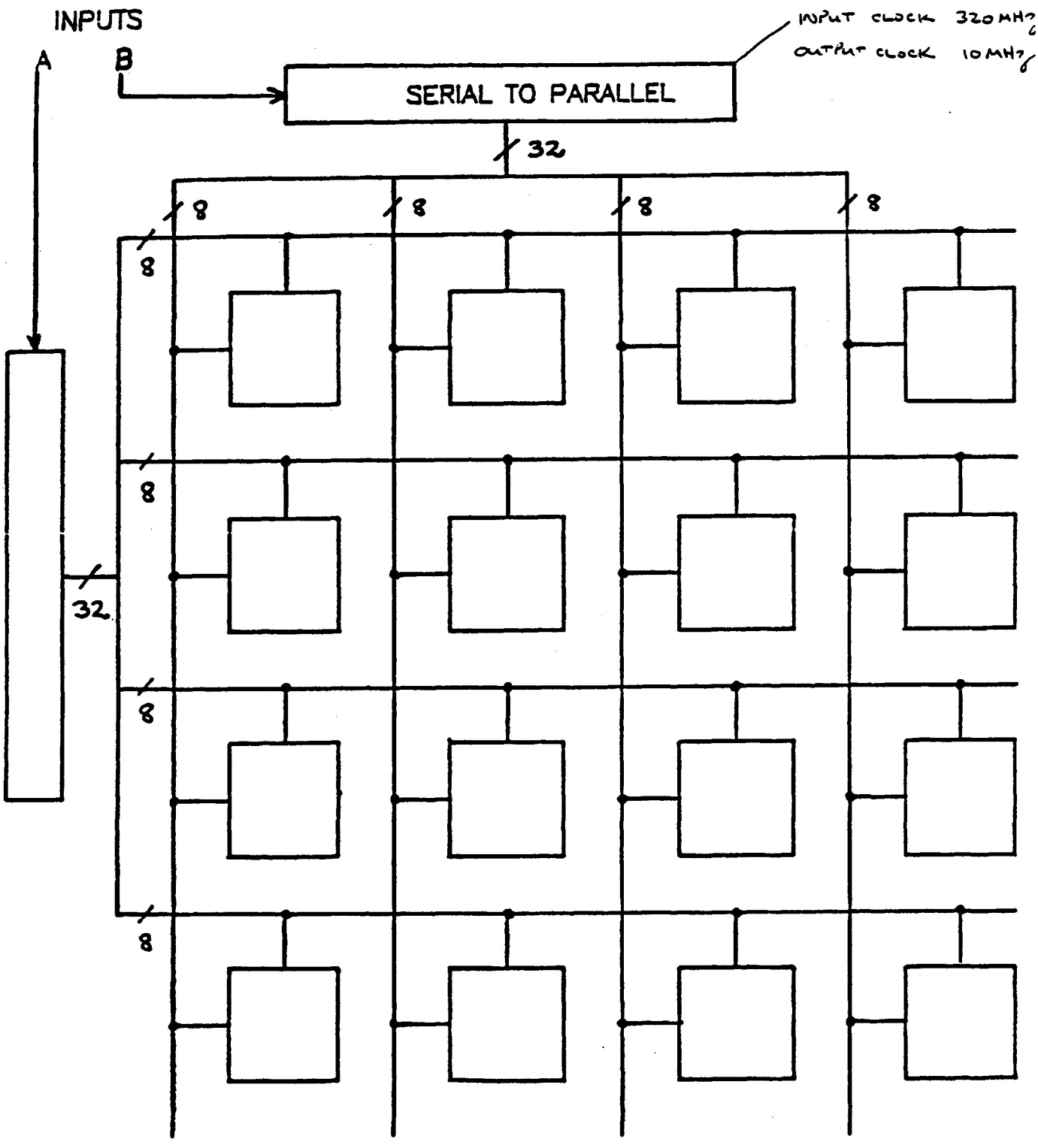




Multiplier accumulator

An 8 x 8 correlator chip

CORRELATOR MODULE



K = RECONFIGURATION FACTOR

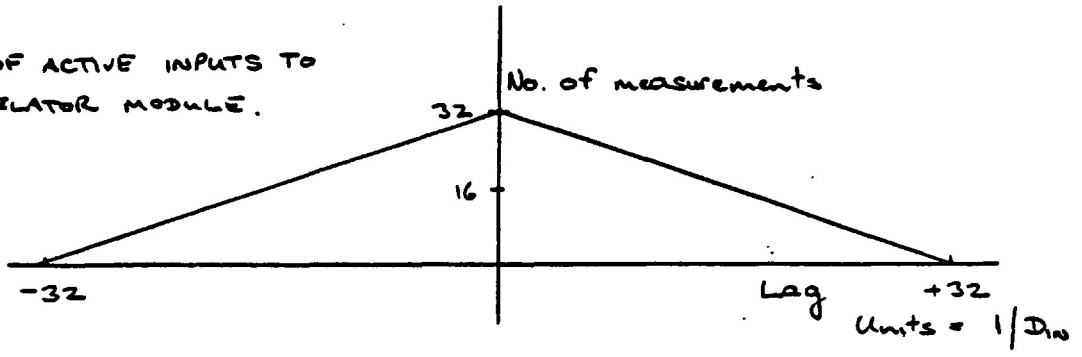
D_{IN} = INPUT DATA RATE AT A & B

I_{ACT} = NO. OF ACTIVE INPUTS TO CORRELATOR MODULE.

K = 1

D_{IN} = 320 Mbits/sec

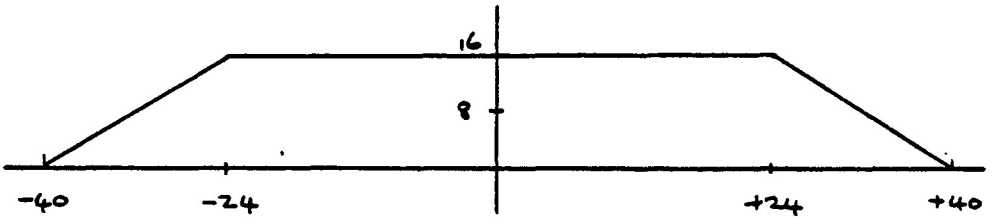
I_{ACT} = 32



K = 2

D_{IN} = 160 Mbits/sec

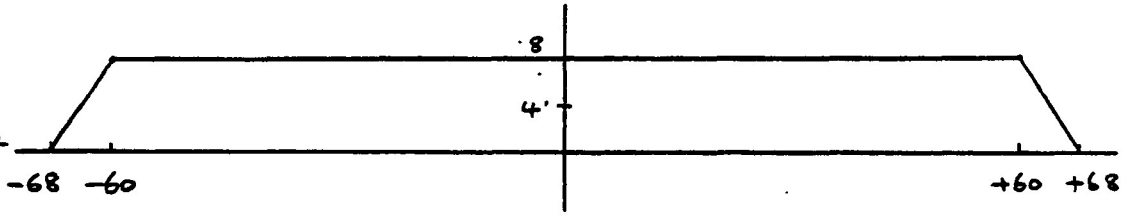
I_{ACT} = 16



K = 4

D_{IN} = 80 Mbits/sec

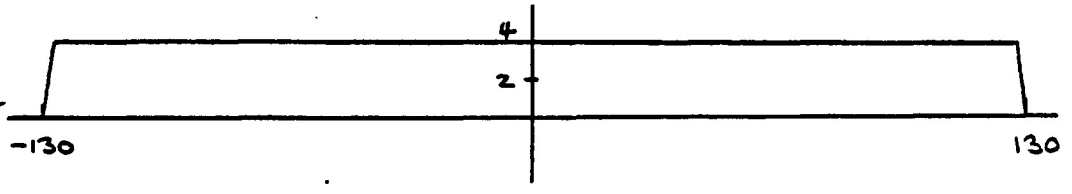
I_{ACT} = 8



K = 8

D_{IN} = 40 Mbits/sec

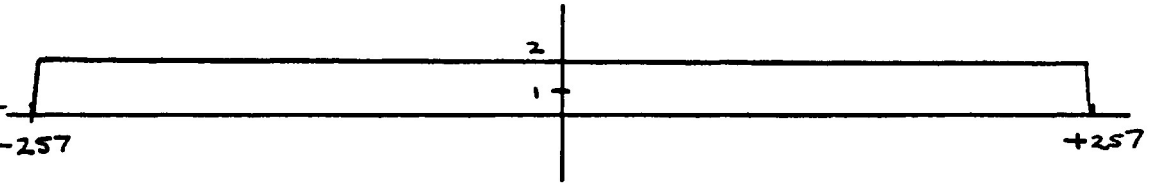
I_{ACT} = 4



K = 16

D_{IN} = 20 Mbits/sec

I_{ACT} = 2



K = 32

D_{IN} = 10 Mbits/sec

I_{ACT} = 1