VLBA CORRELATOR MEMO
VC 044
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Subject: Per Station Delay and Phase Accuracy

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This note looks at the number of bits of fractional delay and phase that must be sent to the VLSI chip to prevent significant loss of SNR.

Delay:

Consider the case where 2 bits of fractional delay from each station are sent to the VLSI chip to implement the vernier delay correction. Each delay can have the values 0, 1, 2 or 3 +/- 1/2 in units of one quarter of a bit. After subtraction the result can have the values -3, -2, -1, 0, 1, 2 or 3 +/- 1. The number of ways of obtaining each result is 1, 2, 3, 4, 3, 2, 1 respectively. If the vernier delay is now adjusted to change the +/- 3 states to -/+ 1 then the resulting states are -2, -1, 0, 1 or 2 +/- 1 (still in units of one quarter bit). The number of ways of obtaining each result is 2, 4, 4, 4, 2 respectively. It can be seen that the delay error can be greater than plus or minus half a bit but, statistically, the fraction of the results that are in the range (1/2,3/4) or (-1/2,-3/4) is smaller than other 1/4 bit error ranges. In fact, 12.5% of the results are outside (-1/2,1/2) and 50% are inside (-1/4,1/4). Integrating sinx/x over the three error ranges one gets the following.

Error Range	Mean Error	% of Time	sinx/x
>1/2 bit	0.625 bit	12.5%	0.845
<1/2>1/4 bit	0.375 bit	37.5%	0.941
<1/4 bit	0.125 bit	50.0%	0.992

The weighted mean sinx/x amplitude is 0.955 compared to 0.966 for the case where the station delays are subtracted with a large number of bits (which produces a uniform error distribution over (-1/2,1/2). Therefore, a loss of 1.1% in SNR would result if only 2 fractional bits are sent for each station.

The same analysis can be made for the case of sending 3 bits. The result is a loss of 0.3%. Therefore, it would seem necessary to send at least 3 bits of fractional delay in our per station scheme. It should be noted that the spectral line case will incur greater losses at the bandedges and more bits would be useful.

Phase:

Exactly the same calculations can be made for phase if the first three bits of phase are considered to be integral 'bits' of the 8 segment 3-level fringe rotation waveform and the remaining bits are then the fractional bits. In order to reduce the SNR loss to 0.3%, a total of 6 phase bits should be sent.

The total number of delay and phase bits to be sent are then 9 for an SNR loss of 0.6% . This is a rather inconvenient number of bits, albeit possible. It would also be possible to send the fractional delay on one wire and the phase on another or send incremental values. However, sending both in 8 bits on one wire would be preferable. The following discussion illustrates a different way of looking at the problem which suggests another solution.

Consider the case where only one bit of fractional delay is sent. This case is equivalent to the one where four bits of phase are sent. The station states are 0 or 1 +/- 1/2 in units of half a bit. After differencing the two stations, the states are -1, 0 or 1 +/- 1 and can be obtained in 1, 2 or 1 ways respectively. There is no way of using this information unless the vernier delay could be applied in units of half a bit. If this could be done, then the error range could be reduced to (-1/2,1/2) uniformly distributed and all would be well. Vernier delays of +/- half a bit are tricky but 'vernier' phases of +/- one half of an eighth of a turn are not.

What is needed is a fringe rotator waveform with 16 phase bins. The waveform should also be symmetric about the zero phase bin or a constant phase bias results. These conditions leave only two reasonable 3-level waveforms, namely

1 1 1 0 0 0 -1 -1 -1 -1 -1 0 0 0 1 1

and 1 1 1 1 0 -1 -1 -1 -1 -1 -1 -1 0 1 1 1 (cosine).

Unfortunately, the fundamental content of these waveforms is about 2% lower than that of the tried and true 8 bin waveform. If, however, more levels are allowed, things are better. For example, consider

W W W 1 0 -1 -W -W -W -W -W -1 0 1 W W.

For W=3 and W=4 the fundamental content is 98.2% and 97.7% respectively compared to 96.1% for the conventional 3-level waveform. Actually, there is additional SNR loss because the phase error range is twice that for the ideal case. A simulation of the four bit phase subtraction gives 97.6% and 97.0% for W=3 and W=4 respectively. A bit more SNR loss would result from the probable use of an incomplete multiplier for the fringe rotator.

It would seem possible to implement the 5-level fringe rotator and maintain or slightly improve the SNR relative to the normal 3 level case while sending only 4 phase bits. In this case, 4 fractional delay bits might as well be sent and make the SNR loss due to delay error negligible.