VLBA Correlator Memo No. 61

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MEMORANDUM:

TO: VLBA Correlator Group

FROM: R. Escoffier/J. Benson

SUBJECT: VLBA Correlator Block Diagram

I. Introduction

This memo will describe, at the block diagram level, a design for the VLBA correlator. This design is of the "FX" type as described in Romney VLBA Correlator Memo No. 60.

Figure 1 illustrates the VLBA correlator design now being considered. This FX, or FFT first, design will, it is hoped, result in a VLBA correlator of both substantially higher performance and substantially lower cost compared to a conventional lag correlator. Blocks marked with a question mark (?) represent functions that may not be needed.

II. Station Electronics

The block of Figure 1 marked data buffer is an earth radius delay line. This buffer will provide rapid delay changes to synchronize the station data streams and will be implemented in RAM logic.

The station based lobe rotators are digital mixers that will multiply the incoming sample streams by quadrature components of the station fringe phases. This multiply produces "complex" samples for the FFT input.

The station FFT logic will take groups of 2^N consecutive samples from each channel and Fourier transform them into station voltage spectra. The requirement to Fourier transform many fast sample streams is severe and will require many dedicated logic FFT circuits but seems, at this time, to be practical using inexpensive off-the-shelf digital logic or custom gate array logic.

A correction for the sample time error, the "fractional bit shift", will be done at the FFT output by multiplying the output by a phase slope across the voltage spectra. This phase slope will cancel the phase slope introduced by any fractional bit sample time error.

Addresses for the data buffer, fringe phases for lobe rotation, and slope parameters for the fractional bit shift correction will probably be produced by hardware Taylor series model generators as described by Greenberg VLBA Correlator Memo No. 63. A sufficiently long Taylor series could reduce the computer generated

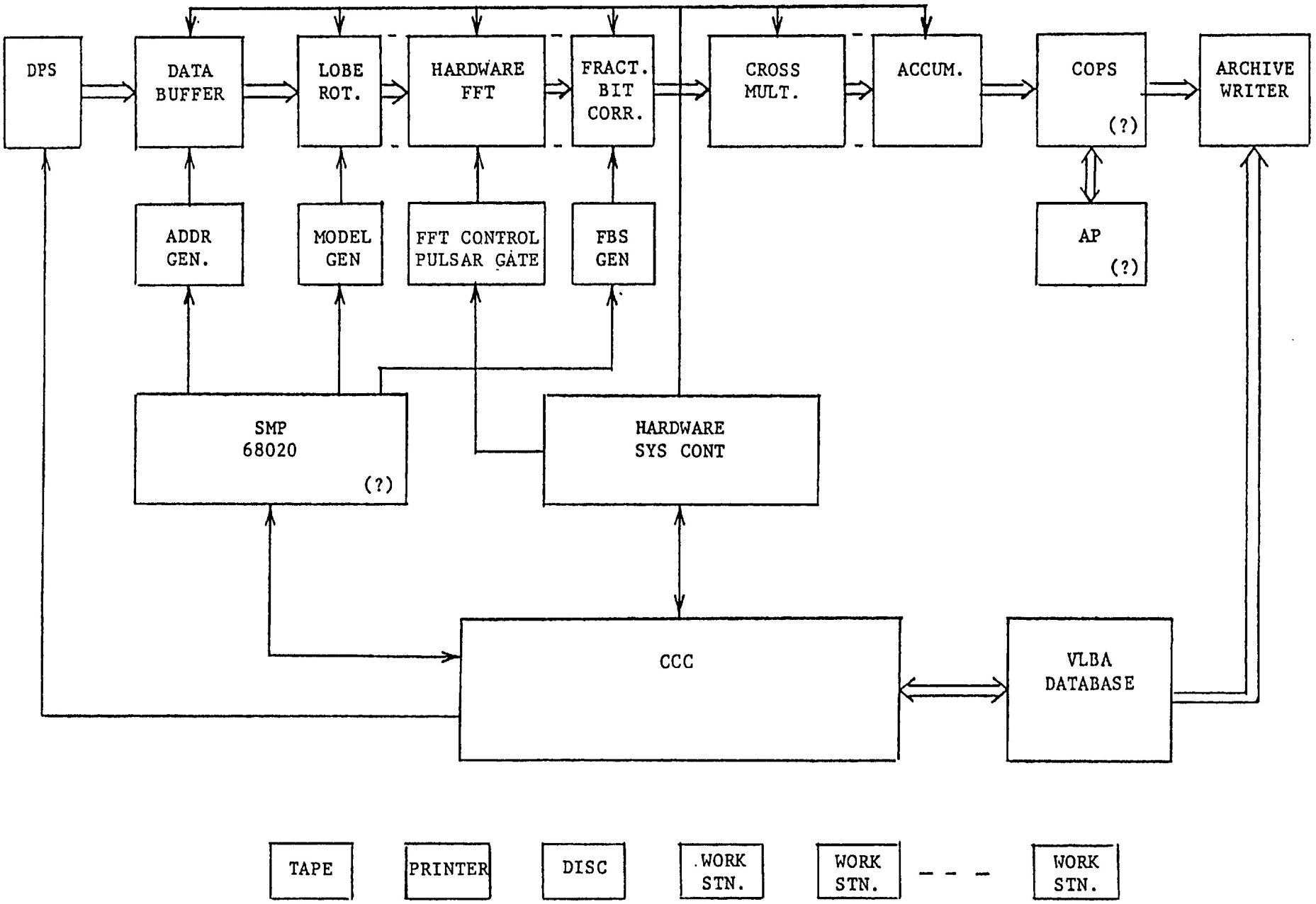

Fig. 1. VLBA correlator block diagram.

model update rate to levels that would require no dedicated station processor. In this case, the correlator control computer would handle all model updating and no SMP's as shown in Figure 1 would be required.

Pulsar gating will be provided by performing Fourier transforms only on samples taken during pulsar on times.

III. Baseline Electronics

The baseline electronics will perform complex cross multiplies of the station voltage spectra and will do short term accumulation.

The FFT operation has resulted in a substantial reduction in multiplies per second from that required in the baseline electronics of a lag correlator at the cost of more complicated multiplies. Depending on the resolution needed for the cross multiplies, either ROM look-up table, gate array, or parallel multiplier IC's will be used in the baseline electronics.

Another difference between this FX approach and a lag correlator is that the trade-off of resolution and stations can no longer be made. Hence, a simple 20-station correlator is contemplated. The reduced cost of the baseline electronics of the FX correlator makes this move possible and a simpler overall architecture and enhanced performance result.

The accumulator is, however, made more difficult by the improved performance (more spectral points). At this time, it looks as if 389,120 terms must be kept for the accumulator.

IV. Correlator Back-End Computing

The amount of computing power required at the correlator back-end is, at this time, not well understood. The data has already been Fourier transformed and this fact should reduce the back-end computing requirements but the requirements of quantization correction, normalizations, tape formatting, etc. still remain to be defined.