VLBA Correlator Memo No. 62

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MEMORANDUM:

TO: VLBA Correlator Group

FROM: R. Escoffier

SUBJECT: VLBA Correlator Hardware Design

I. Introduction

This memo will present a preliminary hardware overview of the proposed VLBA "FX" correlator. Subjects covered will include system performance and rough block diagrams of internal functions.

Figure 1 gives a block diagram of a FX-type VLBA correlator.

II. Performance

Table I gives a brief summary of correlator performance so far as spectral resolution is concerned.

TABLE I

Channel-Phase Center Product	Spectral Points	Stations
1	1024	20
2 Non-Polarized	512	20
2 Polarized*	256	20
4 Non-Polarized	256	20
4 Polarized	128	20
8 Non-Polarized	32	20
8 Polarized	32	14

*Two-channel polarized operation is defined as processing observations made over one frequency band with two active IF's (channels), one for each polarization. All four polarizations products are computed.

The station based FFT hardware will produce station voltage spectra with 2048 (1, 2, 4 channel) or 512 (8 channel) spectral points, and this resolution is carried through the baseline cross-multiplication. From 2 to 16 adjacent spectral cross products are summed together before accumulation producing the final cross spectral resolution of Table I.

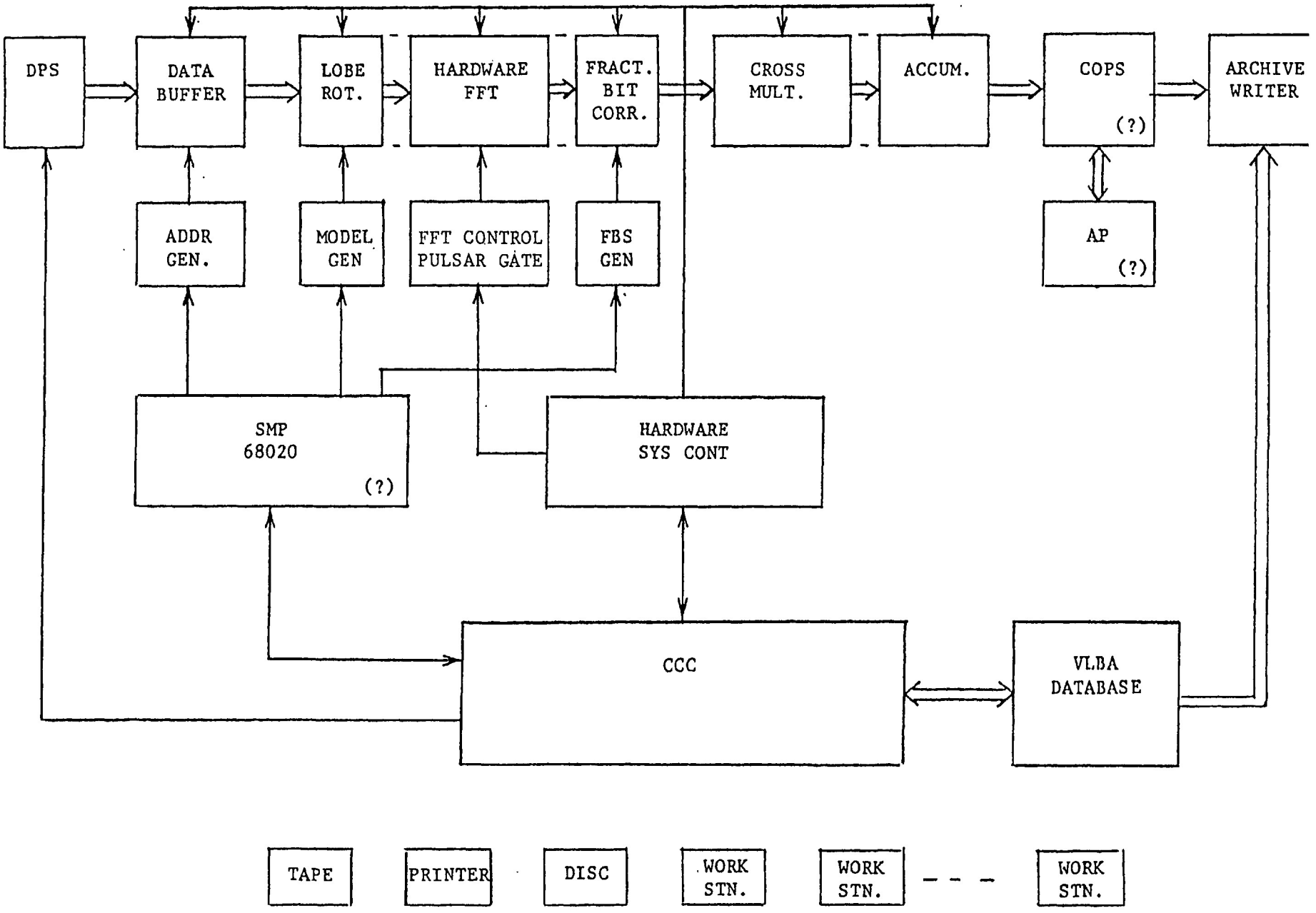


Fig. 1. VLBA correlator block diagram.

III. Data Buffer

The data buffer is an earth radius delay line used to rapidly phase the station sample streams. A total 21 msec delay range at 32 Mbs will require about 1 Mbit of RAM per sample/validity bit. About 1500 256K RAM and control IC's are required to provide this function for a 20-station correlator.

IV. Lobe Rotation

Lobe rotation will be accomplished via a digital mixer as shown in Figure 2.

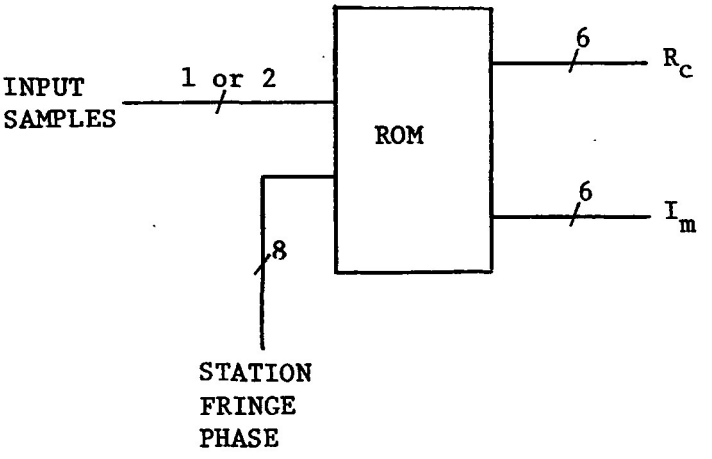


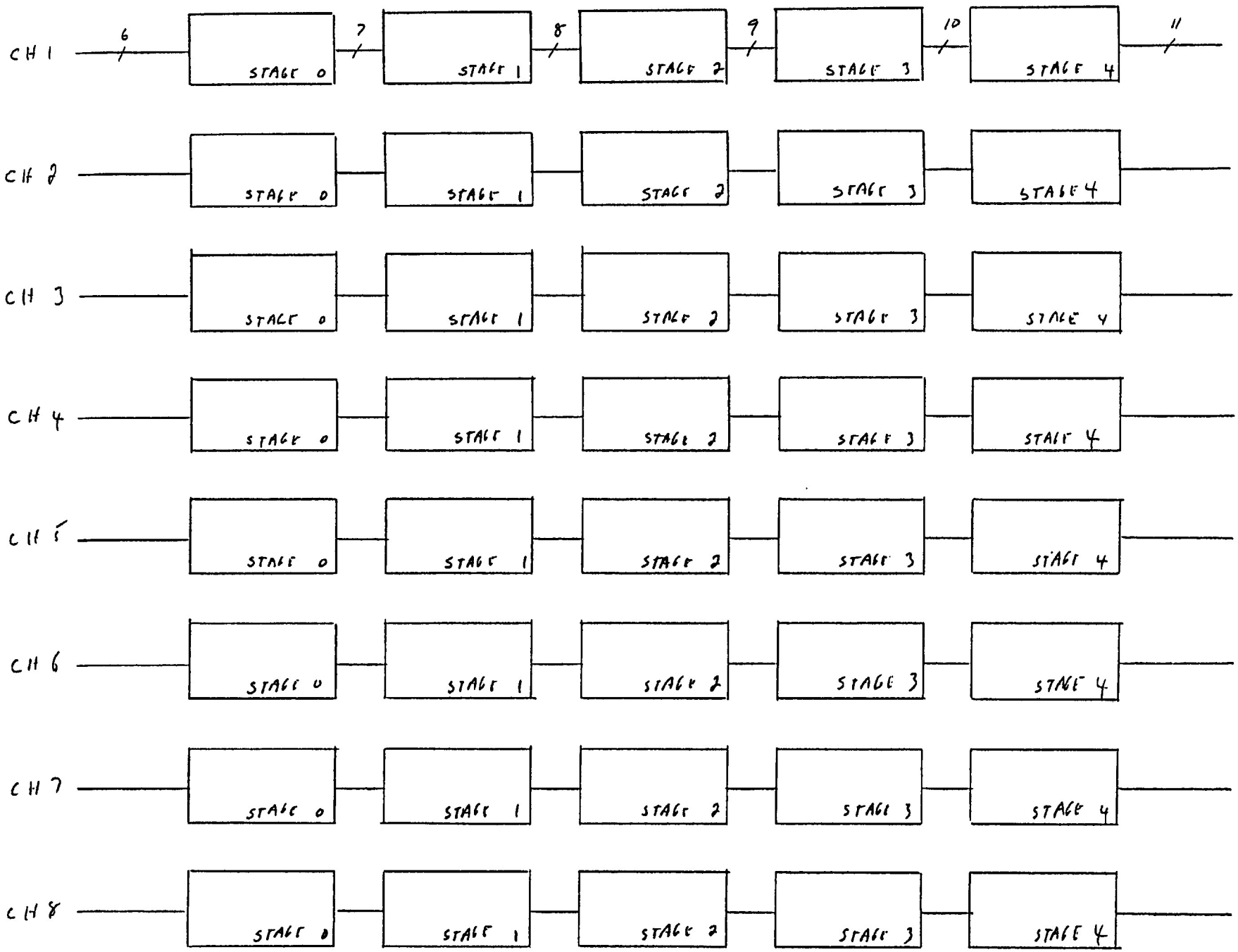
Fig. 2

Each one- or two-bit sample will be multiplied, in a look-up table ROM, by the sine and cosine of a station (channel) fringe phase quantized in magnitude to 8 bits and in time to 31.25 nsec (playback time). Output quantization to 6 bits will be assumed in this memo.

V. FFT

Figures 3 through 6 give, in block diagram form, a description of the station based FFT hardware. In each figure the logic required for one antenna is presented. Each box shown in these figures is a hardware Radix 4 FFT butterfly.

Figure 3 illustrates the electronics required for one antenna operated in 8 channel mode. Eight parallel 1024 point hardware FFT's are performed using a Radix 4 implementation. Input quantization is at 6 bits each for the real and imaginary lobe rotator outputs and the level of resolution is allowed to grow at 1 bit per Radix 4 butterfly stage. Thus, this figure depicts hardware that would perform eight 1024 point FFT's at the maximum playback rate.



ALL BOXES ARE RADIX 4
FFT HARDWARE BUTTERFLYS

8 CH MODE

FFT LENGTH 1024

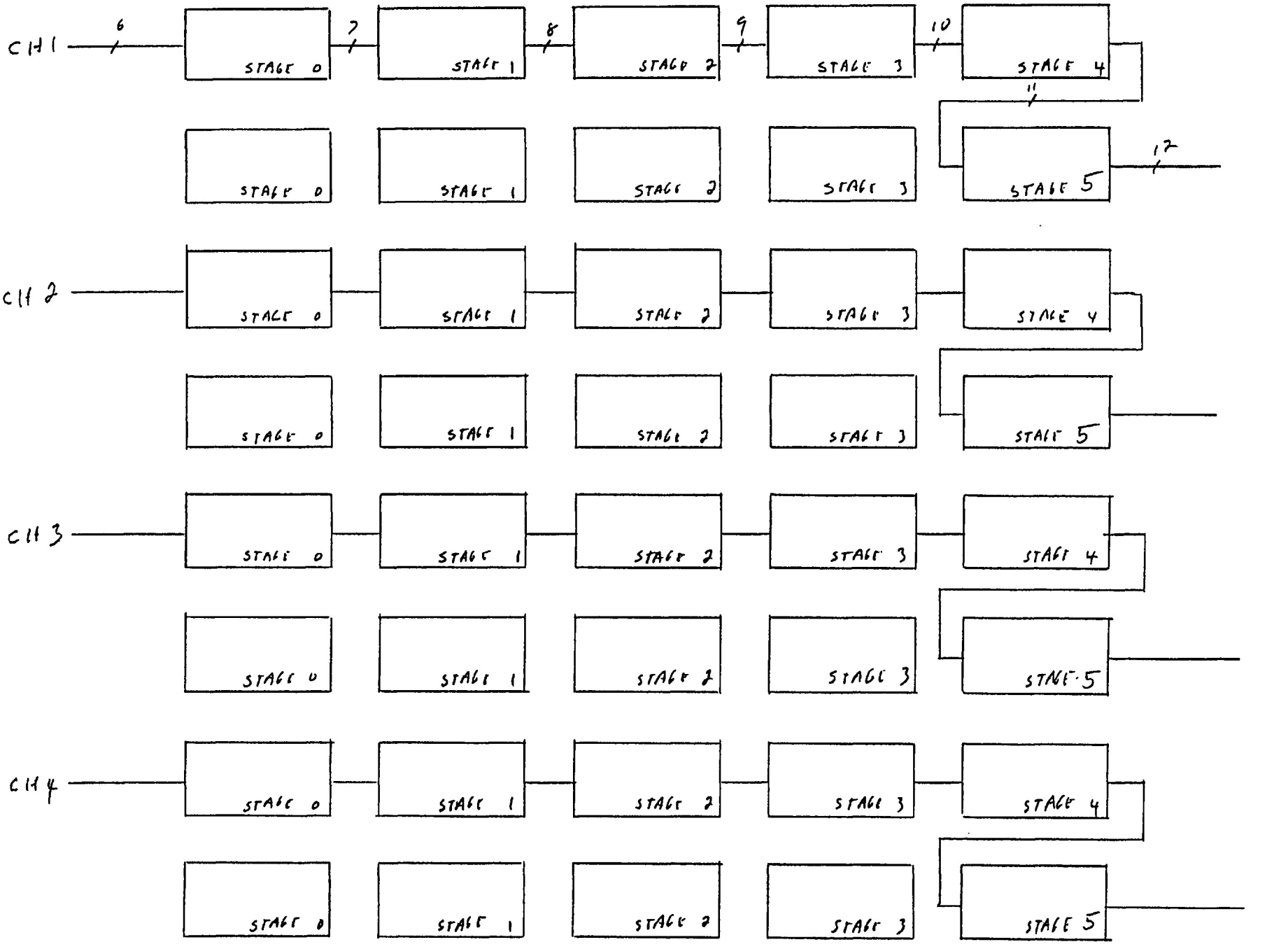

CH 1
CH 2
CH 3
CH 4
STAGE 0
STAGE 1
STAGE 2
STAGE 3
STAGE 4
STAGE 5
6
7
8
9
10
11
12
ALL BOXES ARE RADIX 4
FFT HARDWARE BUTTERFLYS
4 CH MODE
FFT LENGTH 4096

Fig. 4

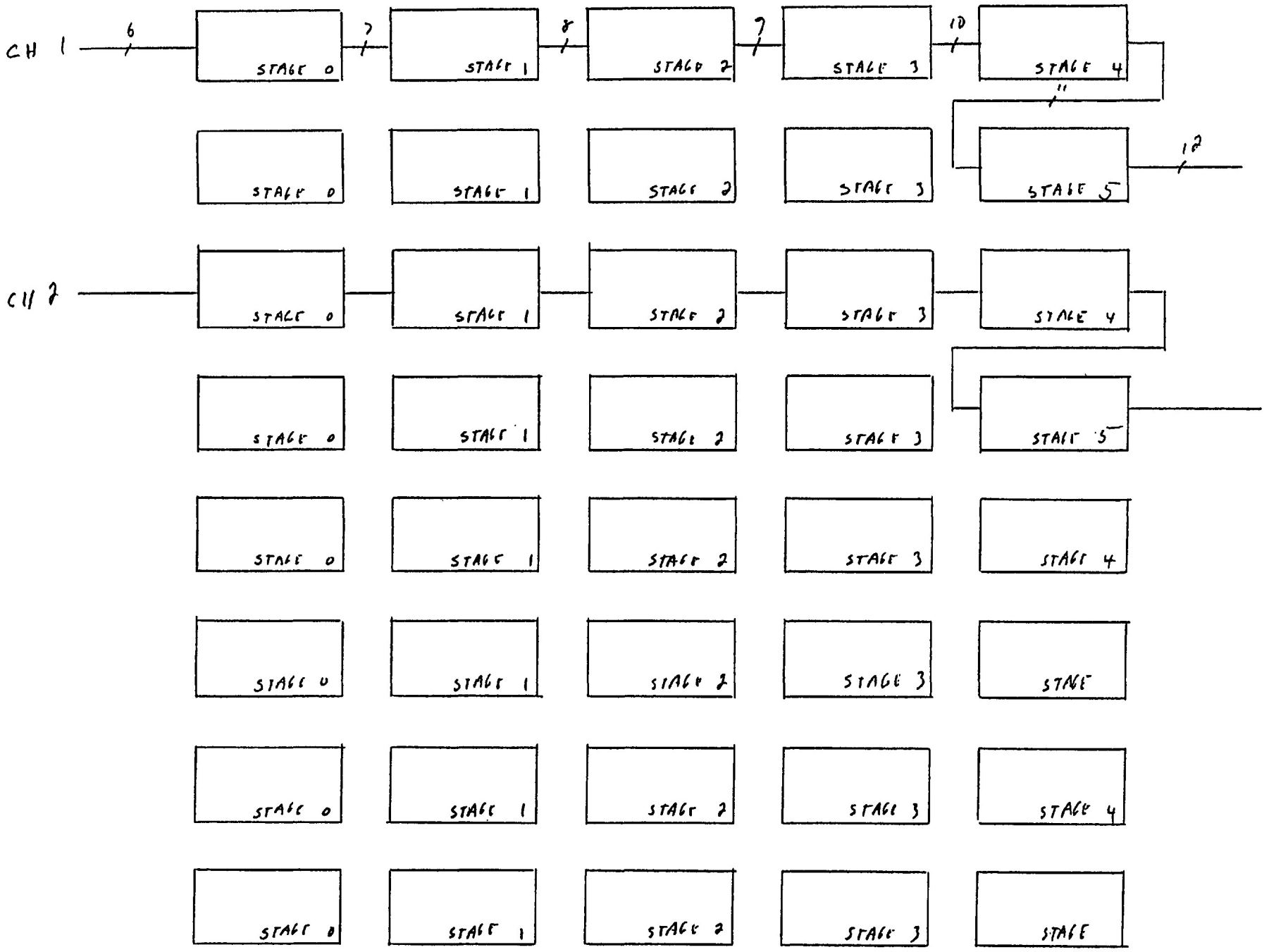

CH 1
6
7
8
7
10
11
12
STAGE 0
STAGE 1
STAGE 2
STAGE 3
STAGE 4
STAGE 5
CH 2
ALL BOXES ARE RADIX 4 FFT HARDWARE BUTTERFLYS
2 CH MODE
FFT LENGTH 4096

Fig. 5

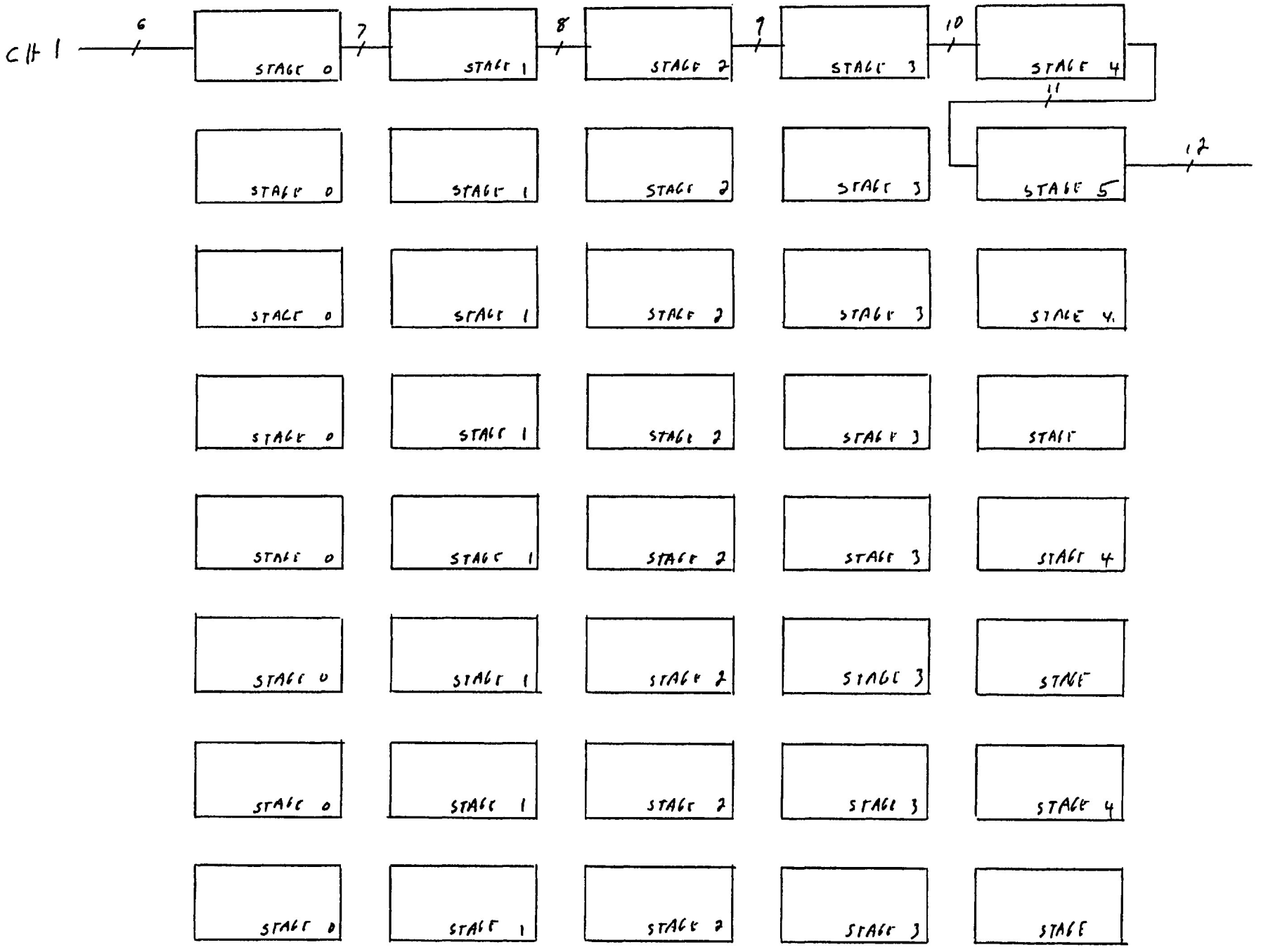

CH 1
6
7
8
9
10
11
12
STAGE 0
STAGE 1
STAGE 2
STAGE 3
STAGE 4
STAGE 5
ALL BOXES ARE RADIX 4
FFT HARDWARE BUTTERFLYS
1 CH MODE
FFT LENGTH 4096

Fig. 6

Figure 4 shows the circuit utilization for 4 channel operation and how four parallel 4096 PT FFT's are performed by using the final butterfly stage of unused hardware FFT logic. Figure 5 shows 2 channel operation and Figure 6 is 1 channel operation.

Figure 7 is a diagram of a Radix 4 FFT butterfly. A Radix 4 FFT implementation seems, at this time, to have significant advantages over a more conventional Radix 2 architecture, but more study is needed before a final design is chosen. Figures 8A and 8B show a possible gate array IC that would fit an entire Radix-4 FFT butterfly on a single chip (alternately, Figure 8A could be a smaller chip and 8B a second smaller chip). Figure 8A shows a 12-bit complex multiplier which is time shared among four input samples in the four clock periods in which it is necessary to do a Radix 4 butterfly, and Figure 8B shows a four-way adder which is multiplexed among the four complex multiplier products to form the eight (four real and four imaginary) butterfly outputs. This chip would reduce the entire station FFT engine to a simple, small design. In addition, the butterfly adder section (Figure 8B) could be bypassed and the complex multiply portion of this IC used for both the fractional bit correction complex multiply and the baseline multiplies.

Other FFT options being considered include using floating point arithmetic in the FFT computation or using a sign/logarithm implementation.

VI. Fractional Bit Correction

This block of Figure 1 requires a complex multiply circuit at the output of each FFT. Since spectral points will come out of the FFT logic in serial form, this block should amount to just the complex multiply logic of the gate array IC described above for each cnannel.

VII. Cross Multipliers

The requirements of the cross multipliers can be calculated in multiplies per second, worse case, as below:

8	channels/station
190	baselines (20 stations)
128	spectral points
4	factor for complex multiply
778,240	multiplies in the 8 μsec it took to accumulate the 256 points FFT'ed.

or 9.728×10^{10} multiplies/second

The complex multiplier portion of Figure 8 is, again, applicable to the baseline multipliers. By adding a little extra logic on the butterfly gate array, the butterfly adder stage can be bypassed and a baseline adder inserted so that a RAM can be directly connected to the chip.

VIII. Accumulation

The tabulation, below, computes the number of accumulator terms that must be supported by the VLBA correlator accumulator (worst case):

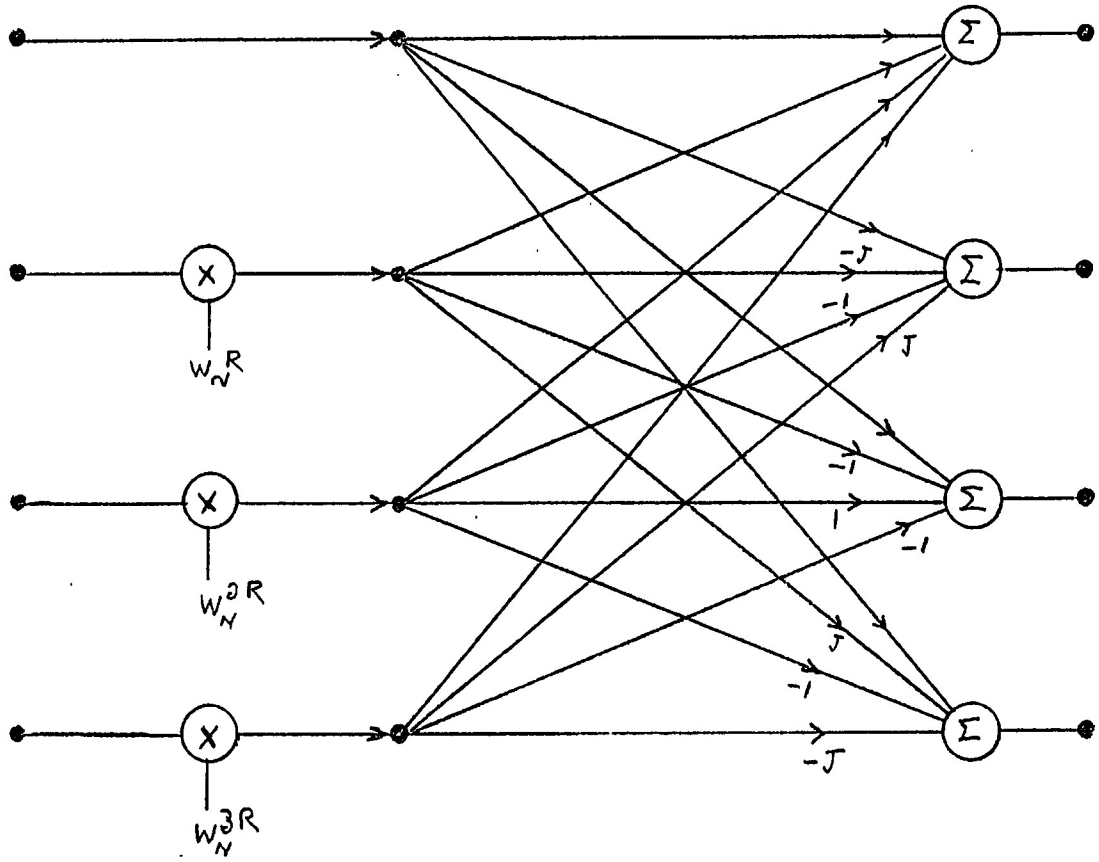
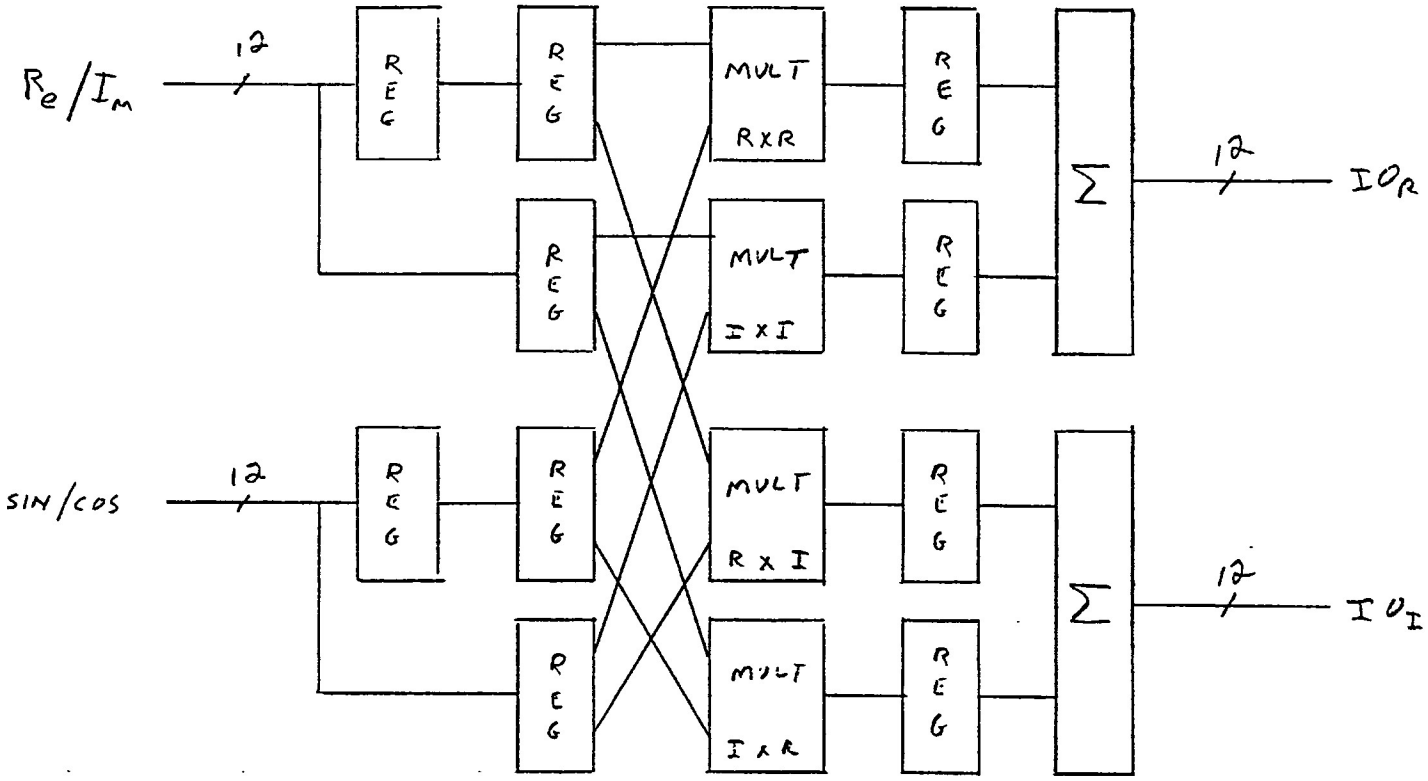


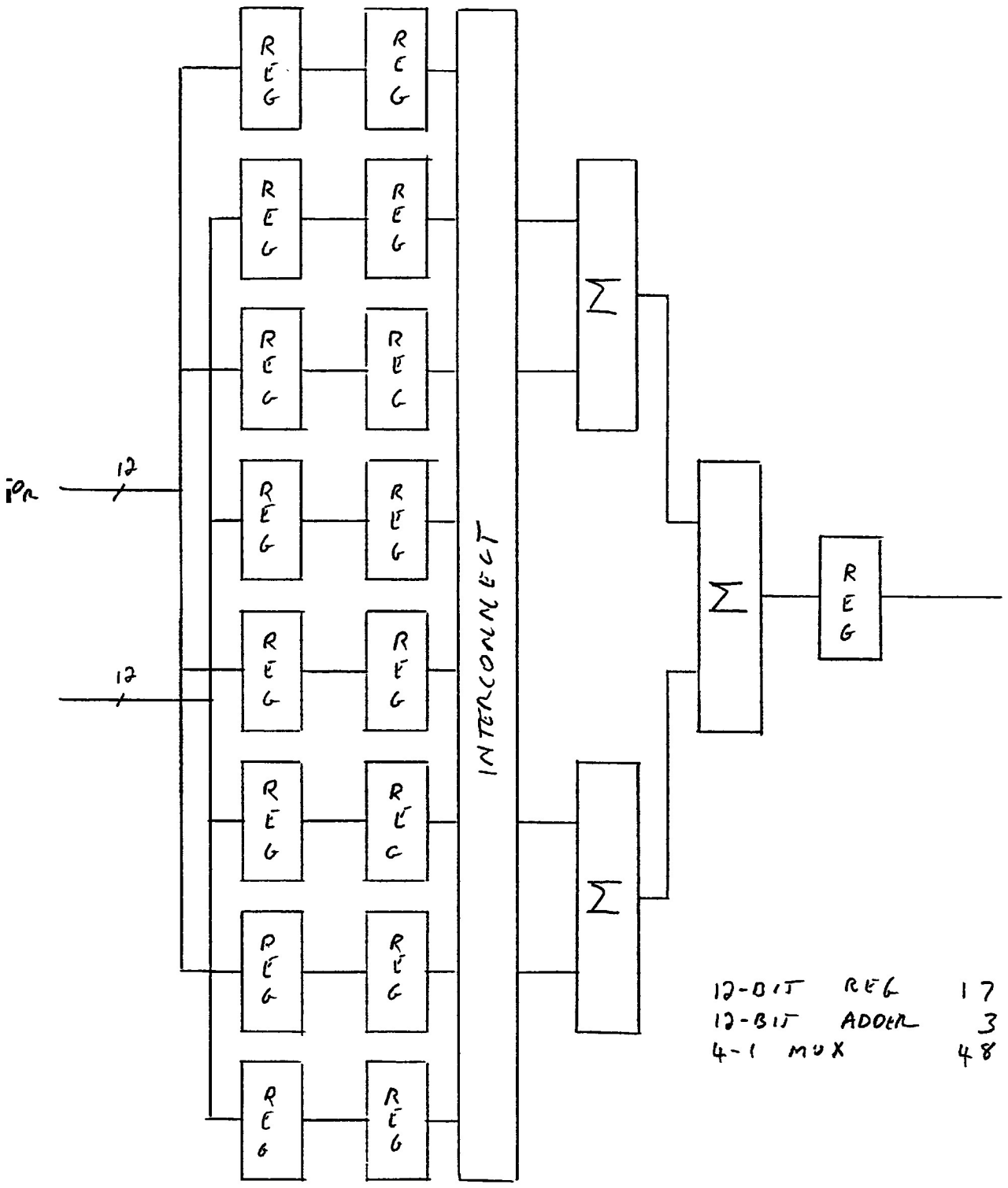
Fig. 7. Radix 4 DIT FFT butterfly.



12-BIT	REG	10	600 GATES
12-BIT	MULT	4	4408 GATES
12-BIT	ADDER	2	408 GATES
			5416 GATES

5416
1944
7360

Fig. 8A



12-BIT	REG	17	1020 GATES
12-BIT	ADDER	3	612 GATES
4-1	MUX	48	312 GATES
			1944 GATES

Fig. 8B

4 channel/station
190 baseline (20 stations)
128 point spectra
2 factor for polarization
2 factor for complex points

or 389,120 terms!

The accumulator design is made easier by doing longer fast Fourier transforms than is needed and summing adjacent cross spectral points before accumulation. Table 2 gives the "summation factor" in each mode.

TABLE 2

Mode	FFT Length	Spectral Points In Baseline Mult.	Spectral Points Into Accumulator	"Summation Factor"	Effective "Summation Factor"
1 CH	4096	2048	1024	2	16
2 CH NP	4096	2048	512	4	16
2 CH P	4096	2048	256	8	16
4 CH NP	4096	2048	256	8	16
4 CH P	4096	2048	128	16	16
8 CH NP	1024	512	32	16	16
8 CH P	1024	512	32	16	16

The effective summation factor reflects the dispersion of the station voltage spectral points into the baseline multipliers. For example, in 1 channel mode the voltage spectra can be dispersed through the eight sets of baseline multipliers needed to support 8 channel mode.

XIX. Control Logic

The levels of control logic shown in Figure 1 include:

1) Data buffer control
2) Lobe rotator model generation
3) FFT control
4) Pulsar gate generator
5) Fractional bit shift parameter generator
6) Master system control

Items 1, 2, 4 and 5, above, will probably be done in hardware Taylor series model generators of the type described in Greenberg's VLBA Correlator Memo No 63. At this time it looks as if this technique will be a low cost way of tracking model parameter for a few minutes at a time. If the update rate for computer generated models can be reduced sufficiently, all such requirements can be met by the correlator control computer.

The master system control function will probably be a fast 8-bit or 16-bit microprocessor programmed to do hardware control functions in assembly language.